Silicon Test Wafer Specification for 180 nm Technology

Technology Transfer # **97113407A-ENG**
International 300 mm Initiative
December 3, 1997

Abstract: This document describes silicon wafer specifications suitable for International 300 mm Initiative (I300I) 180 nm demonstrations in 1998. The specifications were developed in conjunction with the I300I Silicon Working Group and SEMI Standards.

Keywords: 300 mm Wafers, Specifications, Silicon

Authors: Randy Goodall

Approvals: Randy Goodall, Associate Director of Productivity and Infrastructure
Laurie Modrey, Technical Information Transfer Team Leader

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1 INTRODUCTION

In 1998, the International 300 mm Initiative (I300I) demonstration and characterization programs will focus on 180 nm technology capability. To support these activities, I300I and equipment supplier demonstration partners must use starting silicon wafers with key parameters specified at a level appropriate level for 180 nm processing, including contamination and lithographic patterning. This document describes I300I's silicon wafer specifications, as developed with the I300I Silicon Working Group (member company technical advisors) and SEMI Standards. These specifications, with accompanying guidance and precautions, can be used by equipment suppliers and others who provide wafers for I300I tests in 1998. Note, however, that silicon wafers are among the most highly engineered, man-made substances, and instructions for the complete technical specification of wafers is beyond the scope of this document. Contacts at I300I (see below) can provide additional information.

Note that these specifications supersede any previously distributed specifications for 180 nm technology and/or I300I purchases to support 1998 demonstrations.

2 RELEVANT STANDARDS

I300I strongly supports global standardization of all aspects of silicon wafer specification. The I300I specifications use the format, parameters, and values of relevant SEMI standards as extensively as possible. The SEMI standards M1.15 (basic 300 mm prime wafer) and M28-97 (development wafer) were passed in March 1997. These standards were targeted to support 0.25 µm technology (particularly M28-97), but in many cases the values are acceptable for 180 nm. Use of these and other standards is noted; exceptions are shaded.

The 1997 *National Technology Roadmap for Semiconductors* is also used by I300I as a basic guideline for performance targets for 300 mm 180 nm technology. Its use as a source of specification values is noted.

3 WAFER TYPES

Four types of wafers are specified, with associated applications, as noted in the following table.

Wafer Type	I300I ID	Characteristics	Application	Key Parameters
Mechanical	TW301-180	basic dimensions	handling tests, fillers	diameter, thickness
Furnace	TW302-180	low metals, controlled LLSs[1]	thermal tests, process characterization, cleaning tests	metals, LLSs
Particle	TW303-180	very low particles, controlled crystal defects (COPs[2])	particle-per-wafer-pass tests, cleaning tests	particles, haze, COPs
Lithography	TW304-180	low flatness[3], controlled LLSs	any patterned wafer tests	TTV, site flatness, LLSs

[1]LLSs ≡ localized light scatterers (particles and COPs seen by particle detector)
[2]COPs ≡ crystal originated pits (seen by particle detector)
[3]Flatness ≡ planarity of topography (to support limited stepper depth-of-focus)

3.1 Combining Types

Silicon suppliers, at their option, may combine specifications. This is possible and efficient because most silicon suppliers are currently running only a single process, with the key distinction between various wafer types being the parameters that are measured. One potential specification combination is Furnace+Lithography. Flatness and metal capabilities at the most advanced silicon suppliers are quite good; both these types have the same (relaxed) particle specification. The 180 nm particle specification is very difficult and would be specially sorted by most suppliers. Additionally, heavily doped substrates that contain few COPs for high quality particle wafers are not suitable for furnace or other process testing.

4 SPECIAL PARAMETER CONSIDERATIONS

For these test wafers, a large number of basic parameters (e.g., thickness, crystal orientation) are not controversial, and silicon supplier capability is adequate. Several key parameters normally specified for circuit grade wafers are not as important for test wafers (e.g., interstitial oxygen, resistivity); however, a small set of parameters *is* critical in test wafer specification. Setting the values for these parameters and understanding how to deal with supplier exceptions are very important during early maturity and industry ramp-up.

4.1 Particles and COPs

NOTE: All localized light scatterers (LLS) sizes are given in PSL (polystyrene latex) sphere equivalents.

For I300I test wafers, the particle count specification for all wafer types is 100 particles, chosen as a “reasonable” number to provide particle adder sensitivity for equipment and process testing. The particle size for particle wafers (TW303-180) is the 180 nm target of the SIA Roadmap, namely 90 nm. The particle size for furnace and lithography wafers (TW302-180 and TW304-180, respectively) is approximately the previous (0.25 µm) generation target (120 nm). For the 90 nm particle size, the SIA Roadmap calls for 192 LLSs (including crystal originated pits [COPs]) on polished, circuit grade wafers and 60 real particles on epitaxial, circuit grade wafers (which do not have COPs). The number 100 for particle test wafers was chosen by I300I as an intermediate but high quality LLS capability.

Experience indicates that most routinely grown, lightly doped 300 mm polished wafers will have about 400-600 LLSs, of which less than 100 are real particles, the remainder being stationary crystal defects (i.e., COPs). Silicon suppliers have demonstrated two methods of achieving low LLS counts, namely heavy boron doping (below 10 mΩ-cm) and slowly pulled (much less than 0.5 mm/s) ingots. Both of these techniques have demonstrated fewer than 100 (real) particles @ 120 nm. Silicon suppliers are working to deliver fewer than 100 particles @ 90 nm (specification for 1998), but this capability is not robust or widespread. To control costs, “best effort” below 200 LLSs per wafer may be acceptable for tests that include pre- and post-test particle measurements.

I300I specifies 100 LLSs @ 120 nm for furnace and lithography wafers to ensure high quality for these wafers in 180 nm technology demonstrations. To control costs, “best effort” below 500-600

LLSs per wafer (most of which will be COPs) may be acceptable for non-critical process tests that do not involve particle measurements.

Note that although epitaxial wafers do not have COPs, they are still too expensive to use as particle test wafers.

Scratches are reported by particle detectors by identifying clusters of LLSs (at whatever lower detection threshold is configured) that have a specified minimum size and aspect ratio. There is little definitive understanding of the impact of scratches built up from 90 nm (or even 120 nm) scratches. Silicon suppliers are generally conservative; their recipes for scratch detection should generally be accepted.

I300I member companies are concerned about the cost impact of overspecifying backside particles. Although there is no solid data upon which to build member company consensus, this specification is somewhat relaxed from the previous version and represented as an “expectation,” not a specification, per se. Note that the I300I process and metrology equipment performance metrics call for fewer than 200 added particles per wafer pass on the backside.

4.1.1 FLATNESS

Because I300I will be using a 300 mm full-field DUV stepper for 1998 patterning, the specification of wafer flatness is critical for any patterned wafer testing. Pattern CDs as small as 180 nm (lines) and 200 nm (contacts) will be printed using various, lithographic enhancement techniques. A standard industry guideline is that the site flatness distribution on wafers (reported as SFQR; see SEMI M1 for definitions) should be below the CD (180 nm).

The I300I full-field stepper uses 25 mm x 25 mm fields; therefore, wafers for I300I demonstrations should be specified using that site size. Although I300I will print fields at the edge of the wafer (partial sites), wafers should be specified using the “Max Full” site layout with partial sites reported. Note that some metrology equipment is not capable of reporting more than one site layout per measurement and asking for multiple specifications from a supplier is a significant cost adder (lower sampling, process capability data is a better alternative).

The SIA Roadmap indicates the use of scanning steppers with a field size of 32 mm x 25 mm for 180 nm technology. Since I300I will not be using a scanning stepper for demonstration patterning in 1998, it will not specify at this site dimension for demonstration wafers. I300I *will*, however, be characterizing silicon suppliers relative to this industry target later in 1998 (using the “Max Partial” site layout). The final SEMI standards definitions for a scanning stepper flatness measurement (SFSR) will be completed in early 1998.

NOTE 1. The site pattern offsets used in this specification have been updated to function according to the ad hoc standard of ADE flatness measurement tools.

NOTE 2. The electronic version of this document (Microsoft Excel 5.0) contains a working site layout system. Contact I300I for information.

4.2 Wafer ID Mark

4.2.1 ALPHANUMERIC MARK

Formerly, the I300I-specified wafer ID mark was a modified SEMI M12 mark, including a special code letter indicating the I300I wafer type. Although the basic mark is being retained, the special code letter is being eliminated. In addition to being non-standard, the special code was not economical. This is because the wafer ID must be applied very early in the wafer manufacturing process, thus committing each wafer to a certain final wafer classification long before the quality of that particular wafer is established. Sorting and other product redirection strategies are required to compensate for processes variations.

Wafer ID marking is still required, but the content is as specified in SEMI M12, i.e., a universally unique, supplier sequence number. The following is a brief description of the SEMI M12-type mark:

- 10 message characters + 2 checksum characters
  - Positions 1–5 (alphanumeric) are supplier lot ID
  - Position 6 (alphanumeric) and 7–8 (numeric) are supplier lot sequence number
  - Position 9–10 (alpha) are SEMI initials for supplier
  - Position 11–12 are SEMI M12 checksum

The M12 mark is placed according to (now defunct) SEMI M28-96 (frontside of wafer; left of notch [notch downward]; character baseline towards wafer edge). Note that mark exclusions for this location must be implemented for both particle and flatness measurements.

4.2.2 2-D DOT MATRIX MARK

To support a universal standard for silicon supplier wafer traceability, I300I member companies are supporting the mandatory use of the SEMI T7 along with any other user-specified mark. The T7 mark, currently an option in the SEMI M1.15 300 mm prime wafer standard, is a backside dot matrix coded mark. The mark, just under 1 mm x 4 mm in size, is located 5° counterclockwise from the notch, within the backside edge exclusion. The I300I member company guideline is that any other mark should have the same content as the T7 mark on the back.

Note that the SEMI specification does not yet mandate the T7 mark; I300I is only recommending—strongly—that suppliers begin to incorporate this mark into their production capability.

5 STATISTICAL SPECIFICATION

For I300I deliveries, values shall be 100% guaranteed, unless otherwise noted or negotiated. If statistically significant manufacturing capability data is available (usually in the form of parameter distributions, i.e., histograms), then a 99% distribution conformance level (or other negotiated level) of risk will be accepted by I300I (normal, log-normal, or other distribution shape must be negotiated on a parameter basis). When reporting sample/typical values is requested (as noted by “(R)” in the specification), the sampling plan and test method (including measurement equipment supplier and model) must be identified.

6 I300I CONTACTS

Randy Goodall
Associate Director of Productivity and Infrastructure
randy.goodall@i300i.org
(512) 356-7622 PHONE
(512) 356-3070 FAX

Chi Au
Silicon Program Manager
chi.au@i300i.org
(512) 356-7531 PHONE
(512) 356-3070 FAX

Laura Matkin
Administrative Assistant
laura.matkin@i300i.org
(512) 356-3232 PHONE
(512) 356-3305 FAX

7 180 nm I300I SPECIFICATIONS

I300I Designation			TW301-180	TW302-180	TW303-180	TW304-180	
Item		Standard	Mechanical Wafer	Furnace Wafer	Particle Wafer	Lithography Wafers	Test Wafer Comments
Per SEMI M18; missing = "NS"		Unless otherwise noted, all specs are SEMI M28-97; Any exception to indicated standard is shaded; "(R)" = Report sampled/typical value; "NS" = Not Specified; NTRS = 1997 SIA Roadmap					
1. General Characteristics							
1.1	Growth Method		Cz or MCz	Cz or MCz	Low COP crystal	Cz or MCz	Supplier Option
1.2	Crystal Orientation	M1	{100} ± 1°	{100} ± 1°	{100} ± 1°	{100} ± 1°	
1.3	Conductivity type		p	p	p	p	
1.4	Dopant		Boron	Boron	Boron	Boron	
1.5	Nominal Edge Exclusion	NTRS	2 mm	2 mm	2 mm	2 mm	
2. Electrical Characteristics							
2.1.1	Resistivity (Nominal)		NS	15 Ω-cm	NS	NS	Center Point
2.1.2	Resistivity (Tolerance)		NS	10 Ω-cm	NS	NS	Center Point
2.2	Radial Resistivity Variation (RRG)		NS	< 10%	NS	NS	Within wafer variation
2.3	Resistivity Striations		NS	NS	NS	NS	
2.4	Minority Carrier Recombination Lifetime	NTRS	NS	NS	NS	NS	
3. Chemical Characteristics							
3.1.1	Oxygen Concentration (Nominal)	ASTM-79	(R)	(R)	(R)	(R)	Spec ≤ 24 for contamination tests (no internal gettering) OR ≥ 30 for precipitation testing
3.1.2	Oxygen Concentration (Tolerance)	ASTM-79	NS	(R)	NS	NS	Within shipment variation
3.2	Radial Oxygen Variation		NS	≤ 10% (R) 5 mm from Edge	NS	NS	
3.3	Carbon Concentration		NS	≤ 0.2 ppma	NS	NS	
3.X	Total Bulk Fe	NTRS	NS	$\leq 1 \times 10^{10}/cm^3$	NS	NS	Supplier to state test method

I300I Designation			TW301-180	TW302-180	TW303-180	TW304-180	
Item		Standard	Mechanical Wafer	Furnace Wafer	Particle Wafer	Lithography Wafers	Test Wafer Comments
Per SEMI M18; missing = "NS"		Unless otherwise noted, all specs are SEMI M28-97; Any exception to indicated standard is shaded; "(R)" = Report sampled/typical value; "NS" = Not Specified; NTRS = 1997 SIA Roadmap					
4. Structural Characteristics							
4.1	Dislocation Etch Pit Density		NS	≤ 250/cm^2 (R)	NS	NS	
4.2	Slip		NS	none	none	none	
4.3	Lineage		NS	none	none	none	
4.4	Twin		NS	none	none	none	
4.5	Swirl		NS	none	none	none	
4.6	Shallow pits		NS	none	none	none	
4.7	Oxidation-Induced Stacking Faults (OSF)	NTRS	NS	(R)	NS	NS	May be difficult to control OISF and LLSs at 0.12 µm due to crystal growth issues. Negotiate based on most critical need. OISF is often harmless for equipment demo
4.8	Oxide Precipitates (BMD) O_i Reduction (ΔO_i)		NS	(R)	NS	NS	Test (R) with 0.18 µm I300I front-end thermal cycle
5. Wafer Preparation Characteristics							
5.1	Wafer ID Marking	M28-96 M1, M12	Frontside OCR	Frontside OCR	Frontside OCR	Frontside OCR	NOTE: T7 Laser ID Mark on backsurface near notch is recommended
5.2	Front Surface Thin Film(s)		NS	NS	NS	NS	
5.3	Denuded Zone		NS	NS	NS	NS	
5.4	Extrinsic Gettering Treatment		NS	none	none	none	
5.5	Backseal		NS	NS	NS	NS	
5.6	Annealing		NS	Donor annihilation permitted. RTP preferred (R)	Donor annihilation permitted. RTP preferred (R)	Donor annihilation permitted. RTP preferred (R)	Alternate Anneals Require User/Supplier Mutual Agreement

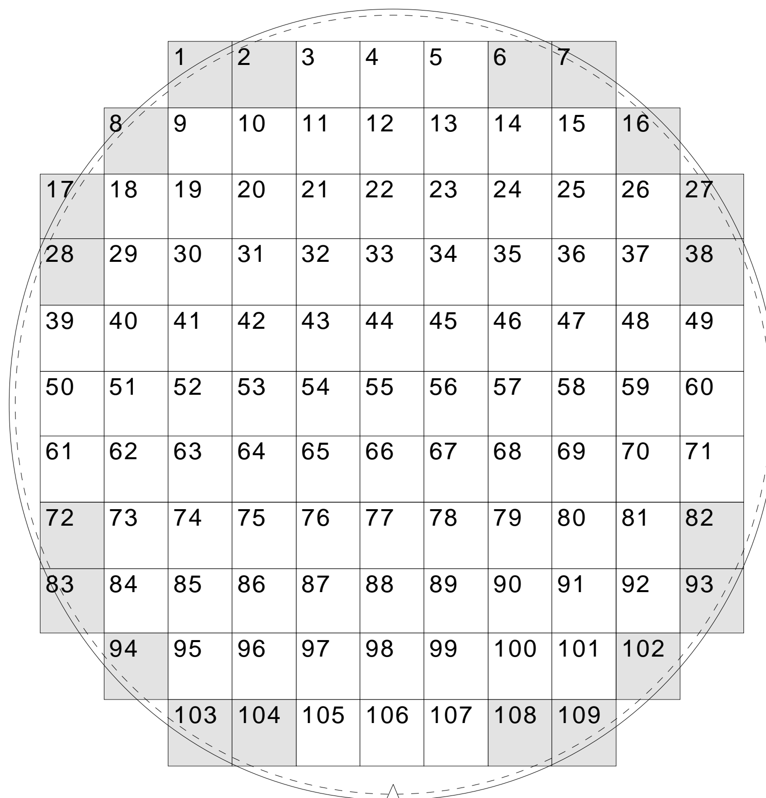
I300I Designation			TW301-180	TW302-180	TW303-180	TW304-180	
Item		Standard	Mechanical Wafer	Furnace Wafer	Particle Wafer	Lithography Wafers	Test Wafer Comments
Per SEMI M18; missing = "NS"		Unless otherwise noted, all specs are SEMI M28-97; Any exception to indicated standard is shaded; "(R)" = Report sampled/typical value; "NS" = Not Specified; NTRS = 1997 SIA Roadmap					
6. Mechanical Characteristics							
6.1	Diameter	M1	300 ± 0.2 mm	300 ± 0.2 mm	300 ± 0.2 mm	300 ± 0.2 mm	
6.2	Diameter Notch Dimensions	M1					
6.2.1	Notch Depth	M1	1 +0.25,-0.00 mm	1 +0.25,-0.00 mm	1 +0.25,-0.00 mm	1 +0.25,-0.00 mm	
6.2.2	Notch Angle	M1	90 +5,-1 degrees	90 +5,-1 degrees	90 +5,-1 degrees	90 +5,-1 degrees	
6.3	Notch Orientation	M1	<110> ± 1°	<110> ± 1°	<110> ± 1°	<110> ± 1°	
6.6.1	Edge Profile		C_y = 194 µm, A_x = 120 µm, D_y = 50 µm	C_y = 194 µm, A_x = 120 µm, D_y = 50 µm	C_y = 194 µm, A_x = 120 µm, D_y = 50 µm	C_y = 194 µm, A_x = 120 µm, D_y = 50 µm	"blunt edge"
6.6.2	Edge Surface Finish	M1	Polished	Polished	Polished	Polished	Identify test measurement method
6.7	Thickness	M1	775 ± 25 µm	775 ± 25 µm	775 ± 25 µm	775 ± 25 µm	
6.7.1	Thickness Variation (9-Point TTV)	M1	≤ 10 µm	≤ 10 µm	≤ 10 µm	NS	
6.72	Thickness Variation (GBIR)		NS	NS	NS	£ 3 µm	Full Scan
6.9	Surface Orientation	(see 1.2)					
6.10	Bow		NS	NS	NS	NS	
6.11	Warp	M28-97	≤ 100 µm	≤ 100 µm	≤ 100 µm	≤ 50 µm	
6.12	Sori		NS	NS	NS	NS	
6.13	Flatness/Global		NS	NS	NS	NS	
6.14A	Flatness/Site (for lithography tests)		NS	NS	NS	SFQR ≤ 0.18 µm SFSR (R)	32 mm x 25 mm, Max. Full Sites (see figure); Partial sites NOT included.
6.14B	Flatness/Site (for wafer characterization)		NS	NS	NS	SFQR ≤ 0.18 µm SFSR (R)	32 mm x 25 mm, Max. Partial Sites (see figure); Partial sites included

I300I Designation		Standard	TW301-180 Mechanical Wafer	TW302-180 Furnace Wafer	TW303-180 Particle Wafer	TW304-180 Lithography Wafers	Test Wafer Comments
Item							
Per SEMI M18; missing = "NS"		Unless otherwise noted, all specs are SEMI M28-97; Any exception to indicated standard is shaded; "(R)" = Report sampled/typical value; "NS" = Not Specified; NTRS = 1997 SIA Roadmap					
6.14C	Flatness/Site (for full field stepper)		NS	NS	NS	SFQR ≤ 0.18 µm (Report 6.14A and 6.14B process capability, including SFSR)	25 mm x 25 mm, Max Full Sites (see figure); Partial sites included. This will support early 1998 full-field stepper usage.
7. Front Surface Chemistry							
7.1	Surface Metal Contamination						
	Sodium	NTRS	NS	≤ $1.3 \times 10^{10}/cm^2$	NS	NS	
	Aluminum	NTRS	NS	≤ $1 \times 10^{11}/cm^2$	NS	NS	
	Potassium	NTRS	NS	≤ $1.3 \times 10^{10}/cm^2$	NS	NS	
	Chromium	NTRS	NS	≤ $1.3 \times 10^{10}/cm^2$	NS	NS	
	Iron	NTRS	NS	≤ $1.3 \times 10^{10}/cm^2$	NS	NS	
	Nickel	NTRS	NS	≤ $1.3 \times 10^{10}/cm^2$	NS	NS	
	Copper	NTRS	NS	≤ $1.3 \times 10^{10}/cm^2$	NS	NS	
	Zinc	NTRS	NS	≤ $1 \times 10^{11}/cm^2$	NS	NS	
	Calcium	NTRS	NS	≤ $1.3 \times 10^{10}/cm^2$	NS	NS	
7.2	Surface Organics (Polymer carbon atoms)	NTRS	NS	NS	NS	NS	
8. Front Surface Criteria							
8.1A	Scratches (macro)		NS	none	none	none	Tencor SP-1 Wide and Narrow channels with sensitivity at relevant particle size
8.1B	Scratches (micro)		NS	≤ 10 mm (total length)	≤ 10 mm (total length)	≤ 10 mm (total length)	(see 8.1A)
8.2	Pits (COPs)	NTRS	NS	NS	(R)	NS	Reporting (R) requires advanced measurement/analysis techniques

I300I Designation			**TW301-180**	**TW302-180**	**TW303-180**	**TW304-180**	
	Item	**Standard**	**Mechanical Wafer**	**Furnace Wafer**	**Particle Wafer**	**Lithography Wafers**	**Test Wafer Comments**
Per SEMI M18; missing = "NS"		Unless otherwise noted, all specs are SEMI M28-97; Any exception to indicated standard is shaded; "(R)" = Report sampled/typical value; "NS" = Not Specified; NTRS = 1997 SIA Roadmap					
8.3	Haze		NS	NS	Goal < 0.03ppm	NS	Tencor SP-1 Wide channel (or technical equivalent)
8.4	Localized Light Scatterers – Only particles for epitaxial wafers – Sizes are PSL equivalents	NTRS	NS	≤ 100 @ ≥ 0.12 µm (Supports non-critical particle monitoring)	≤ 100 @ ≥ 0.09 µm	≤ 100 @ ≥ 0.12 µm (Supports non-critical particle monitoring)	Tencor SP-1 Wide channel (or technical equivalent)
8.6	Edge Chips		NS	none	none	none	
8.7–8.16	Other		NS	NS	NS	NS	
9. Back Surface Criteria							
9.1	Edge Chips		NS	none	≤ 3	≤ 3	
9.2-9.5	OTHER		NS	NS	NS	NS	
9.6	Roughness		NS	NS	NS	NS	
9.7	Brightness (Gloss) NOTE: Double-side polish process preferred		≥80%	≥ 80%	≥ 80%	≥ 80%	60° angle of incidence, referenced to a mirror polished silicon wafer.
9.X	Localized Light Scatterers		NS	NS expect ≤ 500 @ ≥ 0.25 µm PSE	NS expect ≤ 500 @ ≥ 0.25 µm PSE	NS expect ≤ 500 @ ≥ 0.25 µm PSE	Report characterization method and level with and without final particle detection
9.YA	Scratches (Macro)		NS	none (5 macro "extended/ area defects" allowed for harmless effects, e.g., organics, non-damage equip. chuck marks)			Visual Inspection
9.YB	Scratches (Micro)		NS	≤ 25 mm (total length)	≤ 25 mm (total length)	≤ 25 mm (total length)	Visual Inspection

8 SITES 25 x 25 MAX. FULL

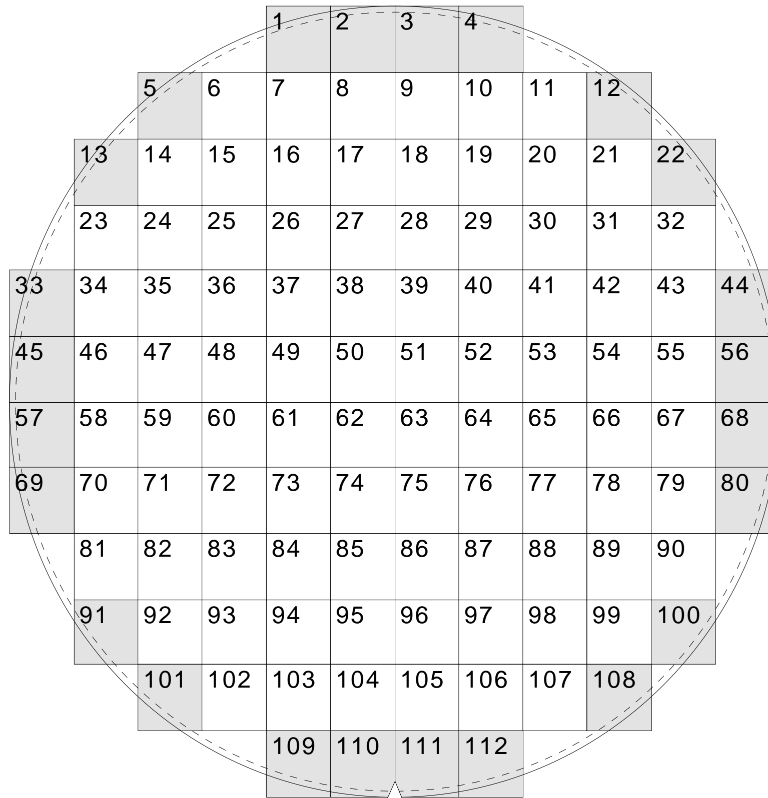
Diameter	300
xSize	25
ySize	25
xOffset	12.5
yOffset	12.5
EdgeXcl	2



Full	Partial	Total	%FQA Full
89	20	109	80.83

9 SITES 25 x 25 MAX. PARTIAL

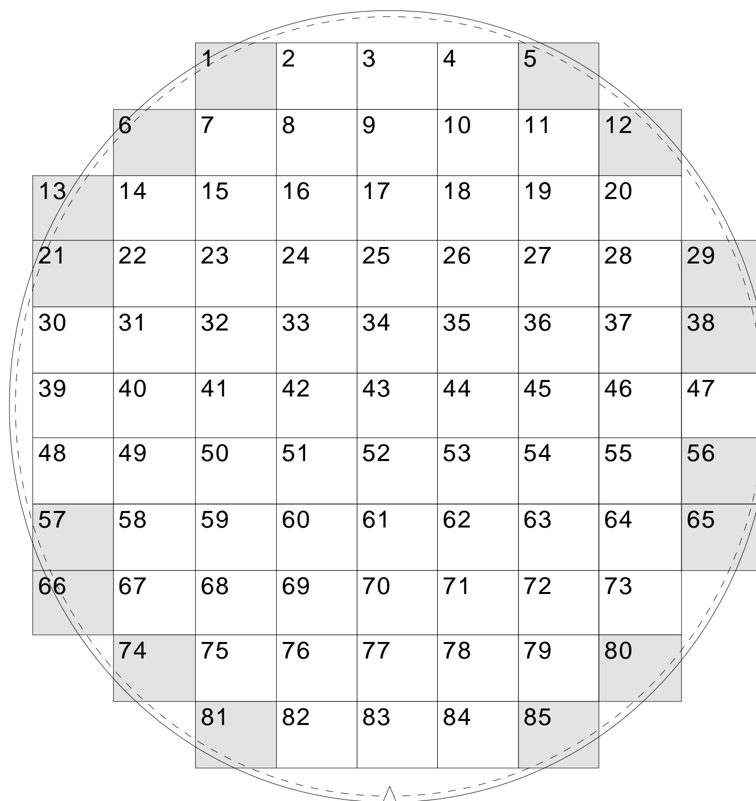
Diameter	300
xSize	25
ySize	25
xOffset	0
yOffset	0
EdgeXcl	2



Full	Partial	Total	%FQA Full
88	24	112	79.93

10 SITES 32 x 25 MAX. FULL

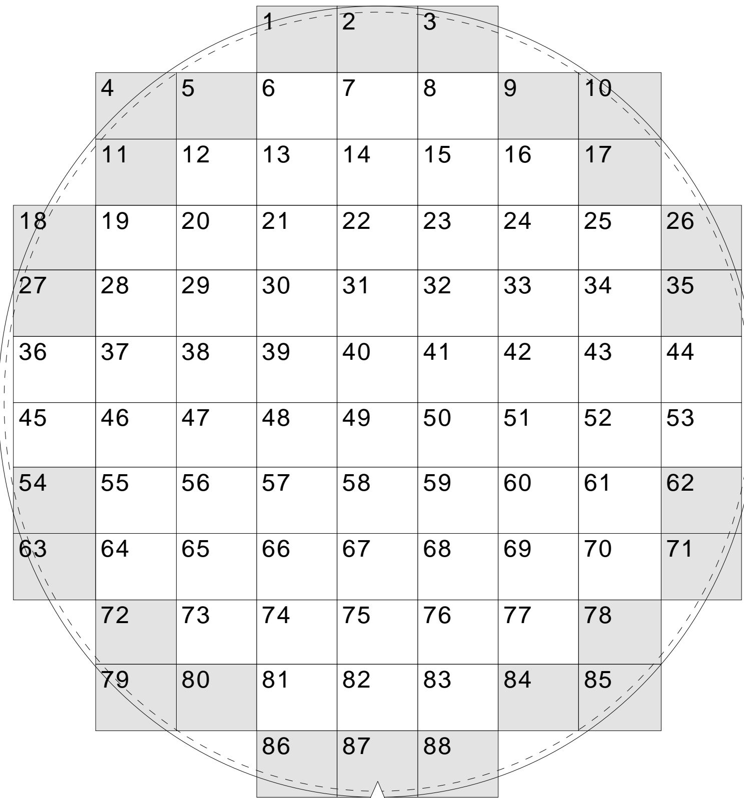
Diameter	300
xSize	32
ySize	25
xOffset	-13
yOffset	12.5
EdgeXcl	2



Full	Partial	Total	%FQA Full
69	16	85	80.22

11 SITES 32 x 25 MAX. PARTIAL

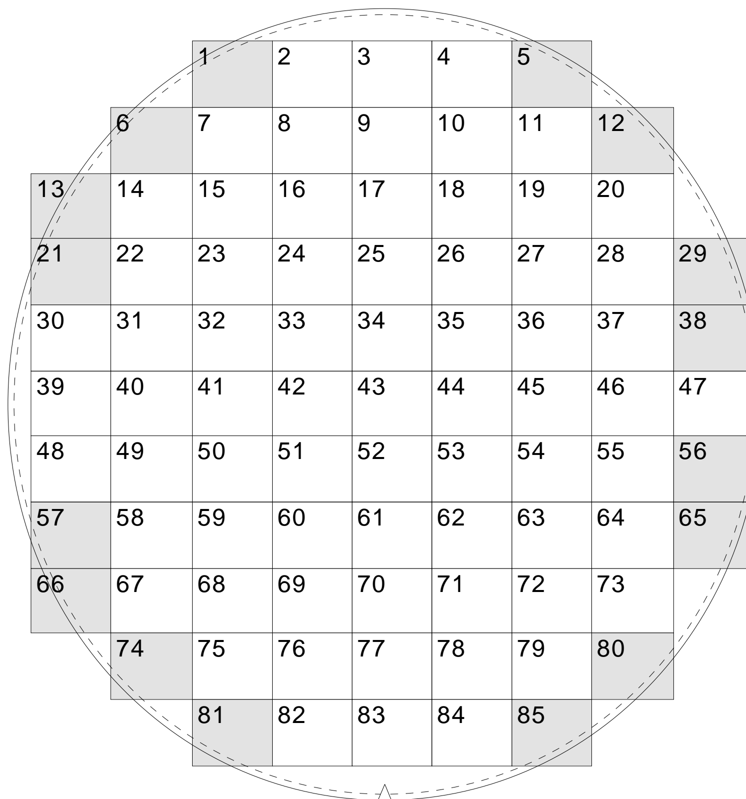
Diameter	300
xSize	32
ySize	25
xOffset	16
yOffset	0
EdgeXcl	2



Full	Partial	Total	%FQA Full
62	26	88	72.08

12 TEST SITE PATTERNS

Diamete	300
xSize	32
ySize	25
xOffset	-13
yOffset	12.5
EdgeXcl	2



Full	Partial	Total	%FQA Full
69	16	85	80.22

International SEMATECH Technology Transfer
2706 Montopolis Drive
Austin, TX 78741

http://www.sematech.org
e-mail: info@sematech.org