2.5D and 3D Semiconductor Package Technology: Evolution and Innovation

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Abstract
The electronics industry is experiencing a renaissance in semiconductor package technology. A growing number of innovative 3D package assembly methodologies have evolved to enable the electronics industry to maximize their products functionality. By integrating multiple die elements within a single package outline, product boards can be made significantly smaller than their forerunners and the shorter interconnect resulting from this effort has contributed to improving both electrical performance and functional capability. Multiple die packaging commonly utilizes some form of substrate interposer as a base. Assembly of semiconductor die onto a substrate is essentially the same as those used for standard I/C packaging in lead frames; however, substrate based IC packaging for 3D applications can adopt a wider range of materials and there are several alternative processes that may be used in their assembly. Companies that have already implemented some form of 3D package technology have found success in both stacked die and stacked package technology but these package methodologies cannot always meet the complexities of the newer generation of large-scale multiple function processors.

A number of new semiconductor families are emerging that demand greater interconnect densities than possible with traditional organic substrate fabrication technology. Two alternative base materials have already evolved as more suitable for both current and future, very high-density package interposer applications; silicon and glass. Both materials, however, require adopting unique via formation and metallization methodologies. While the infrastructure for supplying the glass-based interposer is currently in development by a number of organizations, the silicon-based interposer supply infrastructure is already well established.

This paper outlines both positive and negative aspects of current 3D package innovations and addresses the challenges facing adopters of silicon and glass based interposer fabrication. The material presented will also reference 3D packaging standards and recognize innovative technologies from a number of industry sources, roadmaps and market forecasts.

Key words: 2.5D, 3D Semiconductor Package Technology, Through Silicon Via, TSV, Through Glass Via, TGV

Introduction
A majority of the semiconductor die elements continue to be designed with bond sites at the perimeter edge. For a wide range of applications, both single and multiple die-stack package assembly processes will likely continue to employ conventional face-up die attach and wire-bond methodology. The use of wire-bond interconnect as the exclusive means of termination, however, is somewhat restrictive because it requires significant surface area to accommodate the die-to-interposer wire-bond process. In regard to die-stack package assembly, managing the layout of several hundred interconnects and their wire-loop profile restrictions will entail a great deal of planning.

Even though a great deal of progress has been made in process refinement and system development, methodologies will vary a great deal. To ensure a strong infrastructure for 2.5D and 3D applications the industry will need a degree of harmonization and standardization. There are a number of multiple die package issues that will need to be resolved, including;

- Selection of suitable component functions for multiple die packaging
- Establish a reliable source for semiconductor elements
- Specify physical and environmental operating conditions
- Define package design constraints and understand process protocols
- Stipulate electrical test method and post assembly inspection criteria

3D Semiconductor Package Innovations
Within the current decade the industry has developed an impressive family of multiple die solutions. A majority of the innovations utilized the existing package manufacturing infrastructure while others require the development of specialized materials and process systems. The organic interposer base will likely remain popular for a significant number of multiple die applications. To enable more efficient processing of multiple die sets, the substrates are furnished in a panel or strip format. In regard to assembly, when stacking two or more semiconductors onto a single interposer substrate for wire-bond assembly, the die elements will ideally have a progressively smaller outline. This tiered or pyramid die format has been very successful, generally furnishing the lowest overall multiple die package profile.
In this configuration, each die element is sequentially attached on top of one another. The progressively smaller die outline leaves the edge of all die elements accessible for wire-bond processing in a single operation (**Figure 1**).

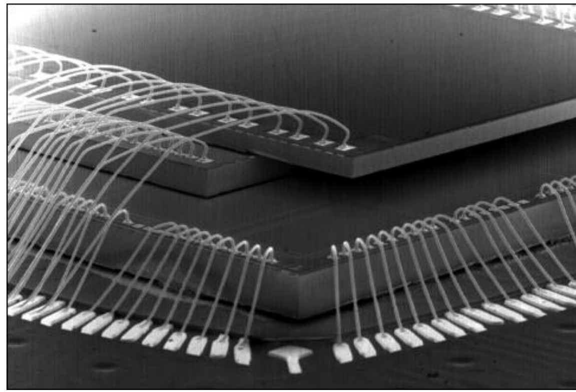

Figure 1. Three-die, wire-bond semiconductor assembly
(Example Source: Intel Corporation)

Following molding operations, alloy ball contacts are commonly applied in the now familiar array format on the opposite surface of the interposer to accommodate electrical test and the eventual mounting of the finished package on the next level assembly. Because these heterogeneous die elements are mounted onto a single high-density interposer structure, the primary signal paths can be very short, contributing to increasing operating speed and power reduction. Although multiple die package technology has reached a level of maturity, package assembly yield may be adversely impacted when one or more die in the stack do not perform to their expected level or fail altogether.

When die elements have the same outline or nearly the same outline, thin silicon spacers are added between die elements to accommodate wire-bond loop heights. The example furnished in **Figure 2** represents a stacked die assembly using a number of semiconductor die elements having the same outlines.

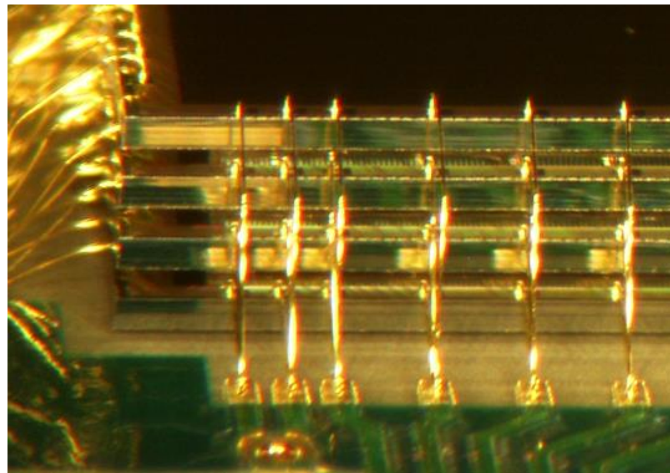

Figure 2. Same size die stack using spacers
(Example Source: Dimation)

Excessive overall package height can be a critical roadblock for a number of personal hand-held product applications. For example, same size die elements generally represent memory functions. Unlike the tiered die assembly noted above, the memory die-stack process is less efficient. Although all memory die elements are assembled onto a common interposer base, die-attach and wire-bond operations for each die element must be completed before progressing to the next level. Even though the die elements can be made very thin, the accumulated stack-up height generated by the added spacer and wire-bond loop profile may not meet all package profile requirements.

3D Package-on-Package Solutions for Heterogeneous Applications
Combining the memory and logic functions in a single package outline has often compromised both test efficiency and overall package assembly yield. Vertically mounting one or more pre-packaged die elements (package-on-package) has evolved as a preferred alternative to die stacking, especially for applications requiring multiple heterogeneous semiconductor elements and, separating dissimilar logic and memory functions has proved to be very efficient. The logic die element often have a significantly larger outline and a greater number of I/O than the memory elements. For this reason, the base or lower package section will typically accommodate the logic while the memory functions associated with the logic die will be

deployed to the upper section of the package. Additionally, the package sections may utilize both wire-bond and flip-chip assembly methodologies. The flip-chip assembly will enable significant in-package interconnect capability and provide a very low package profile for the bottom section. This design illustrated in **Figure 3** allows the mold material to extend out to the edge of the interposer on the lower section to minimize package warp and utilizes a through-mold-via (TMV) enabling smaller and closer pitch contact features between the upper and lower section.

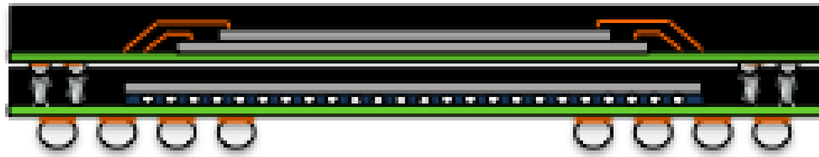

Figure 3. Package-on-Package (PoP)
(Example source: IPC-7091)

Even though two substrate interposers are required for the PoP application, the joining of individually tested package sections have proved more economical.

Many of the more advanced 3D package solutions involved a great deal of engineering resources before they were made available for volume manufacturing and, although widely available, some variations will require licensing agreements with the developer before use.

Bond Via Array PoP

To overcome the limiting aspects of the more traditional PoP assembly method shown above, an alternative high-density substrate interconnect solution has evolved. The bond via array process enables a substantial reduction in interface contact pitch between the lower and upper package sections. The main feature of the bond via array concept is the use of commercially available organic based substrate materials and conventional wire-bond systems to furnish the closely spaced narrow copper-post contacts that provide electrical interface between upper and lower package sections. The detail shown in **Figure 4** illustrates the upper and lower sections of the bond via array package.

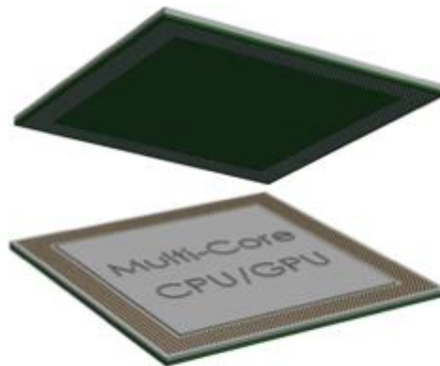

Figure 4. 14.0mm x 14.0mm, 1000 I/O, 240µm pitch Bond Via Array Package-on-Package
(Source: Invensas Corporation)

Following die mounting and wire-bond post formation the Bond Via Array substrate is fully encased, physically reinforcing the thin Cu posts within the mold compound that encapsulates the lower package semiconductor. The reduced contact pitch made possible with the process easily accommodates a much higher number of interconnects in the PoP perimeter stacking arrangement. This interconnect technology lends itself to a wide variety of 3D packaging, including multiple-rows and area array, fan-in or fan-out array, and flat or step mold design. Furthermore, the Bond Via Array technology utilizes the existing wire-bond assembly infrastructure to enable high density, vertical profile interconnects and the length of the Cu wire can be extended to a precise elevation to accommodate differing variations of upper and lower package profiles. The developer of this Bond Via Array PoP assembly states that the process has the potential for providing a contact pitch as small as 100µm, significantly closer pitch than currently possible with solder ball configured PoP technology.

The Cu wire contact extends from the top surface of the lower substrate to align with matching solder bump contact locations on the bottom surface of the upper package section (**Figure 5**). Furthermore, the close coupling between the package sections also contributes to managing power.

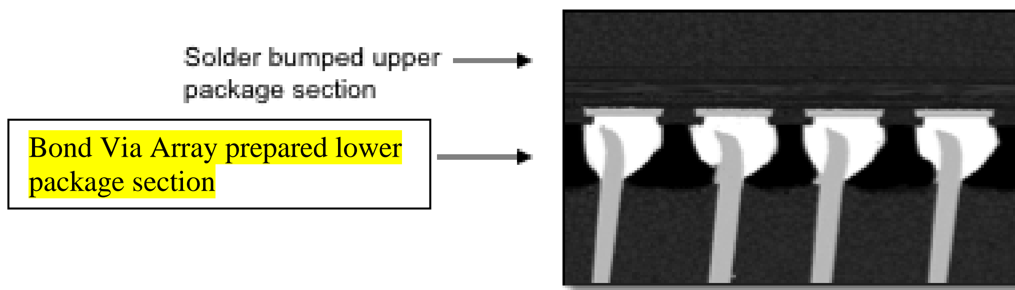

Figure 5. Bond Via Array, Ultra Fine Pitch Copper Post Interconnect
(Source: Invensas Corporation)

Evolving 2.5D Interposer Technology
New semiconductor families are emerging that demand greater interconnect densities than possible with today's organic substrate fabrication technology. Two alternative base materials have already proved to be more suitable for the both current and future very high-density package applications. The two base materials with the physical attributes considered most capable for the very high-density interposers are silicon and glass. Both materials, however, require adopting unique via formation and metallization methodologies to enable the interface between one side of the interposer to the other. The term 'through-silicon-via' (TSV) is applied to miniature ablated and plated via features in the silicon-based interposer. Likewise, furnishing similar features on the glass-based interposer is referred to as Though-Glass-Via (TGV). While the infrastructure for supplying the glass-based interposer is progressing, the silicon-based interposer supply infrastructure is already well established.

Silicon Interposer Fabrication
A great deal of resources have already been invested to bring TSV into a viable interconnect solution for both 2.5D interposers and 3D stacked-die assembly. In preparation for TSV, small diameter holes are first formed on one side of the silicon wafer. The most common process for this operation uses a deep reactive-ion etching (DRIE) process The via ablation process is also known as 'pulsed' or 'time-multiplexed' etching, a process that alternates repeatedly between two modes to achieve nearly vertical hole structures. During the pulsed etching process a passivation layer is naturally formed onto the vias sidewall to block further chemical attack and to prevent additional etching within the via sidewall. These etch/deposit steps are repeated until the ablation reaches the desired depth (**Figure 6**).

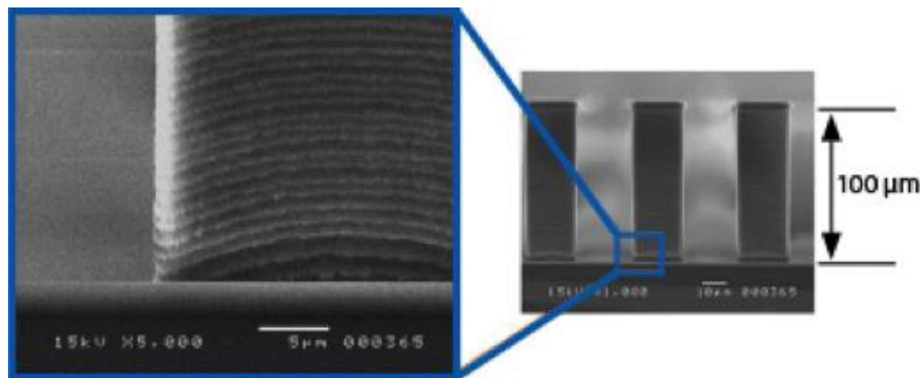

Figure 6. Via formation using deep reactive-ion etching (DRIE) process
(Example source: SAMCO Systems)

Although it is possible to etch via holes all the way through the silicon base, it is common practice to stop the etching process at a predetermined depth that will better promote via filling during the metalization process.

In preparation for via filling a seed layer of copper or tungsten is first applied to enable electroplating the additional copper required to complete the via fill operation. Electroplating is commonly employed for via sizes that range between 5µm and 20µm. To finally access the metallized Cu filled vias on the opposite surface of the wafer, a combination of grinding and/or plasma etching processes are utilized. Further pattern plating processes are finally employed to provide surface interconnect features as illustrated in **Figure 7**.

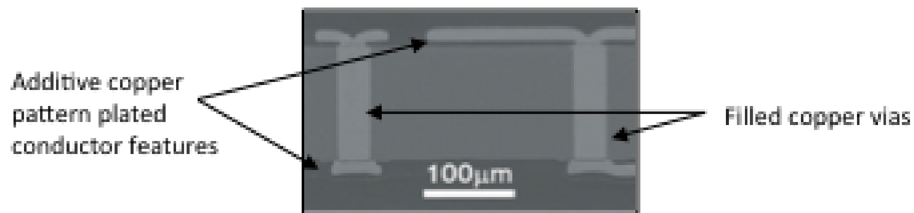

Figure 7. Copper filled TSV interface between the interposers top and bottom surface
(Example source: STATSChipPac)

Because of its low resistivity and conductive characteristics, copper (Cu) has become the favored alloy for interposer via and circuit plating. In preparation for forming the Cu component termination sites (land patterns) and conductors on the silicon wafer surface, the fabricator will first sputter a metal alloy adhesion layer on the wafers surface. Adhesion-promoting metals include: nickel (Ni), molybdenum (Mo), chromium (Cr), tungsten (W), and titanium (Ti). These base materials are then over-plated with a more conductive metal such copper, gold, tin and palladium. Following the pattern plating the remaining thin adhesion layer is chemically etched from the silicon wafer surface followed by the application of a photo-imaged passivation layer to insulate and protect the remaining conductive circuit pattern.

Glass Interposer Fabrication

Glass is gaining momentum for interposer applications because it has a lower dielectric loss than silicon and its cost is significantly less than silicon. Glass differs from silicon wafers because glass thickness, panel size and shape (round, square or rectangular) offer more process variations than silicon wafers. Regarding panel shape, panels up to 500 mm x 500 mm can be furnished with the potential for utilizing board level assembly systems for die placement.

Methods for forming TGVs including laser (CO_2, Excimer, UV), electrostatic discharge, mechanical drilling, chemical etching and may include a combination of these processes. For mechanical drilling, a micro-sandblasting method is commonly utilized as well. In general, 10µm is considered to be the minimum diameter for TGVs, but, based on ablation methods and system settings, vias can be made larger if needed.

Several methods are available for metalizing glass including copper alloy plating, silver and copper pastes, silver and copper inks. To achieve better adhesion between metal and glass, surface treatments and/or some interfacial layers are employed and unlike silicon, glass is a natural insulating material and does not require a barrier layer application prior to plating (**Figure 8**).

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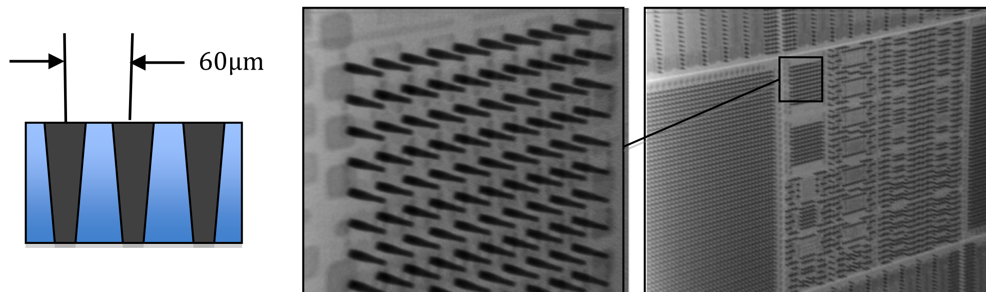

Figure 8. Metallized TGV X-ray Images
(Example source: Dai Nippon Printing)

3D System Level Package Technology

The fundamental driver for those involved in system level package development is to increase product functionality and performance without increasing product size. Industry analysts are forecasting that, *"even though mobile electronics markets will continue to see significant growth, the telecom market demand is widening as well"*. Developers of smart phones and tablet products are already adopting multi-core processors and experiencing greater memory-to-processor bandwidth. Manufacturers, however, are continually developing semiconductors with significantly expanded and faster process capability. These new generations of multicore processors have much higher I/O than their predecessors and the die elements outline to I/O ratio is significantly smaller. Although the die elements can be furnished with a uniform array contact pattern, the contact pitch of the array is far too narrow for mounting onto a conventional organic based interposer. The current solution for interconnecting these new generations of high-density, very fine-pitch die elements is the silicon-based interposer. The silicon interposer circuit routing enables very close coupling between related die elements, thereby minimizing the interface requirements and broadening the contact pitch between the interposer and organic based package substrate. The

contact features located on the individual die elements may have a pitch as small as 30µm to 50µm, while the contacts on the bottom surface of the Si interposer are ‘fanned out’ to a wider 150µm to 200µm pitch. The illustration shown in **Figure 9** is typical of silicon or glass interposer enabled 3D system level product with related but heterogeneous semiconductor die elements.

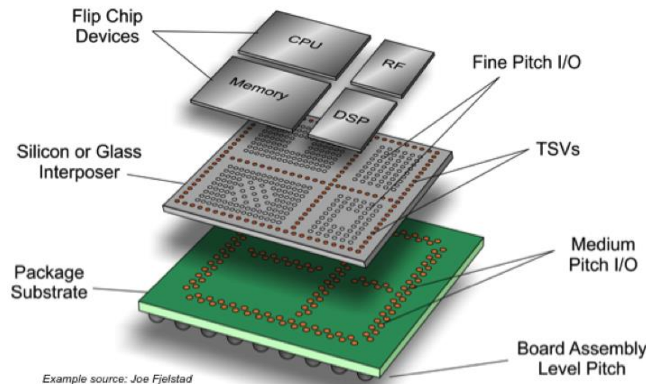

Figure 9. General elements of a 3D system level package
(Illustration courtesy of Joseph Fjelstad)

The wider pitch contact pattern on the bottom surface of the Si-based interposer will better accommodate solder ball or solder bump contacts for reflow solder attachment to the top surface of the organic based package substrate.

Three accepted methodologies for joining high-density semiconductors to the silicon-based interposer include 1) solder reflow processing, 2) thermo-compression bonding and 3) annealed copper bond interconnect (**Figure 10**).

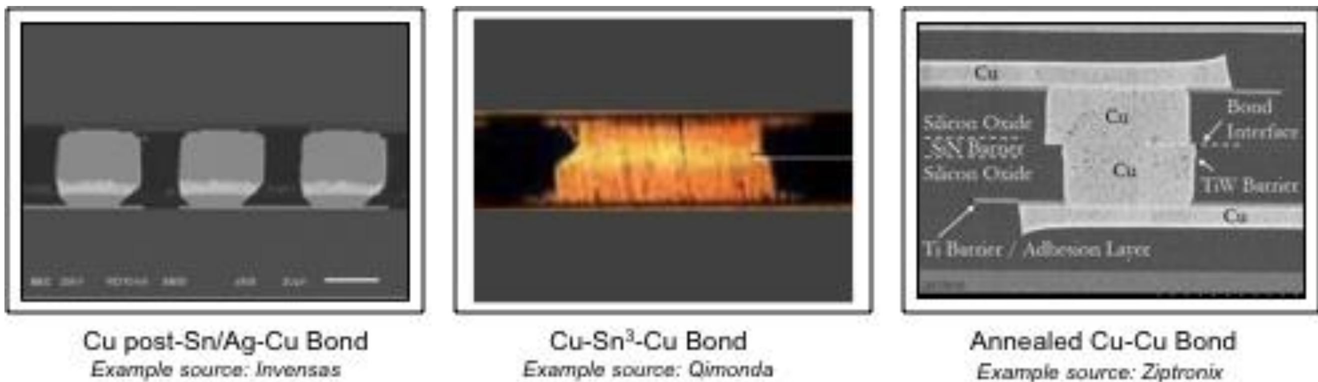

Figure 10. Die-to-interposer attach variations

Reflow soldering- The contact furnished for the very fine-pitch die-to-interpose attachment process is a ‘solder capped’ copper post or micro-bump contact. Key solder process issues include optimizing reflow temperature profiles, flux activation and time above liquidus (TAL). Because the standoff dimension between die and interposer surface can be 50 microns or more, underfill is commonly specified to reinforce the site. Flux selection can also be a factor. Any remaining flux residue that accumulates on the interposer surface during the solder process can promote excessive voids in the underfill.

Thermo-Compression Bond (Cu/Sn/Cu Fusion)- A two-stage procedure that begins with the initial precise alignment and room temperature pre-bonding of the die element to the interposer wafer. Following pre-bond, the interposer is exposed to an annealing process that includes high temperature and pressure. This joining process is significantly enhanced with the deposition of a thin layer of tin-alloy onto the exposed copper contact features. When the wafer interposer is heated to approximately 400°C, the tin alloy layer completely diffuses into the apposing copper contact features to form a stable Cu-Sn- Cu (Cu3Sn) intermetallic.

Low Temperature Hybrid Bond Technology- A heterogeneous or hybrid joining process furnishing an In-Situ electrical interface with patterned metal alloy contact surfaces and silicon oxide dielectric (e.g., Cu/SiO-Cu/SiO, Cu/SiN-Cu/SiN). This is a simple Cu-Cu bond that is scalable to a much finer contact pitch ($\leq$ 30µm). Furthermore, when the die element is bonded

to the silicon interposer there is no remaining air gap so application of underfill between surfaces is not required. The direct bond interconnect process is also being utilized for thin wafer-to-wafer joining as well as joining singulated die prepared with aligned TSV contact features. The actual Cu-Cu annealing process for this requires a relatively short exposure time at a moderate 200 ^{o}C temperature.

Summary and Conclusions

While developers continue to explore alternative semiconductor package assembly methods to further improve yield, significant challenges remain for the newer generations of high-density and high I/O semiconductors. Although high volume consumer electronics will continue to drive similar forms of 3D package technology, high-end Telecom markets will rely on more sophisticated solutions. New generations of memory products have emerged with 30 micron pitch and two-thousand I/O and processors are entering the market that have forty-thousand I/O. To meet the requirement for interconnecting these very large, high I/O die elements, analysts and industry roadmaps predict that companies will continue to migrate toward silicon-based or glass-based interposer technology. Although many process issues have been resolved, there are a significant number of technical issues that influence this segment of the industry. The handling and transport of the large and very thin wafers, solutions for aligning and joining very high I/O die elements, and, when the system level package is incorporated into the end product, methodologies for managing thermal dissipation.

The decision on which interposer base material is selected will be dependent on process maturity, supplier capability and cost. In order to expedite product development many are partnering with suppliers at both the frontend and backend of the semiconductor supply chain. They realize that in order to bring 2.5D and 3D package technology into the forefront they will need to develop viable and robust, high yield wafer level interposer processes.

General References and Acknowledgements:

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Introduction

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- For a wide range of applications, both single and multiple die-stack package assembly processes will likely continue to employ conventional face-up die attach and wire-bond methodology.

But…the use of wire-bond interconnect as the exclusive means of termination is somewhat restrictive because it requires significant surface area to accommodate the die-to-interposer wire-bond process.

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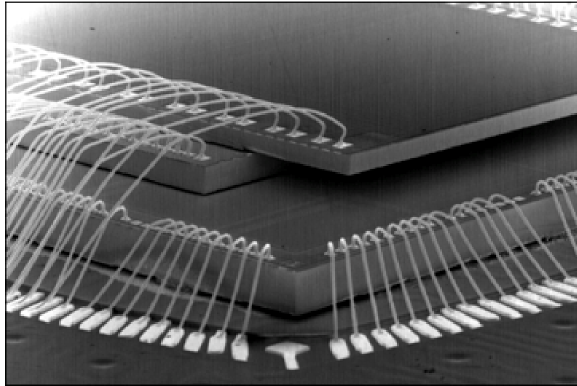
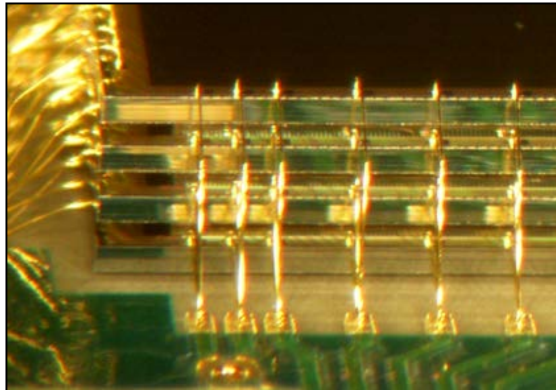
Early 3D Semiconductor Package Solutions



Pyramid Die Stack
Example Source: Intel Corporation

- Die elements are sequentially attached on top of one another.
- The progressively smaller die outline leaves the edge of all die elements accessible for wire-bond in a single operation.



Same Size Die Stack
Example Source: Diemation

- When die elements have the same outline or nearly the same outline, thin silicon spacers are added between die elements to clear wire-bond loop heights.

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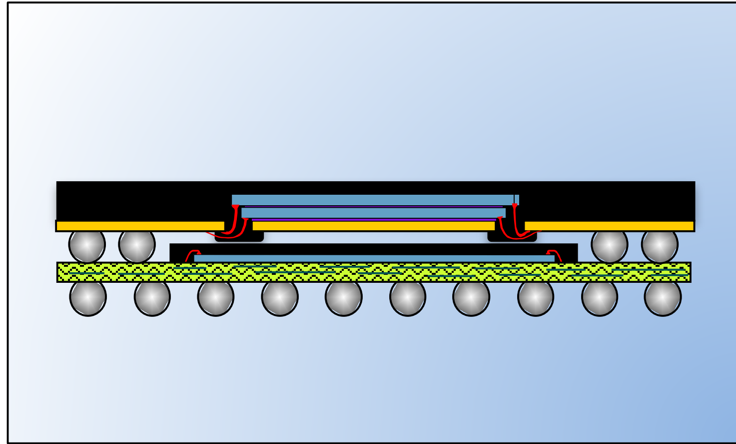
A great deal of progress has been made in 3D package process refinement and system development, however, methodologies will vary a great deal.

Issues that will need to be resolved, include;

- Selection of suitable semiconductors for multiple die packaging
- Establish a reliable sources for semiconductor elements
- Specify physical and environmental operating conditions
- Define package design constraints and process protocols
- Stipulate electrical test method and post assembly inspection criteria

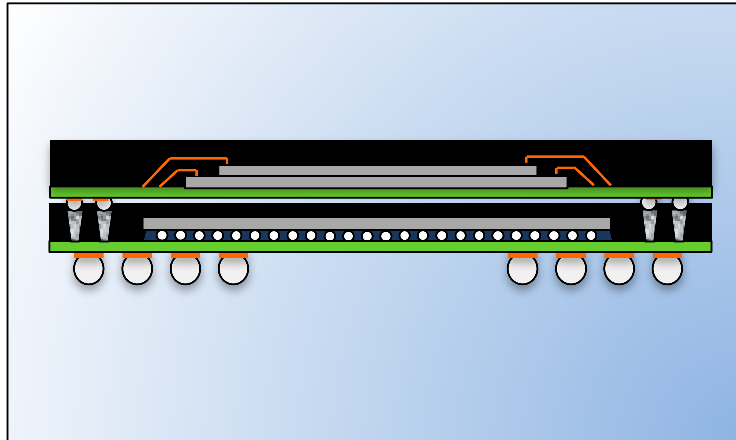
3D Package 'Stacked Package' Solutions



BGA Package-on-Package

- Vertically mounting one or more pre-packaged die elements (package-on-package) is preferred alternative for multiple heterogeneous die applications.

Ball diameter and pitch is typically larger on the upper package section.



Through-Mold-Via PoP

- Through-mold-via (TMV) enables smaller and closer pitch contact features between the upper and lower section.
- Mold design allows material to extend out to the edge of the interposer on the lower section to minimize package warp.

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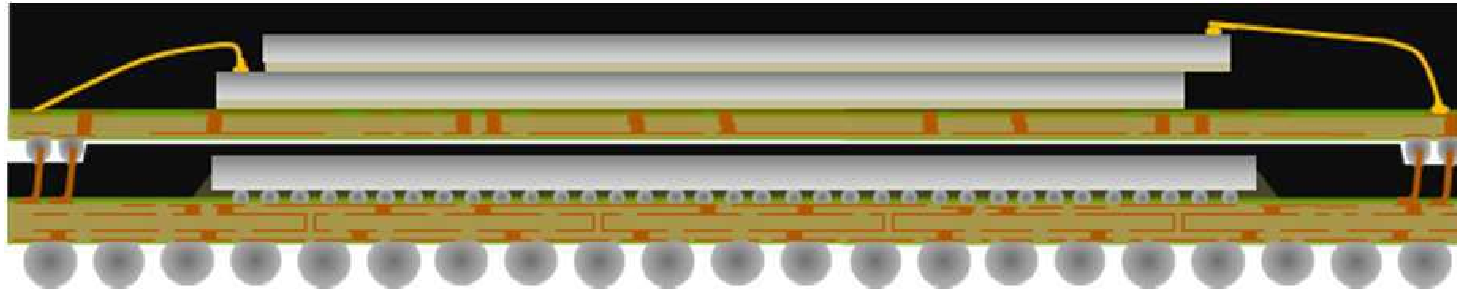
Bond Via Array PoP

- An alternative high-density substrate interconnect solution has evolved to overcome the limiting aspects of the more traditional PoP assembly method.



The bond via array process enables a substantial reduction in interface contact pitch between the lower and upper package sections.

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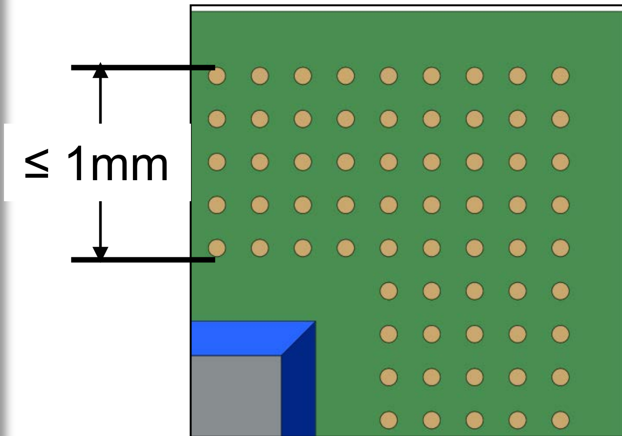
Bond Via Array Contact (I/O) Density Potential

No. of IO rows

Pitch (mm)	2	3	4	5	6
0.50	**200**	**288**	-	-	-
0.40	**248**	**360**	-	-	-
0.30	**336**	**492**	**640**	-	-
0.25	**408**	**600**	**784**	**960**	-
0.20	**512**	**756**	**992**	**1220**	**1440**



Data source: Invensas

Bond Via Array with 240µm pitch can offer up to 1000 I/O using the same amount of area currently required for the 0.5mm FBGA pitch PoP.

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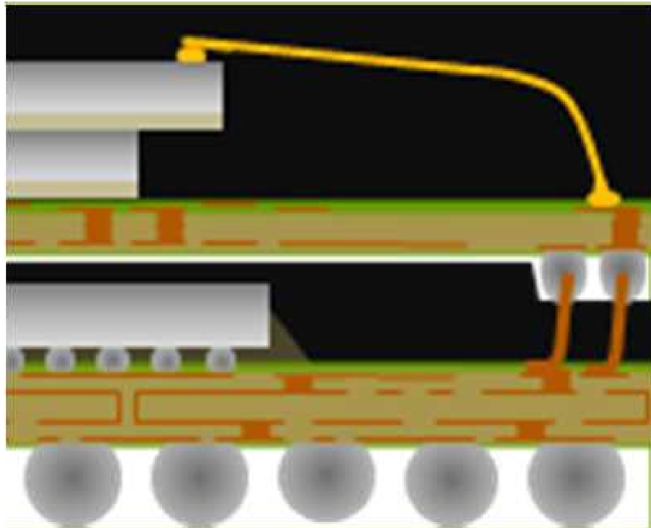
Bond Via Array PoP Assembly

- The main features of the package assembly is that the Pd plated Cu wire-bond contacts are encased and supported in the mold compound that encapsulates the lower package semiconductor.
  - The Cu wire extends from the top surface of the lower substrate to matching contact locations on the bottom surface of the upper package.



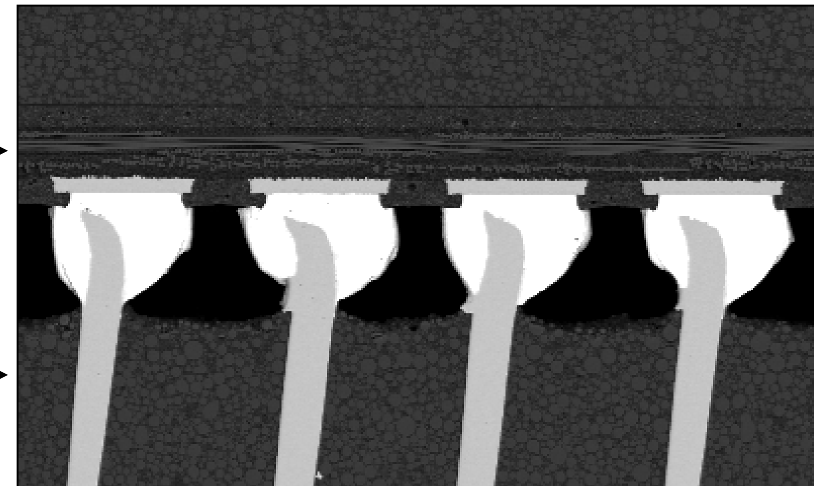
The reduced contact pitch will easily accommodate a greater number of interconnects in the PoP perimeter stacking arrangement.

Bond Via Array Cu Wire to Solder Ball Interface

- The stacked PoP units are heated to 240° C in an in-line convection furnace to reflow the solder and provide a uniform solder interface between the solder bump and Cu contact tip.

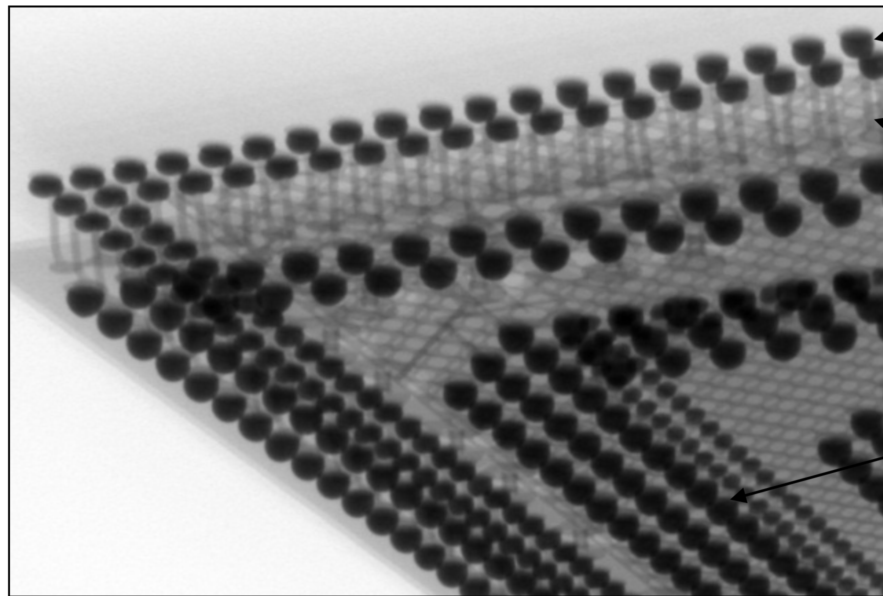
Solder bumped upper package section

Bond Via Array prepared lower package section



Example source: Invensas

Bond Via Array PoP Interface Verification



Solder joint to upper package section

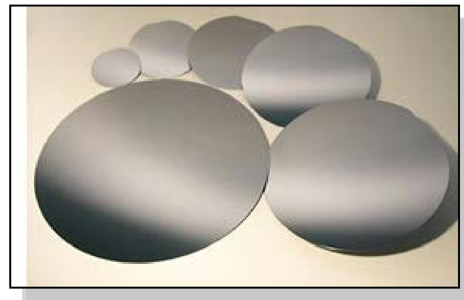
Bond Via Array contact on lower package section

Solder ball contacts on bottom of the lower package section

Example source: Invensas

Evolving 2.5D Interposer Technology

- New semiconductor families are emerging that demand greater interconnect densities than possible with today's organic substrate fabrication technology.
- Two alternative base materials have already proved to be more suitable for both current and future, very high-density package applications---



Silicon, available in 200mm, 300mm and 400mm wafers

Glass, available in both wafer and panel formats

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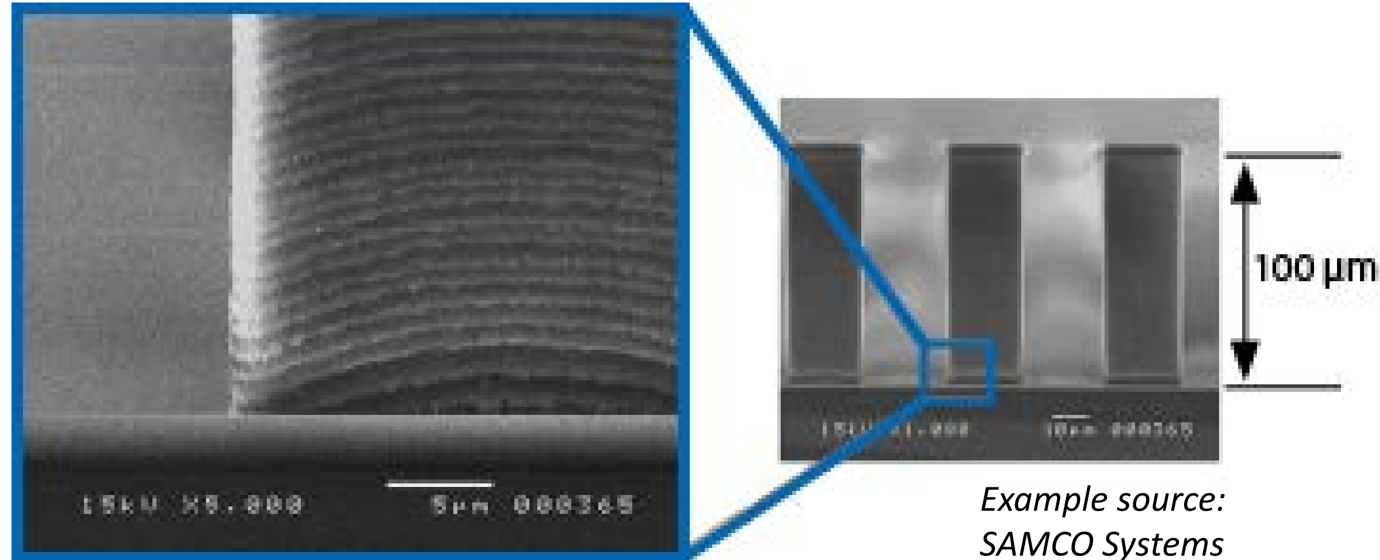
TSV and TGV

- Both silicon and glass materials require adopting unique via formation and metallization methodologies to enable the interface between one side of the interposer to the other.
- The terms ‘through-silicon-via’ (TSV) and ‘through-glass-via’ (TGV) are applied to describe miniature ablated and plated via features in the interposer base material.

While the infrastructure for supplying the glass-based interposer is progressing, the silicon-based interposer supply infrastructure is already well established.

Through Silicon Via (TSV) Formation

- TSV enables efficient fan-out redistribution of very fine-pitch contact features on complex die elements.

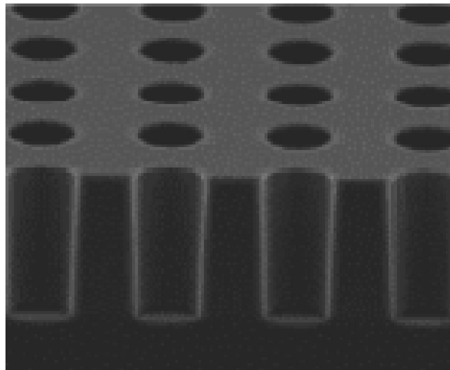


Example source: SAMCO Systems

The vias are commonly formed using a deep reactive-ion plasma etching (DRIE) process.

TSV continued…

The process utilizes a ‘pulsed’ or ‘time-multiplexed’ dry etching technique that alternates repeatedly between two modes to achieve nearly vertical hole structures.



Example source: Panasonic

During the pulsed dry etching process a passivation layer is formed onto the vias sidewall to block further chemical assault and prevent additional etching.

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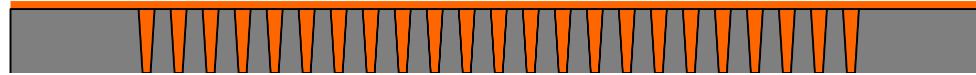
Via Filling and Circuit Forming

- In preparation for via filling a seed layer of copper or tungsten is first applied to enable electroplating the additional copper required to complete the via fill operation.



- To finally access the metallized 'blind' vias on the opposite surface of the wafer, a combination of grinding and/or etching processes are utilized.

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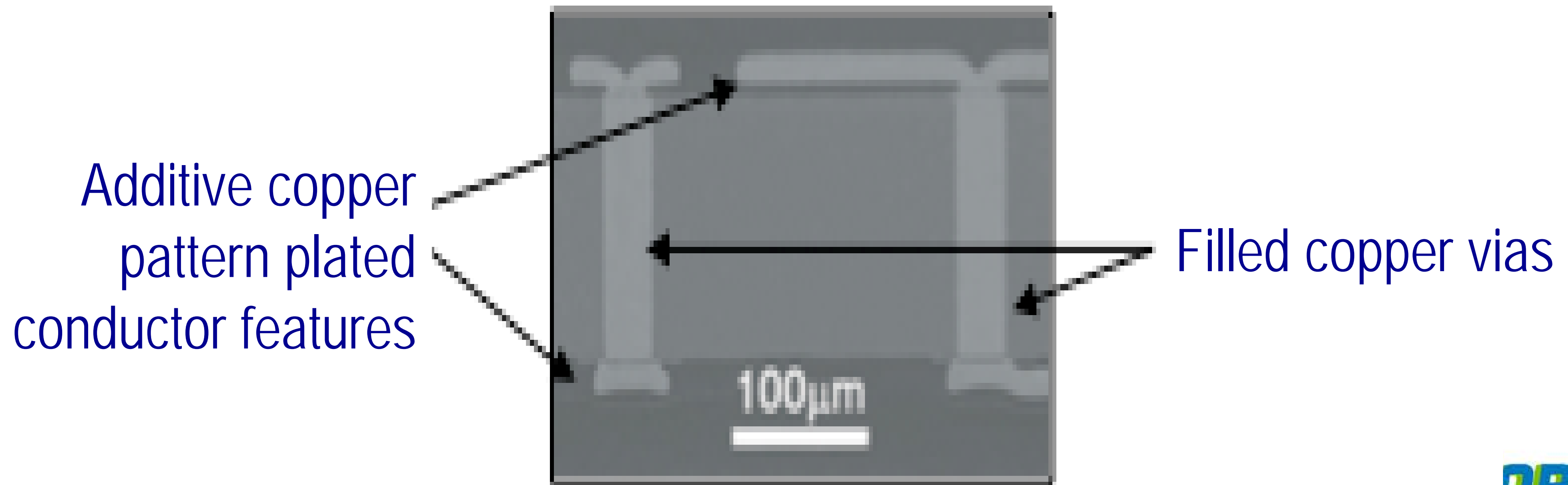
Circuit Forming for Silicon Based Interposers

- Following via filling and thinning of the wafer a additive Cu pattern plating process is employed to provide die attachment sites and fan-out conductors contact features.



Example source: STATSChipPac

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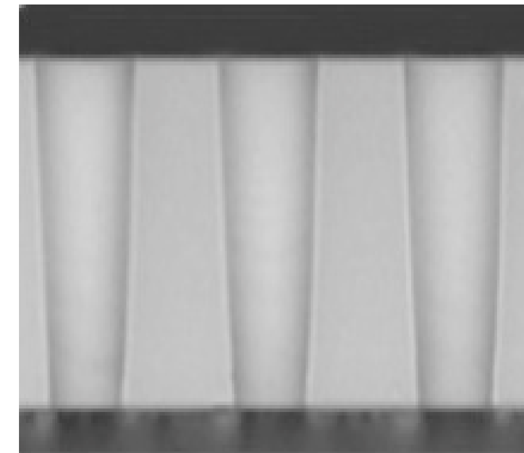
Through Glass Via (TGV) Formation

- Several techniques are being employed to provide vias in thin glass wafers and panels:
  - Laser- CO_2, Excimer, nanosecond UV, picosecond and femtosecond UV
  - Electrostatic discharge (ESD)
  - Mechanical drilling using micro-sandblasting
  - Etching and a combination of processes noted above.



Example source: Corning

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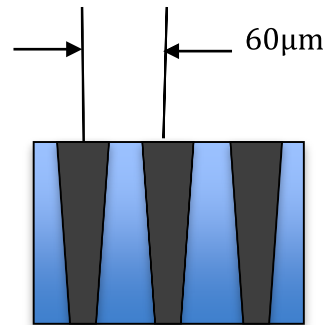
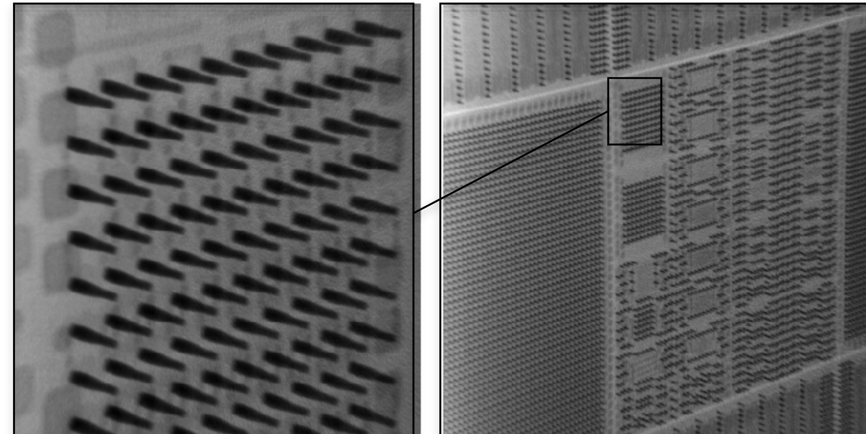
TGV Filling and Interconnect

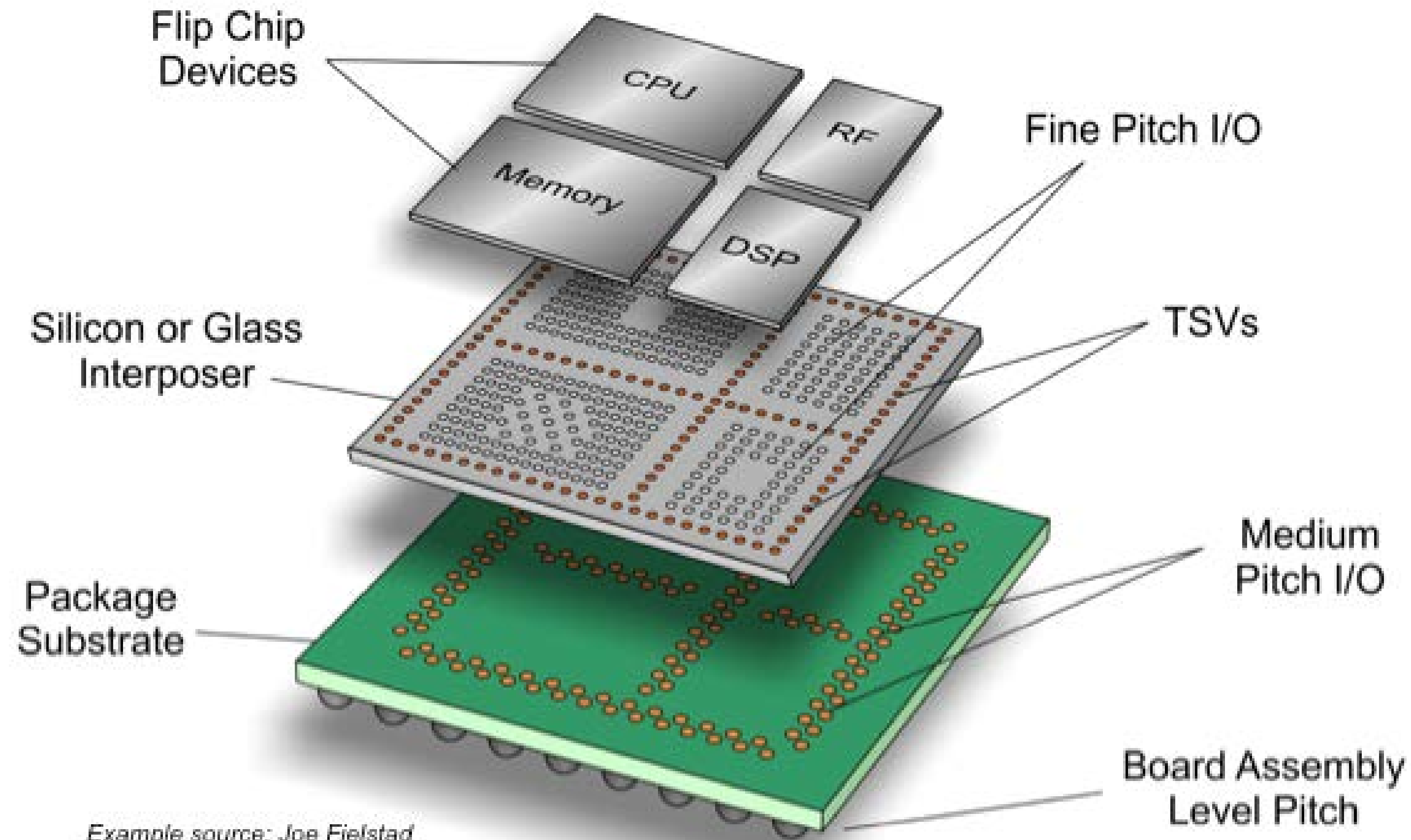
- Copper interconnections can be achieved using a physical vapor deposition (PVD) process and deposited copper paste
- Copper or silver ink can be printed on the interposer surface to provide interconnect circuitry.





Example source: Corning

System Level 3D Packaging

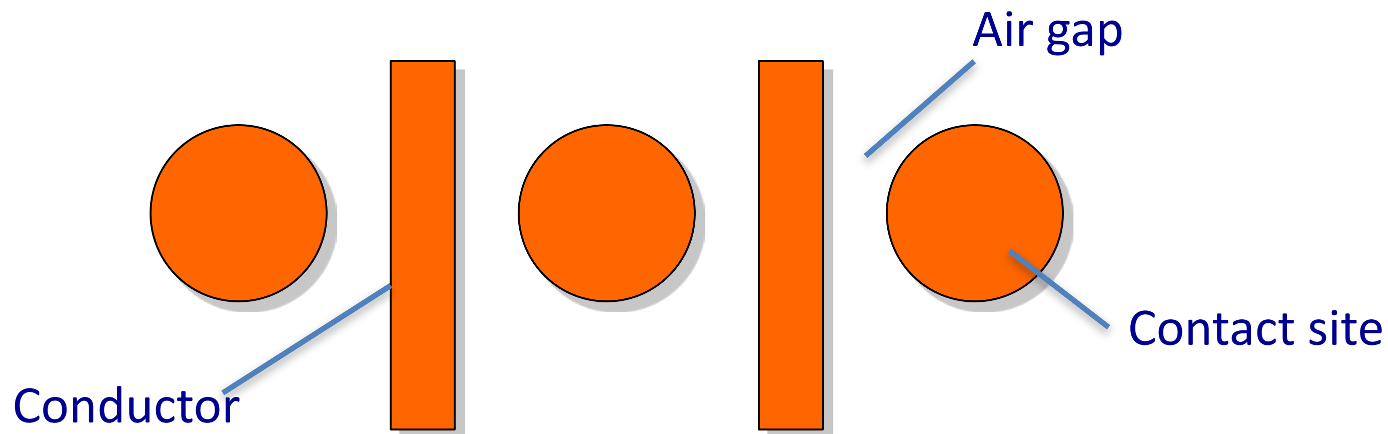


Challenges for New Generation High I/O Semiconductors

- Processor and memory examples
  - CPU outline:
    - *11.0 mm x 11.0 mm*
  - CPU I/O and pitch:
    - *40,000 @ 30µm*
  - *Memory outline:*
    - *6.0 mm x 8.0 mm*
  - *Memory I/O and pitch:*
    - *2,000 @ 30µm*

Interposer Circuit Routing Example for Fine-Pitch and High I/O Die

- Contact Pitch- 30µm (~0.0012”)
- Contact Diameter- 15µm (~0.0006”)
- Space (between contacts)- 15µm (~0.0006”)
- Conductor Width- ~ 5µm (~0.0002”)
- Air Gap (clearance) ~ 5µm (~0.0002”)



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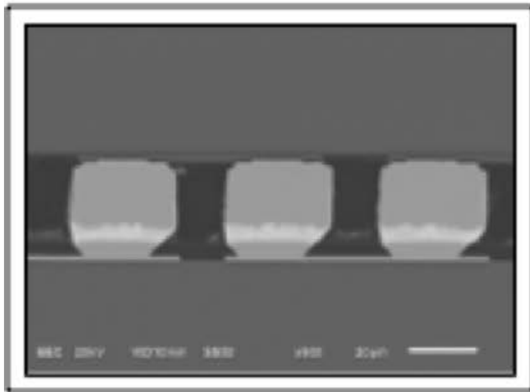
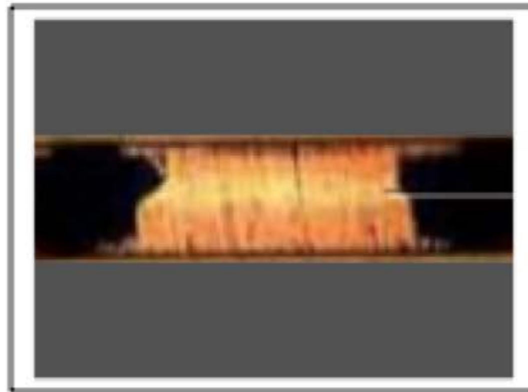
Fine-Pitch and High I/O Die-to-Interposer Joining

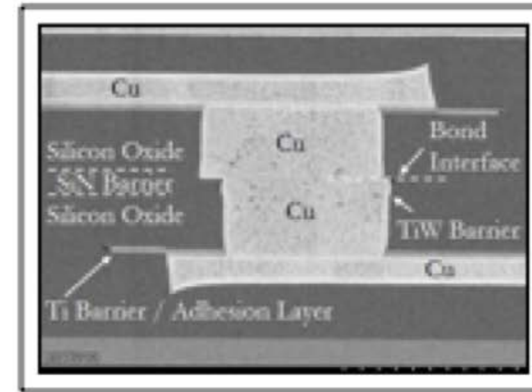
- The methodologies for face-down joining high-density die elements on silicon include:
  - Solder reflow process
  - Thermo-compression bonding
  - Annealed Cu Bond Interconnect



Cu post-Sn/Ag-Cu Bond
Example source: Invensas

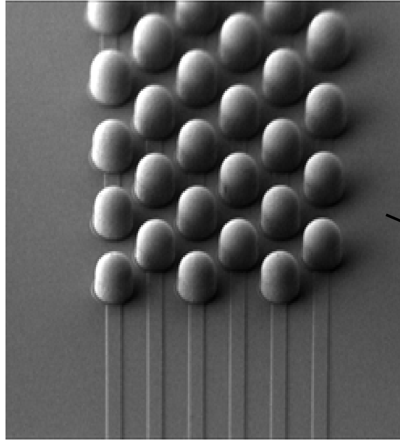


Cu-Sn^3-Cu Bond
Example source: Qimonda



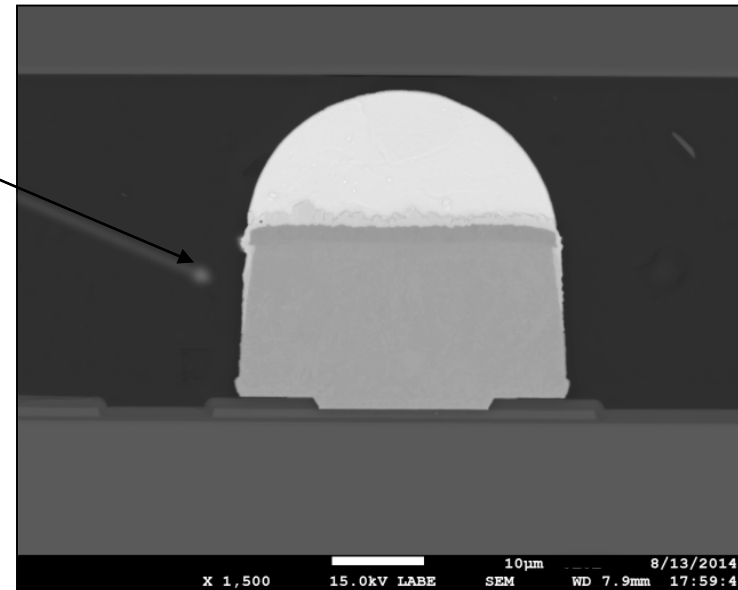
Annealed Cu-Cu Bond
Example source: Ziptronix

Solder Capped Cu Pillar Micro-Bumped Die Example



SEM image of the reflowed solder capped Cu pillar micro-bumps

35µm dia. x 35µm high x 60µm pitch

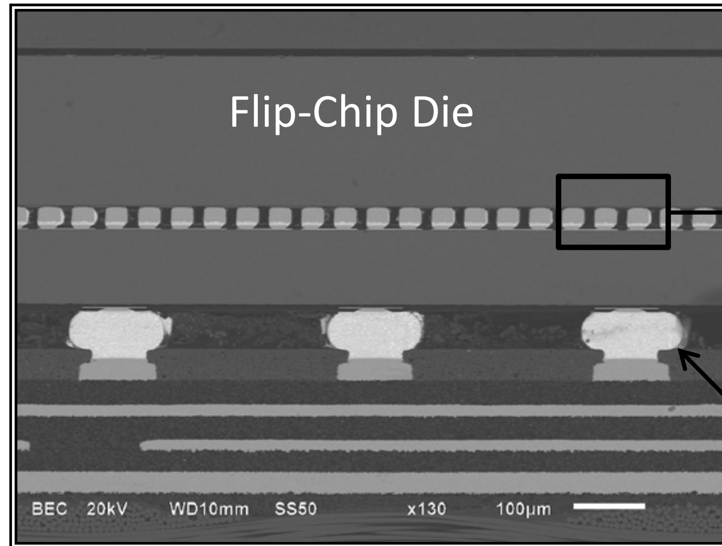


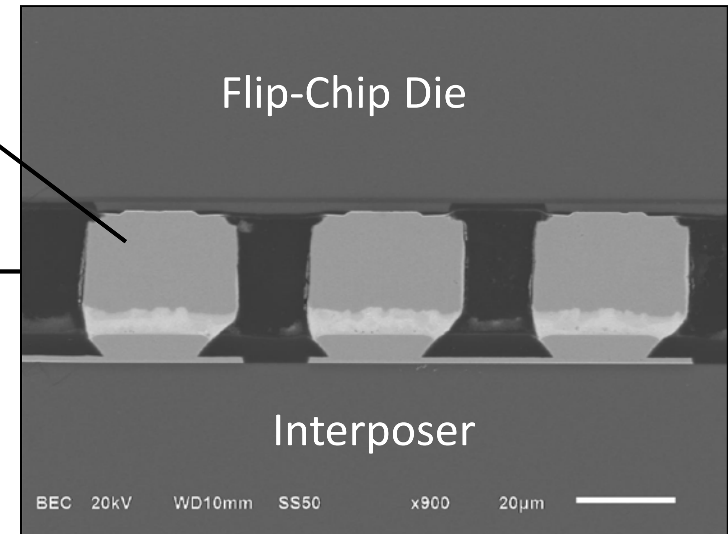
SEM image of a Cu pillar and solder cap.

Example source: Invensas

Post Assembly View, Micro-Bump Flip-Chip to Si Interposer Assembly

Cu micro-bump contact





Solder ball or bump interconnects to package substrate

Example source: Invensas

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Micro-Bump Solder Process

- Developers have demonstrated reliable micro-bump solder attach assembly processes
- Key solder process issues:
  - Optimized reflow temperature profiles, flux activation and time above liquidus (TAL)
  - Flux selection is critical for micro-bump solder joint integrity and to minimize voiding of underfill

Cost, manufacturability and scalability challenges remain an issue

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Thermo-Compression Bond
(Cu/Sn/Cu Fusion)

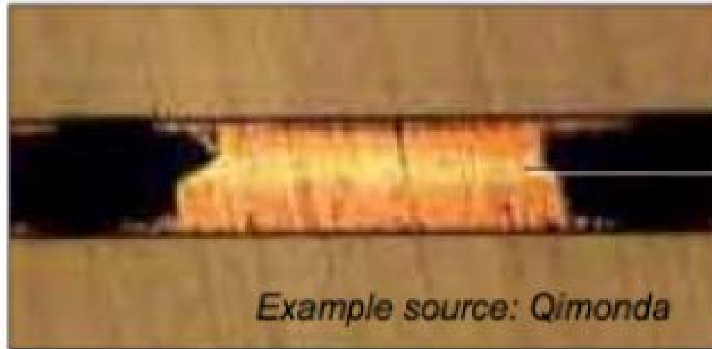
- TCB is a two-stage procedure that begins with the initial precise alignment and a room temperature pre-bonding of the die element to the interposer wafer.
- Following pre-bond, the interposer is exposed to an annealing process that includes high temperature and pressure.

This joining process is significantly enhanced with the deposition of a thin layer of tin-alloy onto the exposed copper contact features.

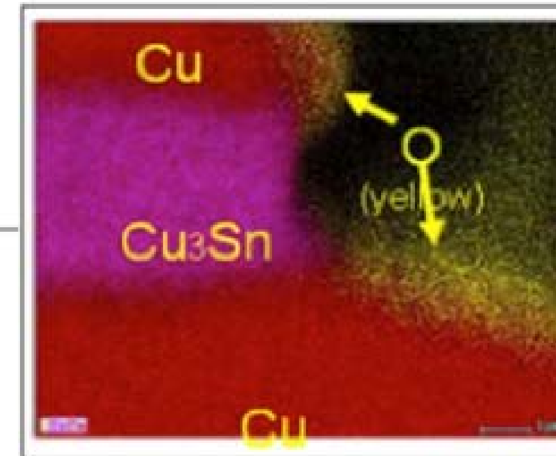
TCB Post Process View

Cu/Cu3Sn/Cu intermetallic bond.

- When the die element and Si interposer is heated to approximately 400°C, the tin alloy will completely diffuse into the opposing copper contact features to form a stable Cu-Sn- Cu (Cu_3Sn) intermetallic



Cross section image of the bond between wafer pairs



Example source: Invensas

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Annealed Cu-Cu Bond Interconnect

- Oxide enabled Cu-to-Cu bonding is a low temperature hybrid process that addresses many die-to-interposer bonding challenges…
  - Oxide bonding (low temperature homogeneous bonding technology) is already proven for high volume manufacturing of CMOS Image Sensors
  - Low temperature hybrid bonding technology provides a scalable, low cost solution for the very high density, high I/O interconnect applications

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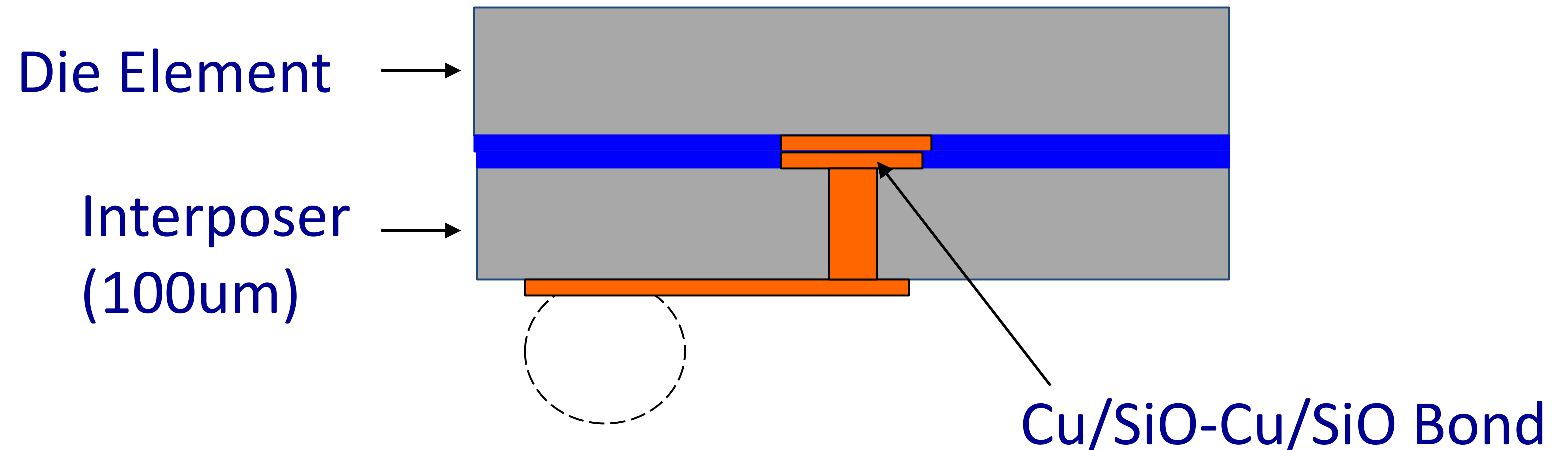
Heterogeneous Die-to-Interposer Bond

– This is a Heterogeneous or Hybrid joining process furnishing an In-Situ electrical interface with patterned metal/dielectric

(e.g., Cu/SiO-Cu/SiO, Cu/SiN-Cu/SiN)

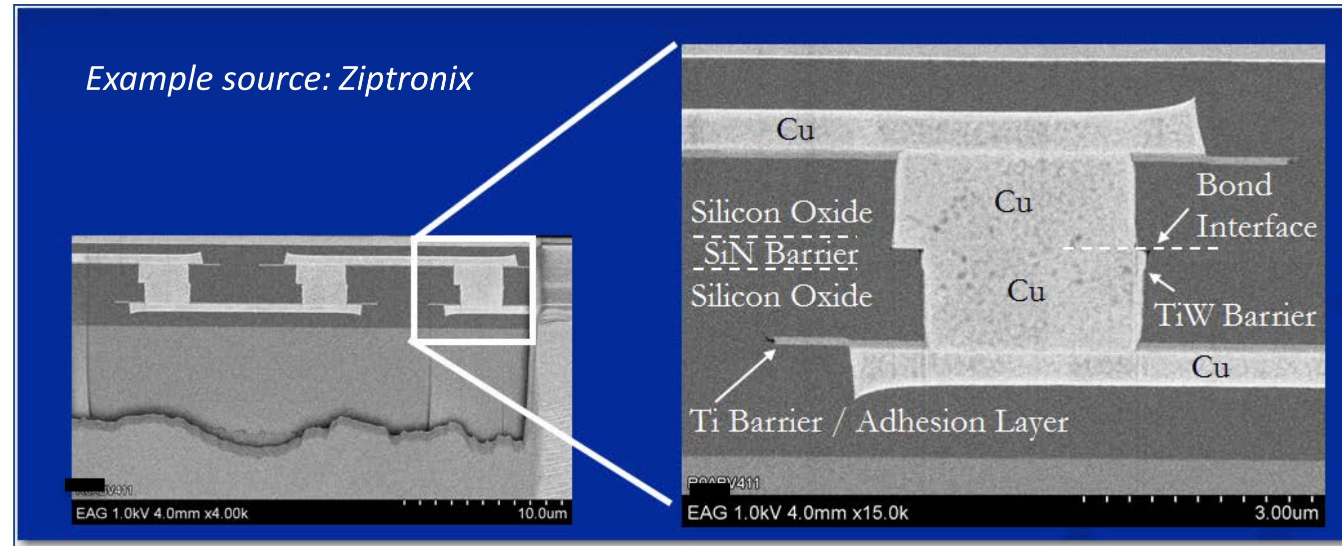


Low Temperature Hybrid Bonding Technology

Post Process View

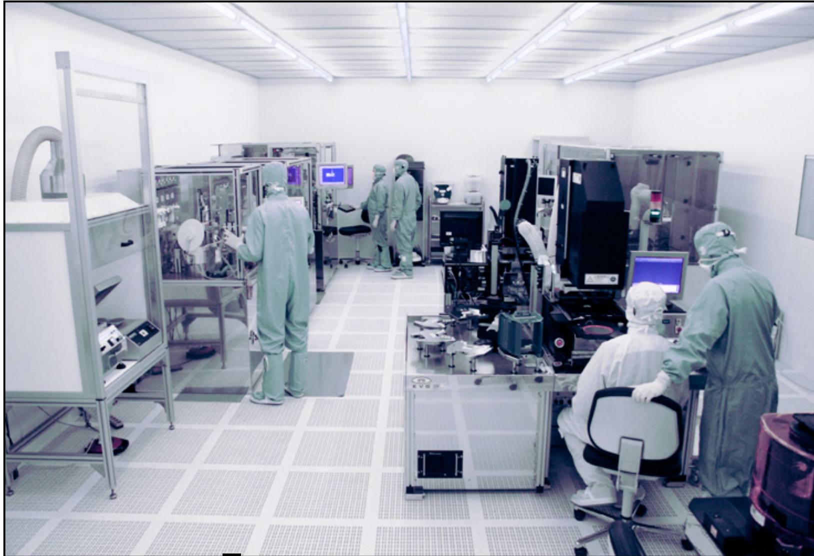
- The silicon/oxide layer enables a simple Cu-Cu bond---

No solder and No underfill required



The process is scalable to very higher density sub-micron pitch semiconductors

Implementation Issues


Clean room photo source: EV Group

- Cost, *always cost*
  - Equipment throughput, facility development, tooling costs, amortization period.
  - Associated consumables; gasses, slurries, resist materials.
  - Fab parameters; number of wafers, engineering resources.
  - Geographic local; operator costs, environmental restrictions.

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Summary and Conclusions

- High volume consumer electronics will continue to drive traditional forms of 3D packaging but high-end Telecom markets must rely on more sophisticated solutions.
- To meet the requirement for interconnecting the large, high I/O die elements, companies are expected to adopt silicon-based or glass-based interposer technology.
- That said, significant package challenges remain for interconnecting future generations of even higher-density and higher I/O semiconductors.

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Summary and Conclusions Cont.

- Although many interposer process issues have been resolved, there remain significant technical issues that influence this segment of the industry.
  - The handling and transport of the large and very thin wafers
  - Solutions for aligning and joining very high I/O die elements

When the system level package is incorporated into the end product, efficient solutions must be developed for managing thermal dissipation.

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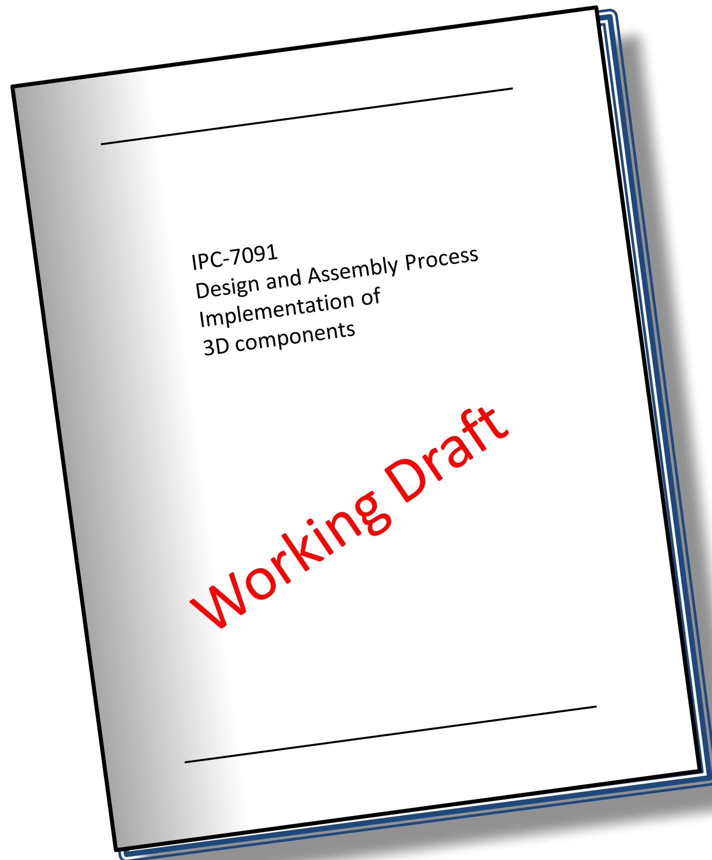
Current 3D Standard in Development



IPC-7091 *Design and Assembly Process Implementation of 3D components*- This document includes the design and assembly challenges for implementing TSV and TGV interposer technology.

The focus is on achieving optimum functionality, process assessment, end product reliability when implementing high-density semiconductor packaging

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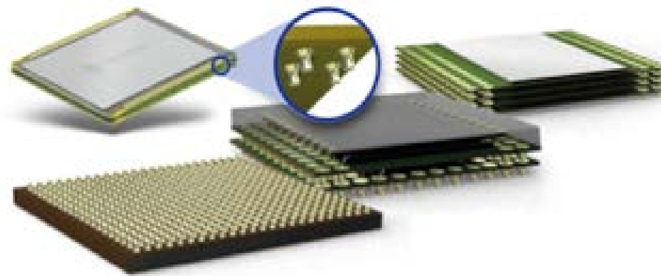
- Acknowledgements:
  - Dr. Charles Woychik, Wael Zohni, Dr. Bel Haba and the package development team at Invensas

Thank you



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