ANALOG FASTSPICE PLATFORM FULL-CIRCUIT PLL VERIFICATION

APPLICATION BRIEF

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Phase-locked loops (PLLs) use negative feedback to generate periodic signals for synchronization and as frequency references in IC designs. PLLs provide clocking in digital systems like CPUs, data converters (analog-to-digital converters and digital-to-analog converters), and high-speed I/Os). PLL-based frequency synthesizers are used in wireless applications such as cellular transceivers, WiFi transceivers, TV tuners, and RF receivers.

PLL designers need to deliver a stable, low-noise, tunable signal at a specified frequency with fast locking times, low power, and high yield. However, the most important and challenging PLL performance specification is low jitter or phase noise. Figure 1 shows the block diagram for a fractional-N PLL. Each block contributes to the output jitter/phase noise as a function of its noise generation and noise transfer function to the PLL output. Output jitter/phase noise is also a function of process, voltage, and temperature (PVT) variations. Device noise, post-layout parasitics, process variability, and device mismatch significantly impact PLL performance at nanometer technology nodes.

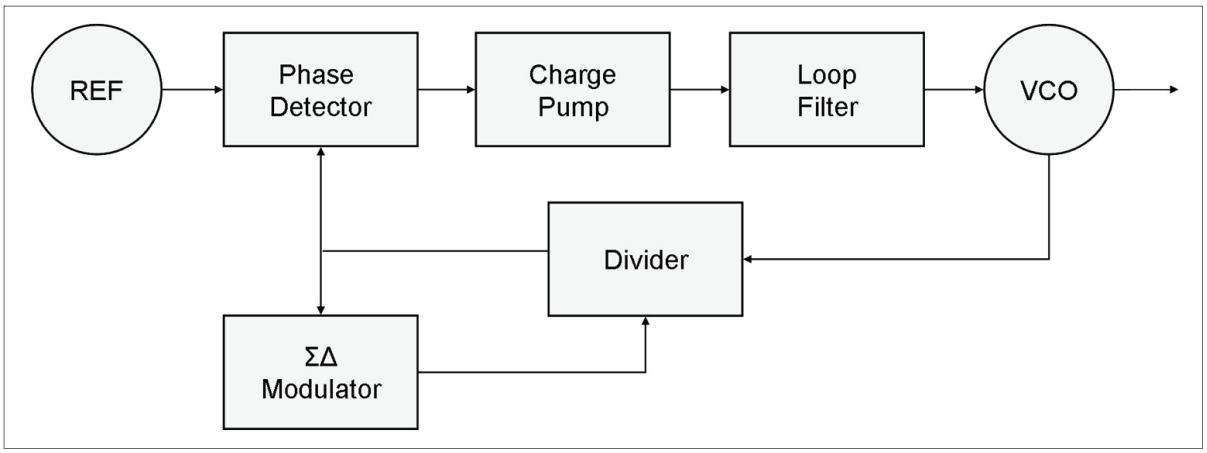

Figure 1: Fractional-N PLL Block Diagram

When designing PLLs in nanometer CMOS, it is essential to validate the key closed-loop PLL performance metrics with nanometer SPICE accuracy before going to silicon. This means performing full-circuit verification at the transistor-level to account for performance degradation due to architecture limitations, device noise, post-layout parasitics, process variability, and device mismatch.

Transistor-level, closed-loop PLL verification has been impossible or impractical due to traditional SPICE and RF simulator performance and capacity limitations. Thus designers have had to rely on block-level verification and behavioral models. PLL designers typically run block-level periodic noise analysis (pnoise) to compute the noise contribution of individual blocks. With frequency-based tools, these results are approximations based on the number of sidebands or harmonics. While reasonable at larger process nodes, such approximations are increasingly inaccurate at lower process nodes. To verify the closed-loop PLL performance, designers must then use the block-level noise results in a behavioral model, the simulation of which is literally an approximation based on approximations.

With the Analog FastSPICE™ (AFS) platform, designers no longer need to rely on such approximations. For block-level analysis, AFS RF delivers full-spectrum, periodic noise analysis technology that does not trade off accuracy for performance. AFS RF also includes VCOPSS and VCONOISE analyses, which target voltage-controlled oscillator (VCO) optimization in PLLs.

AFS Transient Noise analysis (AFS TN) delivers closed-loop PLL transistor-level verification, including the effects of device noise, with nanometer SPICE accuracy. In addition, designers can include post-layout parasitics and characterize the circuit for process variation and device mismatch. Furthermore, AFS Multi-Core Parallel (AFS MCP) reduces AFS TN run times by up to 4x by automatically running multiple transient noise simulations in parallel.

Automated post-processing with the AFS WaveCrave Calculator Pad combines parallel simulation results, supports direct jitter measurements, and automates phase noise measurements with fast Fourier transform (FFT)-based post-processing.

Figure 2 compares post-processed AFS TN results for an Integer-N PLL to the silicon measurement. AFS TN consistently produces phase noise results that correlate to within 1–2 dB of silicon measurements. The alternative is to wait for silicon and hope for the best.

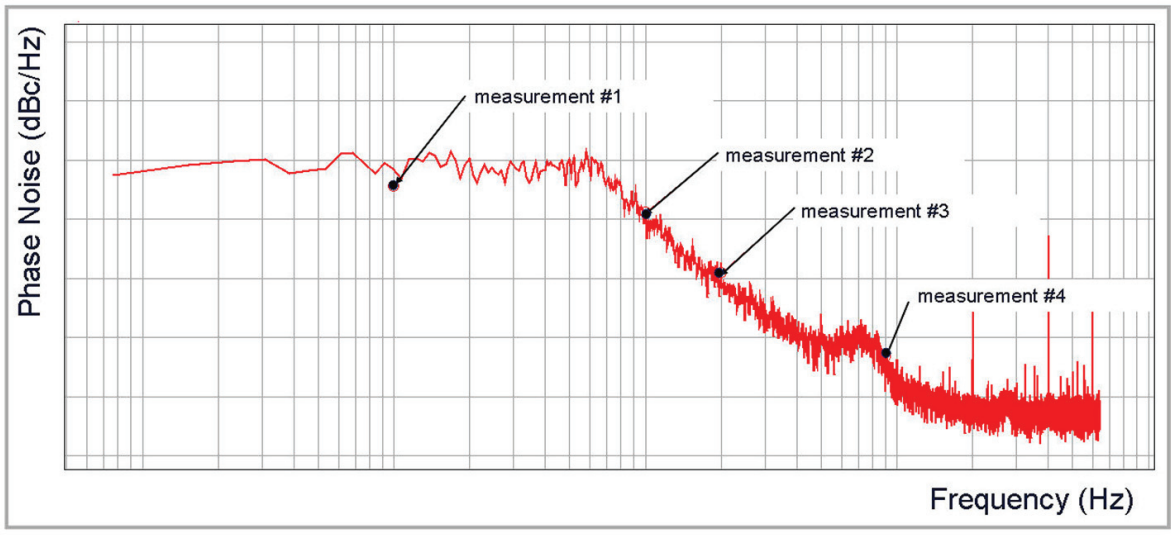

Figure 2: Integer-N PLL AFS TN versus Silicon

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