Autorouting Techniques for Multichip Modules

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Abstract
Many PCB designers are interested in taking advantage of Multichip Modules, but are unfamiliar with the technology. While the design process is very much the same, MCM manufacturing processes vary dramatically. MCM routing requirements are dictated by the manufacturing process and types of components. Components mounted on MCM substrates are predominantly, if not exclusively, bare chips. As a result, the component body and I/O pins are no longer constrained to industry standard pin counts and form factors as are packaged components. In addition, component interconnection technologies such as wire bond, tape automated bonding (TAB), and flip-chip compound the routing challenges. The choice of substrate manufacturing technology will affect via and trace constraints. Find out more about these unique routing requirements and some of the autorouting techniques used to address them.

Key Words: MCM, Autorouter, Wire Bond, TAB, Flip Chip, Staggered Via, Breakout

Introduction
Today's printed circuit board designers are increasingly faced with the challenges of higher density, increased performance, or reduced overall system cost. PCMCIA cards, portable electronics, avionics, and workstations are a few of the applications in which MCM technology is being used. By removing the component packages and packing components closer together, signal delays are reduced as a result of shorter interconnect distances. By reducing layer count, printed circuit board area, and total number of boards in a system, overall system cost can be reduced as well.

For PCB designers, the physical design of an MCM is very much like that of PC boards. The technology differences between PCB and MCM technology are characterized in Table 1.

In addition, there are differences in MCM technologies (Table 2), their corresponding design rules, and manufacturing requirements, all of which will influence routing strategy.

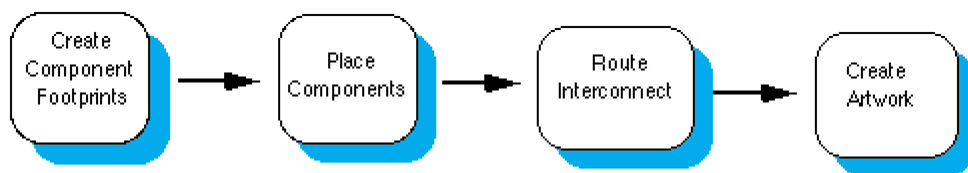


Figure 1. Physical Design Flow MCM

Autorouter Concepts
Let's first review some facts about autorouters. Most autorouters used for PCB and MCM design are capable of orthogonal and diagonal routing. All-angle routing (not
a multiple of 45 degrees) is typically done manually or treated as a special case. Routing bond wires from bare dies, for example, is one such special case.

While grid-based routers have been used to route printed circuit boards for many years, shape-based routers are increasing in popularity. With respect to MCMs, both routers have merit. In some cases, gridded routers have out-performed shape routers, and vice-versa.

Both gridded and shape-based automatic routers are cost-driven, based on the Lee algorithm[1]. Cost is a weight factor used to control router behavior. This paper will focus on gridded routers, although the concepts will generally apply to both gridded and shape autorouters.

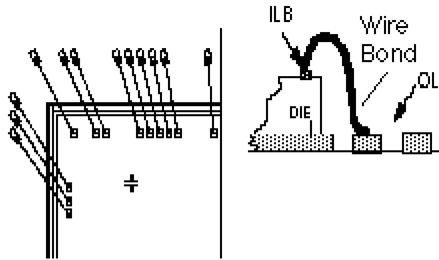
ARTROUTERgridTM, is a grid-based router with the following characteristics.

Iterative - can be set for many passes.
Maze-runner algorithm - Each connection is routed from source to target. The router follows the grid, deciding at each grid point which direction to move next.
Cost-Driven - Router decisions are based on the cost of each move.
Rip-up and re-try - The autorouter will rip-up and re-route unfavorable connections on each subsequent pass.

Table 1	
PCB	**MCM**
packaged components	unpackaged components
low component density	high component density
low interconnect density	high interconnect density
large vias	small vias
standard component pin pitch	arbitrary component pin pitch

Table 2				
Design Rules Comparison				
	PCB (mils/μm)	MCM-L (mils/μm)	MCM-C (mils/μm)	MCM-D (mils/μm)
trace width	6/150	3/75	4/100	1/25
trace-trace	6/150	3/75	4/100	2/50
via pad	20/500	8/200	8/200	3/75

Component Pins
Libraries of unpackaged components are much more limited than those available for packaged components because of their uniqueness. A 28 pin dip package, for example, is standard for many components in a variety of technologies and functions. On the other hand, components in their unpackaged silicon form tend to change frequently as IC manufacturers make process and design improvements. With packaged components, these changes are transparent to the system designer; therefore the geometry that he uses does not change. To facilitate the component creation process, CAD vendors are working together with MCM vendors to automate this process with interfaces that extract component data from an emerging standard called DIE (Device Information Exchange) format. The DIE format specifies die size, pad location and size, and pin type, as well as thermal, electrical, and mechanical information.



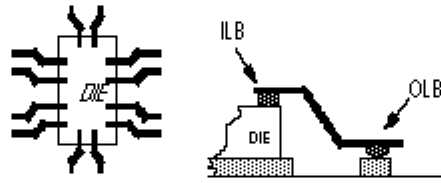


Figure 2. Radial Wire Bond

Figure 3. TAB Component

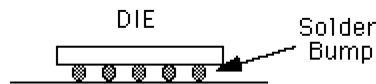


Figure 4.Flip Chip Component

From a CAD perspective, component pins are typically defined as surface pins since they represent the surface metal of the die. Many MCM vendors provide design kits with pre-defined pin padstacks and via padstacks, facilitating padstack definition and minimizing the risk of manufacturing errors.

Wire bond is the most common and mature of the chip connection technologies (Figure 2). Radial fan out from inner lead bond (ILB) to a single row outer lead bond (OLB) can be very area-inefficient if the minimum OLB pitch is greater than the ILB pitch.

VLSI chips with pads at the periphery can have pad pitches as low as 4 mils. Ideally, chip to substrate connection to the OLB would radiate out in a direction orthogonal to the edge of the chip a minimum distance from the ILB. Via pitch, however, is typically selected to allow 2 to 4 traces between vias. As a result, the wire bond fanout pattern could increase the footprint (chip outline plus OLBs). Multiple rows can be used to decrease the effective OLB pitch, reducing the footprint perimeter and wire bond length.

The autorouter does not route bond wires, but has the ability to use a variety of via types, including staggered, blind, buried, and through-vias. Via staggering is required when manufacturing constraints limit the number of vias that are coincident in the vertical axis. (Figure 5.)

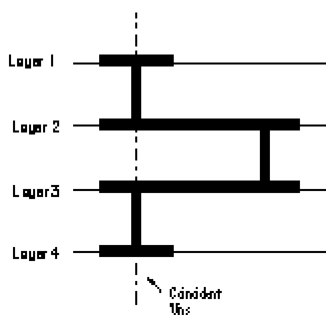


Figure 5. Staggered Vias

Escape Routing

Multirow OLB pads and flip chip die pins result in area array patterns that congest routing channels. In order to escape, there must be sufficient channel capacity for pins in the innermost rows. Typically, the surface layers are congested with large land pad features, making routing difficult. Conventional strategy is

to escape or break out these land pads inward and/or outward, to redistribute the connections to routing layers.[2] Breakout router algorithms attempt to route stubs from the land pad to the first available via site and place a via. Subsequent autoroute passes attempt to route the remaining connection from the end of the via. On dense designs, the order of the sorted connection list could induce the router to block escape channels on lower layers preventing connection to pins on the interior of the array.

Consider a via pitch of .030 inches that permits one trace .006 inches routed between vias. Assuming the pin pitch is greater than or equal to the via pitch, no more than two rows of pins per layer can escape. Additional layers are required to escape more rows, which is counter to the goal of minimizing layer count.

The solution is to break out to lower layers before the maze-runner algorithms are executed. Maze-runner efficiency, as measured by completion rate, can be improved by allowing pins of the same net to route on the same layer.

For technologies in which vias can be coincident on non-adjacent layers, and vias under the land pads are permitted, a zig-zag stagger is most efficient in that the stagger is in the direction of potential trace escapes, reducing channel blockage.

Thermal Vias

Thermal vias compound routing complexity. These vias are manufactured the same as the electrical vias used to connect conductor layers. By placing these vias under the dies, they increase thermal conductivity through the insulator layers and may be electrically isolated or connected to power/ground planes. In choosing the number and pitch of thermal vias, there is a balance that must be achieved since increasing the number improves thermal performance at the expense of routing capacity.

Summary

With the cooperation of MCM vendors, and the availability of design kits, PCB designers can feel confident in their ability to take advantage of MCM technology by employing the same design approach that they've used for years to design PCBs. While unpackaged components are not usually a concern to PCB designers, they can be treated like packaged components with additional routing restrictions on pin definition, breakout, and via usage. Autorouters that understand these routing restrictions have been proven to effectively route MCMs with excellent results.

References

[1] Lee, C.Y., "An Algorithm for Path Connection and its Applications", IRE Transactions on Electronic Computers, Sept. 1961
[2] McBride, R., Chung, J., Shi, E., Cheng, C., "Pin Redistribution for Multichip Module Designs", Proc. International Symposium on Microelectronics 1993

[3] "Layout Autorouter User's Manual", Rev. 8.2_5, Mentor Graphics Corp

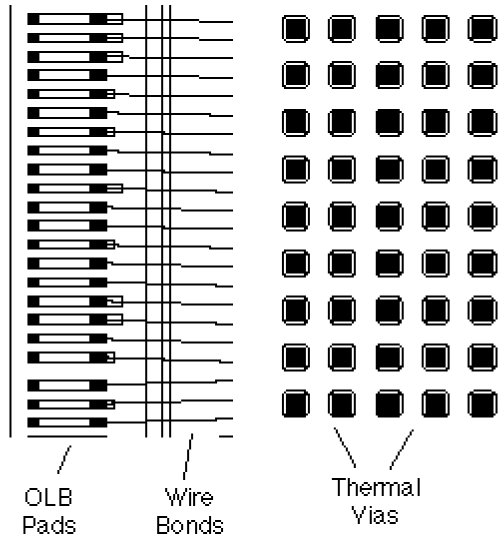


Figure 6. Thermal Vias Under Component

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