Test Structures for Benchmarking the Electrostatic Discharge (ESD) Robustness of CMOS Technologies

Technology Transfer # **98013452A-TR**
SEMATECH
February 27, 1998

Abstract: This document defines a set of standard test structures with which to benchmark the electrostatic discharge (ESD) robustness of CMOS technologies. The test structures are intended to be used to evaluate the elements of an integrated circuit in the high current and voltage ranges characteristic of ESD events. Test structures are given for resistors, diodes, MOS devices, interconnects, silicon control rectifiers, and parasitic devices. The document explains the implementation strategy and the method of tabulating ESD robustness for various technologies.

Keywords: Test Structures, Electrostatic Discharges, CMOS, Semiconductor Diodes

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1 EXECUTIVE SUMMARY

The purpose of establishing an electrostatic discharge (ESD) technology benchmarking strategy is to reduce costs, accelerate product-to-market, and provide ESD-robust designs in the U.S. semiconductor industry.

This document defines a set of standard test structures for evaluating the ESD robustness of various CMOS technologies: resistors, diodes, MOS devices, interconnects, silicon control rectifiers, and parasitic devices. It is intended to be used by semiconductor device and process engineers, ESD reliability engineers, and circuit designers. The structures can be used to compare ESD robustness to other semiconductor disciplines, such as latchup, hot electrons, electromigration, and MOSFET analysis for the optimization and understanding of various semiconductor processes. These standardized structures and metrics also provide a vehicle of communication between the customer and foundry.

The test structures have been defined with the following assumptions:

- The structures are based on standard ESD protection elements in CMOS technology. The structures may be used in other technologies, such as SOI, SiGe, BiCMOS, RF-CMOS, but they do not include new vehicles or structures based on the customization of any specific technology.
- The structures are targeted at P-substrate epi or bulk CMOS. Local substrate plugs contained in some structures are not necessary for epi processes if a low resistance substrate plug is contacted elsewhere.
- The structures are intended to cover both salicided and non-salicided junction technologies. Variations occur when salicide affects test structure geometry.
- The structures assume aluminum or other low resistivity (< 0.1 Ω/square) based first- and second-level metal (Metal 1 and Metal 2, respectively). For other metal schemes, the configuration of metal to the structures should be altered to avoid metal burnout during testing.

2 OBJECTIVES

This work is intended to improve the design process for ESD protection by defining a set of standard test structures to benchmark the ESD robustness of CMOS technologies. The test structures will help evaluate the elements of an integrated circuit in the high current and voltage ranges characteristic of ESD events, well outside the normal range of operation. Knowing the characteristics of circuit elements in these high current and voltage ranges will greatly facilitate ESD protection design. It will reveal how much current an element can carry, how layout parameters affect the amount of current, and which circuit elements need protection.

Because of the dynamic nature of the integrated circuit industry, benchmarking ESD robustness of integrated circuit technologies is extremely important. Products are frequently migrated to new, more advanced technologies; manufacturing may be moved from development or model lines to high volume manufacturing facilities or moved to an integrated circuit foundry. At each of these transitions, changes to the properties of the technology that do not affect standard operation can have disastrous consequences to the ESD robustness of a product. Data on common test structures available in collaborating processes can greatly improve the ability of the

ESD design engineers to avoid problems before they occur and to determine the most compatible ESD structures for all processes involved. Following the standardized test structure practices recommended here will allow the ESD designer to more easily assess commonalties, understand differences, and quickly generate effective ESD protection in product and process development.

2.1 Context

Integrated circuit (IC) product failure from ESD is an important concern in the semiconductor microelectronics industry. ESD has considerable impact on the U.S. semiconductor industry's quality and reliability, yield, delivery, and cost. To prevent undue fallout during assembly, industry standards require that IC products withstand a minimum level of ESD.(See for example the specifications for human body model (HBM) and machine model (MM) in Section 13.9 on Testing in the References. To meet this requirement, ESD protection is built into the I/O and power supply circuits.

2.2 Problem Statement

As CMOS technologies move further into the sub-micron regime, the complexities of the advanced process create numerous difficulties in designing robust ESD protection networks. Lack of understanding of device characteristics in the high current domain often leads to unexpected ESD failures that adversely affect time to market, increase cost, and consume valuable engineering resources.

Standard scaling practices, while optimized for device operation to process logic, have often been shown to have a negative impact on ESD performance. Migration to lower power supply voltages and the associated need for compatibility with I/O operation exacerbates the problem. Scaling must take the high current behavior of devices into account.

Moreover, the business needs of technology transfer, manufacturing sub-contracting, and foundry relations require ESD functionality on a process whose parameters are not necessarily well known. The ability to communicate problems related to ESD robustness between the customer-to-supplier, customer-to-fabrication foundry, and foundry-to-foundry has been an issue because common ESD metrics, standardized test vehicles, common test practices, procedures, and specifications do not exist.

2.3 Purpose

The reason to establish an ESD technology benchmarking strategy is to reduce costs, accelerate product-to-market, and provide ESD-robust designs in the U.S. semiconductor industry.

The purpose of this document is to define a set of standard test structures for evaluating the ESD robustness of a semiconductor technology. This robustness can be understood by comparing standard ESD metrics and electrical parameters, which should make design more successful. With the definition of metrics, technology comparison, migration, and technology scaling can be understood. Standardized structures and metrics will also provide a vehicle of communication between customer and foundry.

Establishing ESD test structures will allow semiconductor processes to be quantified for semiconductor process optimization. Electrical parameters also help peripheral circuit designers and ESD engineers understand how to use the technology. ESD benchmarking can also provide discipline to the ESD design and development process, define design criteria, and develop ground rules. Establishing a set of test vehicles will allow other semiconductor process and device reliability disciplines (gate dielectrics, interconnects, latchup, soft error rate, etc.) to understand the implications of process and device optimization on ESD robustness.

2.4 Scope

These elemental building blocks are not intended to be ESD networks, but developmental structures to be used as a learning platform to characterize the ESD robustness of a CMOS technology. Application of these structures does not guarantee ESD robustness but will provide understanding of the technology and information to build ESD networks. Through this understanding, building reliability and quality into the design and technology can be achieved in a more disciplined fashion.

This document is intended to be used by semiconductor device and process engineers, ESD reliability engineers, and circuit designers. The structures can be used to compare ESD robustness to other semiconductor disciplines, such as latchup, hot electrons, electromigration, and MOSFET analysis for the optimization and understanding of various semiconductor processes.

3 IMPLEMENTATION STRATEGY

The strategy for establishing standardized ESD test structures has been deliberately constructed in a bottom-up approach. Device elements, rather than full ESD circuits, are most appropriate for comparing one process to another, whether it be a new smaller geometry technology being compared to a mature technology, the transfer of a technology to a new fab, or the beginnings of a foundry relationship. Critical ESD metrics can be measured on the device elements as a function of geometry. The geometrical information allows the devices to be scaled appropriately to full protection-level circuits.

3.1 Structure Strategy

The structures incorporated into the ESD technology benchmarking strategy consist of elements used in peripheral circuits, parasitics, and ESD devices themselves. These elements can be thought of as building blocks that can be placed in more complicated circuits and circuitry. Understanding the behavior of ESD and parasitic circuit elements at the device level is key to building a robust peripheral circuit.

Because of variations in device performance with geometry, a matrix of test structure dimensions has been given for every device. The list of geometrical parameters is meant to cover the known physical effects on ESD performance for each structure. Using these parameters, it should be possible to discover a device’s optimal geometry. For a full study of the structure, more geometry variations are certainly possible. For structures of minimal interest, nominal parameters are given.

3.2 ESD Metrics

To quantify and comparatively analyze ESD test structures, ESD metrics must be defined. To analyze the ESD robustness of specific elements, the structure definition, matrix, and design are intended to provide ESD metrics of value. ESD metric objectives will be discussed in the description and definition of individual structures.

3.3 Scaling

In this test structure implementation, ESD device elements are deliberately scaled to be narrower than required for full circuit protection. This is because most generally available test equipment, such as parameter analyzers, may not be able to force as much current as found in an ESD event. Variations in test structure layout parameters have been included to measure the scaling of the structure's robustness as a function of width.

3.4 Testing

To quantify and comparatively analyze ESD metrics of semiconductor chips, test procedures and failure criteria must be defined.

3.5 ESD Module Configuration Philosophy

Module layout rules (e.g., pad configurations, bussing, wiring, etc.) are given to avoid problems when implementing in specific corporations, laboratories, or test houses. Guidelines are provided to avoid the module definition from influencing the ESD results of the test structures.

3.6 Assumptions

The test structures are defined with the following assumptions:

- Structures are based on standard ESD protection elements in CMOS technology. The structures may be used in other technologies, such as SOI, SiGe, BiCMOS, RF-CMOS, but they do not include new vehicles or structures based on the customization of any specific technology.
- Structures are targeted at p-substrate epi or bulk CMOS. Local substrate plugs contained in some structures are not necessary for epi processes if a low resistance substrate plug is contacted elsewhere.
- The structures are intended to cover both salicided and non-salicided junction technologies. Variations occur when salicide affects test structure geometry.
- The structures assume aluminum or other low resistivity (< 0.1 Ω/square) based first- and second-level metal (Metal 1 and Metal 2, respectively). For other metal schemes, the configuration of metal to the structures should be altered to avoid metal burnout during testing.

3.7 Definitions and Conventions Used in This Document

A,b Dimensions are indicated in drawings by upper or lower case letters. Upper case letters signify parameters that are varied to determine their influence on electrical performance. Lower case letters signify parameters that remain fixed across structure variations.

Lmin The minimum drawn dimension of the MOSFET channel length in the CMOS fabrication process.

mdr Minimum design rule. According to a given technology definition, this is the minimum allowed spacing or enclosure for two layers.

4 ESD BENCHMARK STRUCTURES: RESISTOR BENCHMARK STRUCTURES

Resistor benchmark structures are defined to evaluate the ESD robustness of resistor elements used in peripheral circuits and in ESD protection circuits. The structures of interest are salicided and non-salicided P+ and N+, polysilicon, and N-well resistors.

Some measurements of interest from these structures are as follows:

- Power-to-failure versus pulse width, P_f
- Current-to-failure versus pulse width, I_f
- Velocity saturation current magnitude, J_{sat}
- Avalanche voltage (Volts), V_{av}
- Diodic characteristics (diode turn-on and series resistance)
- DC and Pulsed I-V characteristics

Power-to-failure of the resistor and critical current-to-failure provide insight into the ESD robustness of the resistor structure. Velocity saturation determines the linear and high resistance region of the resistor structure. Avalanche voltage determines the voltage at which the voltage across the resistor leads to avalanche breakdown. The diode characteristics such as the forward bias voltage and series resistance determine its conduction ability in a forward bias mode of operation. For the DC measurement, a low current is used to prevent heating effects. The low current R determines the nominal process resistance. The pulsed I-V measurements are used to observe the characteristics of the resistor under the high stress conditions typical of an ESD event.

The dimensional parameter of most interest is the length dependence of the resistor.

4.1 N-Well Resistor Structure

N-well resistors are used in peripheral circuitry for resistor ballasting, diodes, and impedance elements. Wiring is done with the first level metal.

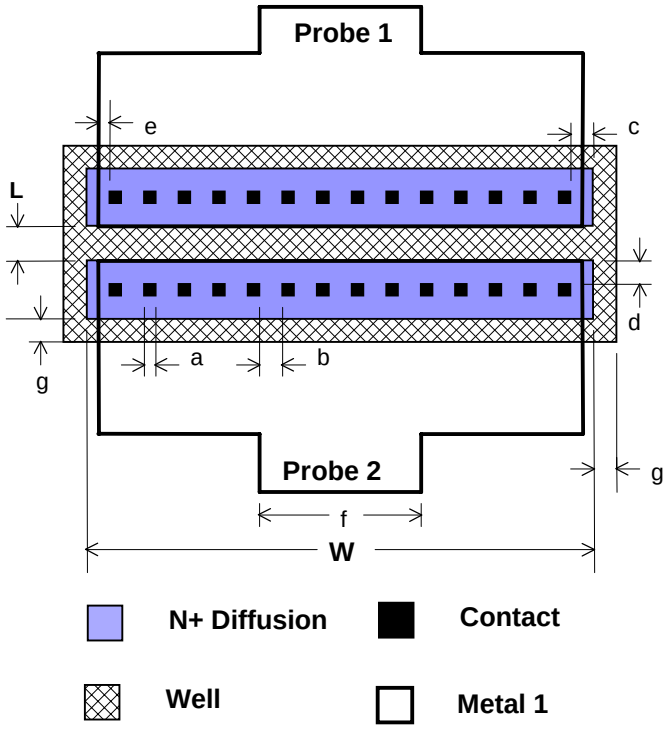

Figure 1 Well Resistor Construction

Table 1 Well Resistor Table of Layout Parameters

Variables	Description of Layout Variables	Ranges of Layout Variables
a	N+ contact width	mdr
b	N+ contact to contact spacing	mdr
c	N+ contact to lateral edge of N+ diffusion	2 x mdr
d	N+ contact to back/front diffusion edge	2 x mdr
e	M1 metal extension beyond contact	mdr
f	Minimum metal interconnect width	25 µm
g	N-well extension beyond N+ diffusion	mdr
L	N+ to N+ diffusion spacing	See Table 2
W	N+ diffusion width	See Table 2

Table 2 Matrix of Variable Parameters for Well Resistor

Name	W (µm)	L (µm)
NWRES_1	25	1.00
NWRES_1A	25	1.25
NWRES_1B	25	1.50
NWRES_1C	25	1.75
NWRES_1D	25	2.00
NWRES_2	50	1.00
NWRES_3	75	1.00

4.2 N+ Diffusion Resistor Structure

N+ diffusion resistors are used in peripheral circuitry for resistor ballasting, diodes, and impedance elements. These are used with salicide and with salicide block masks. When there is no salicide block mask, the length of the resistor is defined from input and output contact spacing (i.e., Probe 1 and Probe 2). For a salicide block mask, the length of the resistor is defined from the length of the mask itself.

In a non-silicide process, use Figure 2 to define the resistor layout.

4.2.1 N+ Diffusion Resistor with No Silicide Block

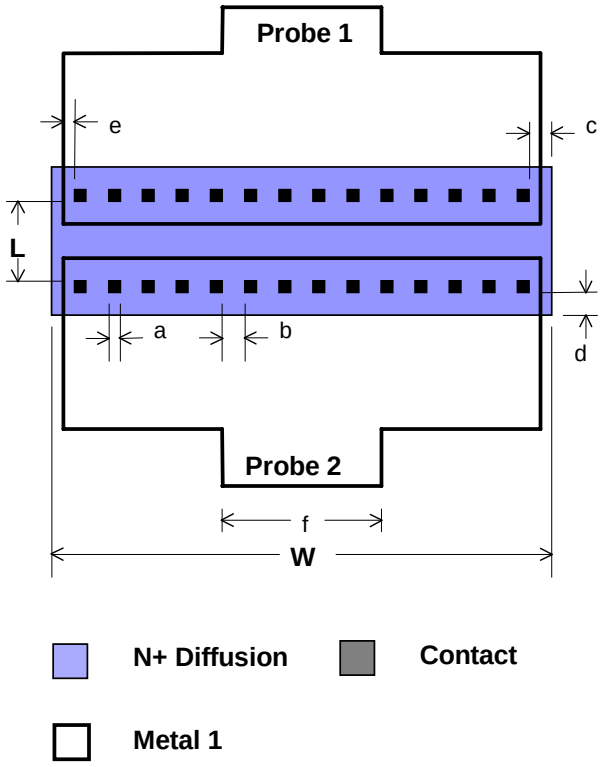

Figure 2 N+ Diffusion Resistor (No Silicide Block)

Table 3 N+ Diffusion Resistor (No Silicide Block) Table of Layout Parameters

Variables	Description of Layout Variables	Ranges of Layout Variables
a	N+ contact width	mdr
b	N+ contact to contact spacing	mdr
c	N+ contact to lateral side of N+ diffusion edge	2 x mdr
d	N+ contact to back diffusion edge	2 x mdr
e	M1 metal extension beyond contact	2 x mdr
f	Min. metal interconnect width	25 µm
L	Contact to contact spacing	See Table 4
W	N+ diffusion width	See Table 4

Table 4 Matrix of Variable Parameters for N+ Diffusion Resistor Without Silicide Block

Name	W (µm)	L (µm)
SNDRES_1	25	1.00
SNDES_1A	25	1.25
SNDES_1B	25	1.50
SNDES_1C	25	1.75
SNDES_1D	25	2.00
SNDES_2	50	1.00

4.2.2 N+ Diffusion Resistor with Silicide Block

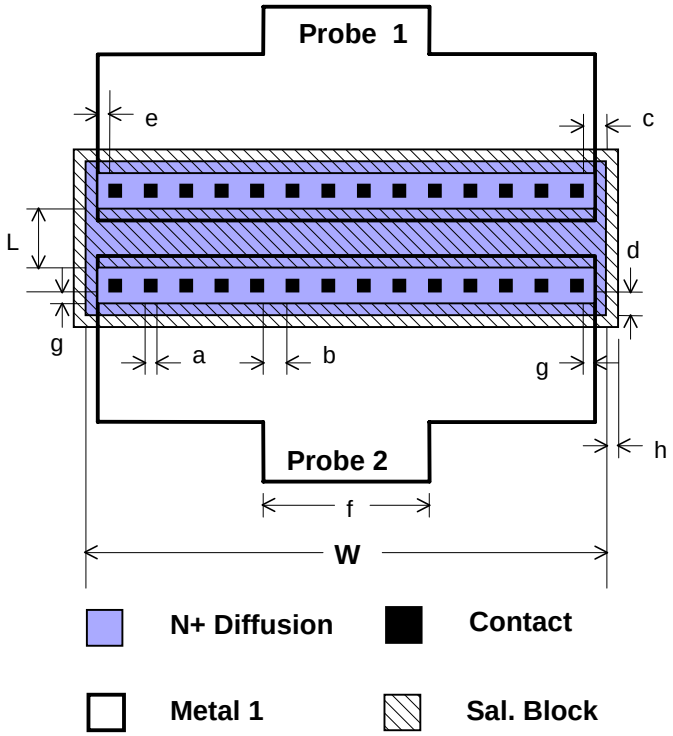

Figure 3 N+ Diffusion Resistor with Silicide Block

Table 5 N+ Diffusion Resistor (with Silicide Block) Table of Layout Parameters

Variables	Description of Layout Variables	Ranges of Layout Variables
a	N+ contact width	mdr
b	N+ contact to contact spacing	mdr
c	N+ contact to lateral side of N+ diffusion edge	2 x mdr
d	N+ contact to back diffusion edge	2 x mdr
e	M1 metal extension beyond contact	mdr
f	Min. metal interconnect width	25 µm
g	Salicide block opening space around contact	mdr
h	Salicide block mask extension beyond diffusion	mdr
L	Salicide block opening edge to salicide block opening edge	See Table 5
W	N+ diffusion width	See Table 5

Note: The salicide block mask can also be a simple rectangle of length L and a width which extends h µm beyond the diffusion width boundaries.

Table 6 Matrix of Variable Parameters for N+ Diffusion Resistor (With and Without Silicide Block)

Name	W (µm)	L (µm)
NDRES_1	25	1.00
NDRES_1A	25	1.25
NDRES_1B	25	1.50
NDRES_1C	25	1.75
NDRES_1D	25	2.00
NDRES_2	50	1.00
NDRES_3	75	1.00

4.3 Polysilicon Resistor

Polysilicon resistors are used in peripheral circuitry for impedance elements. These structures may or may not be silicided. The resistance is specified for a fixed width. The polysilicon sheet resistance defines the length.

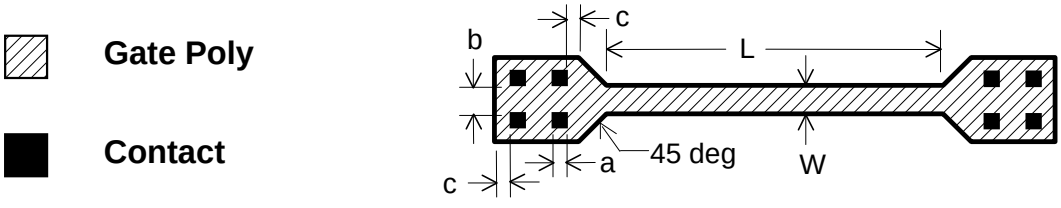

Figure 4 Polysilicon Resistor

Table 7 Polysilicon Resistor Table of Layout Parameters

Variables	Description of Layout Variables	Ranges of Layout Variables
a	Poly contact width	mdr
b	Poly contact to contact spacing distance	mdr
c	Poly contact to poly edge	mdr
L	Poly length measured from end of chamfer taper to other end of chamfer	See Table 7
W	Poly width	See Table 7

Notes:
1. Metal 1 placement on contacts at each end is non-critical. M1 is assumed to be low resistivity (<0.1 Ω/square) and total metal resistance << poly resistance.
2. Resistor length depends on poly sheet resistance.
3. Silicided resistors can be zigzagged due to required length.
4. Polysilicon end design: Number of contacts = 4.
5. Polysilicon end design: Chamfer inside corners.

Table 8 Matrix of Variable Parameters for Polysilicon Resistor

Name	W (µm)	R (W)	Technology
POLYRES_1	1	75	silicided
POLYRES_1A	1	150	silicided
POLYRES_2	2	75	silicided
POLYRES_2A	2	150	silicided
POLYRES_3	2	75	non-silicided
POLYRES_3A	2	150	non-silicided
POLYRES_4	4	75	non-silicided
POLYRES_4A	4	150	non-silicided

5 DIODE BENCHMARK STRUCTURES

Diodes are used as ESD protection circuits in peripheral circuits. Analyzing diodes is important in understanding the ESD robustness. The following structures are included to evaluate diodes:

- P+/N-well diodes with 1-, 2-, and 3-finger variations
- N+/substrate diodes
- N-well/substrate diodes

P+ diodes are used in single diode and diode string configurations for an ESD network to the V_{DD} power supply. N+ and N-well diodes are used in single diode configuration for an ESD network to the V_{SS} power supply. These elements are also contained inherently in p- and n-channel MOSFETS.

Some measurements of interest from these structures are as follows:

- Power-to-failure versus pulse width
- Current-to-failure versus pulse width
- ESD metric of volts/µm of diode perimeter
- ESD metric of amps/µm of diode perimeter
- Forward bias voltage
- On-resistance, R_{on}
- Reverse breakdown voltage, V_{br}
- Pulsed I-V curve
- Pulsed and DC PNP characteristics for P+ to N-well diodes on p substrate (e.g., β(Ic), Vbe(Ie))

5.1 Single Finger P+ Diode

Single finger P+ diodes are used in single diode and diode string configurations for ESD networks to the V_{DD} power supply, between power supplies, and in other applications. P+ diodes are also contained inherently in p-channel MOSFETs.

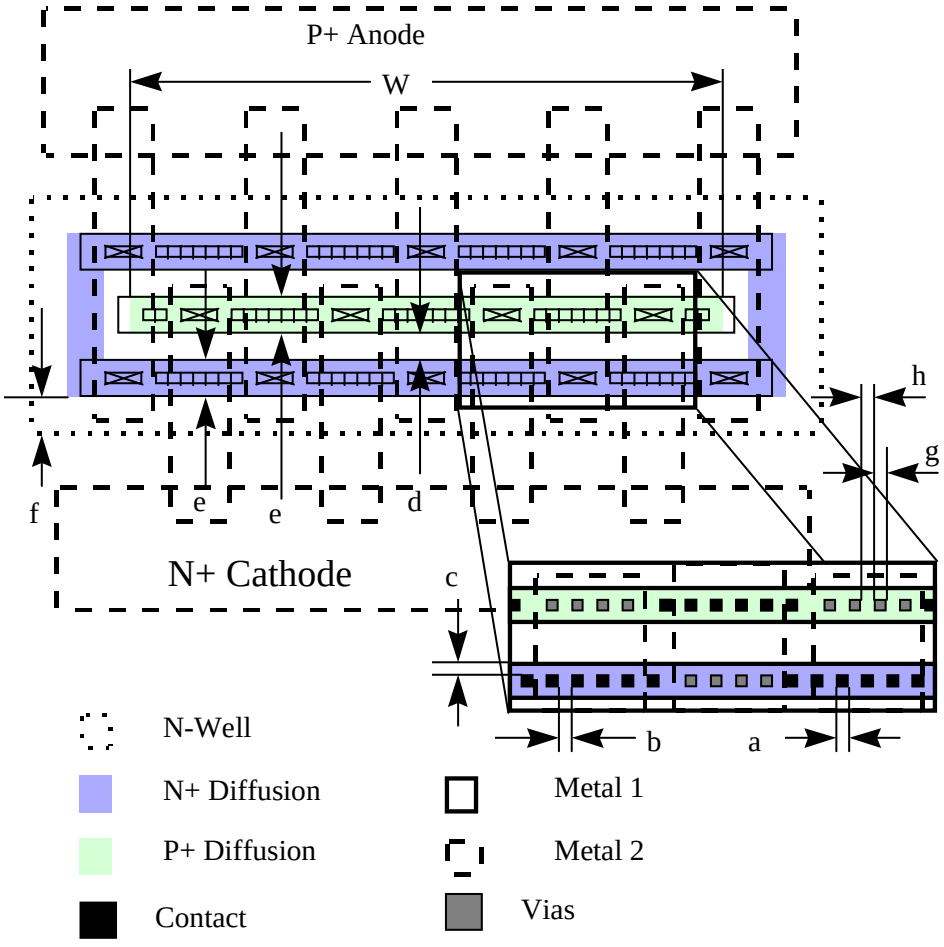

Figure 5 Single Finger P+ to N-Well Diode

Table 9 Layout Parameters for Single Finger P+ to N-Well Diode

Variable	Description of Layout Variable	Range of Layout Variable
a	N+ and P+ contact width	mdr
b	Contact to contact space	mdr
c	Contact to diffusion edge	mdr
d	N+ to P+ separation	mdr
e	N+ and P+ diffusion heights	a+2c
f	N+ inside N-well	mdr
g	Via size	mdr
h	Via to via space	mdr
W	Width of N+ and P+ diffusions	See Table 8

Notes:
1. Metal 2 to Metal 1 vias over N+ and P+ diffusions should have 4 vias per Metal 2 finger at mdr.
2. Stack vias and contacts to N+ and P+ diffusions if allowed by technology. Otherwise use maximum number of contacts which will fit between the groups of 4 vias.
3. Metal width from structure to bond pad greater than 25 µm.
4. Metal 1 height over N+, minimum width allowed by design rules
5. Metal 1 height over P+, maximum allowed by design rules consistent with M1-M1 space
6. Number of M2 fingers shown is for illustration only. Maximum number of fingers of M2, consistent with the design rules and 4 vias per finger, should be used.

Table 10 Matrix of Variable Parameters for Single Finger P+ Diode

Name	W (µm)
PDIODE_1	50
PDIODE_1A	100
PDIODE_1B	150

5.2 Two-Finger P+ Diode

Two-finger P+ diodes are used in single diode and diode string configurations for ESD networks to the V_{DD} power supply, between power supplies, and in other applications

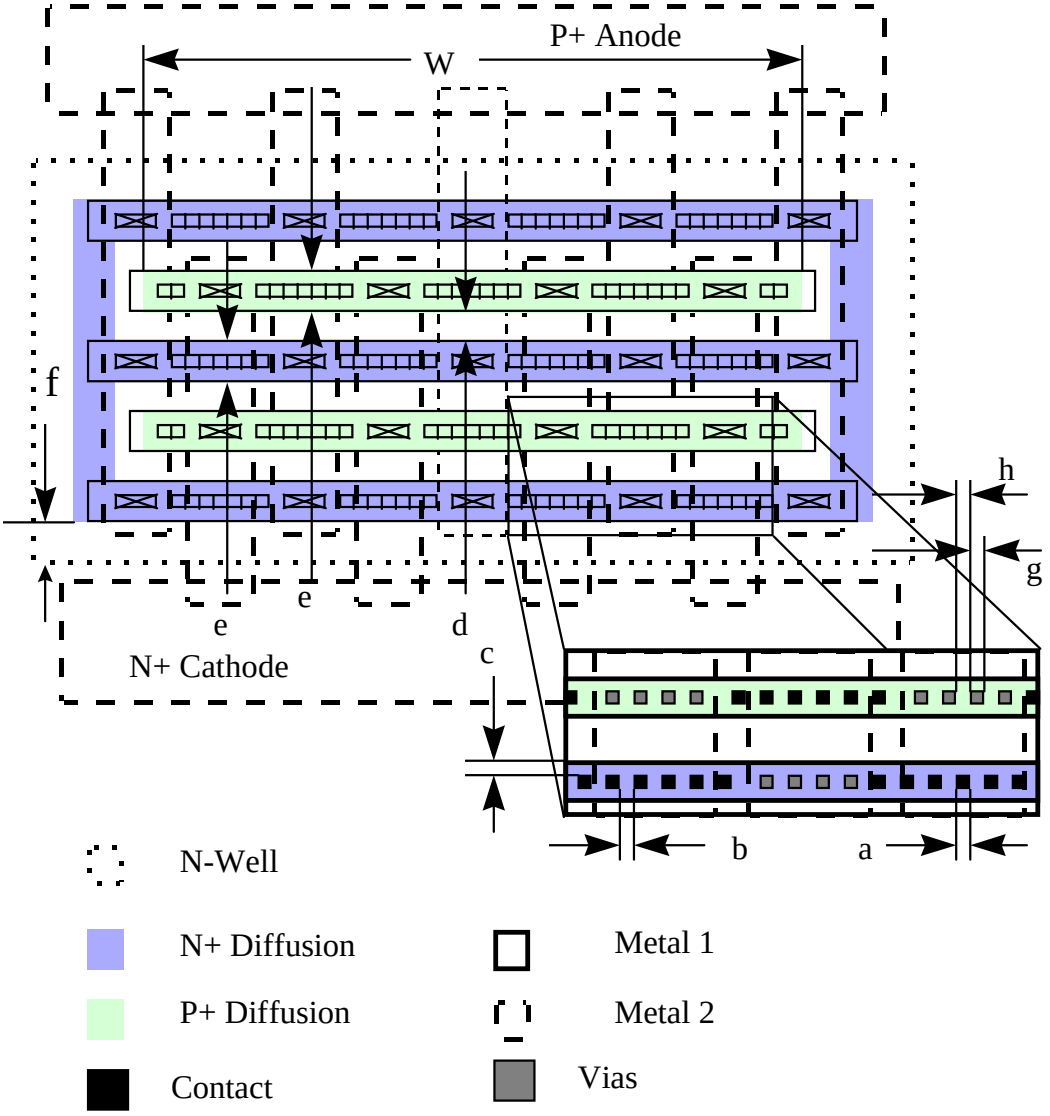

Figure 6 Two-Finger P+ to N-Well Diode

Table 11 Layout Parameters for Two-Finger P+ to N-Well Diode

Variable	Description of Layout Variable	Range of Layout Variable
a	N+ and P+ contact width	mdr
b	Contact to contact space	mdr
c	Contact to diffusion edge	mdr
d	N+ to P+ separation	mdr
e	N+ and P+ diffusion heights	a+2c
f	N+ inside N-well	mdr
g	Via size	mdr
h	Via to via space	mdr
W	Width of N+ and P+ diffusions	See Table 12

Notes:
1. Metal 2 to Metal 1 vias over N+ and P+ diffusions should have 4 vias per Metal 2 finger at mdr.
2. Stack vias and contacts to N+ and P+ diffusions if allowed by technology. Otherwise use maximum number of contacts which will fit between the groups of 4 vias.
3. Metal width from structure to bond pad greater than 25 µm.
4. Metal 1 height over N+, minimum width allowed by design rules.
5. Metal 1 height over P+, maximum allowed by design rules consistent with M1-M1 space.
6. Number of M2 fingers shown is for illustration only. Maximum number of fingers of M2 consistent with 4 via per finger should be used

Table 12 Matrix of Variable Parameters for Two-Finger P+ to N-Well Diode

Name	W(µm)
PDIODE_2	50

5.3 Three-Finger P+ Diode

Three-finger P+ diodes are used in single diode and diode string configurations for ESD networks to the V_{DD} power supply, between power supplies, and in other applications.

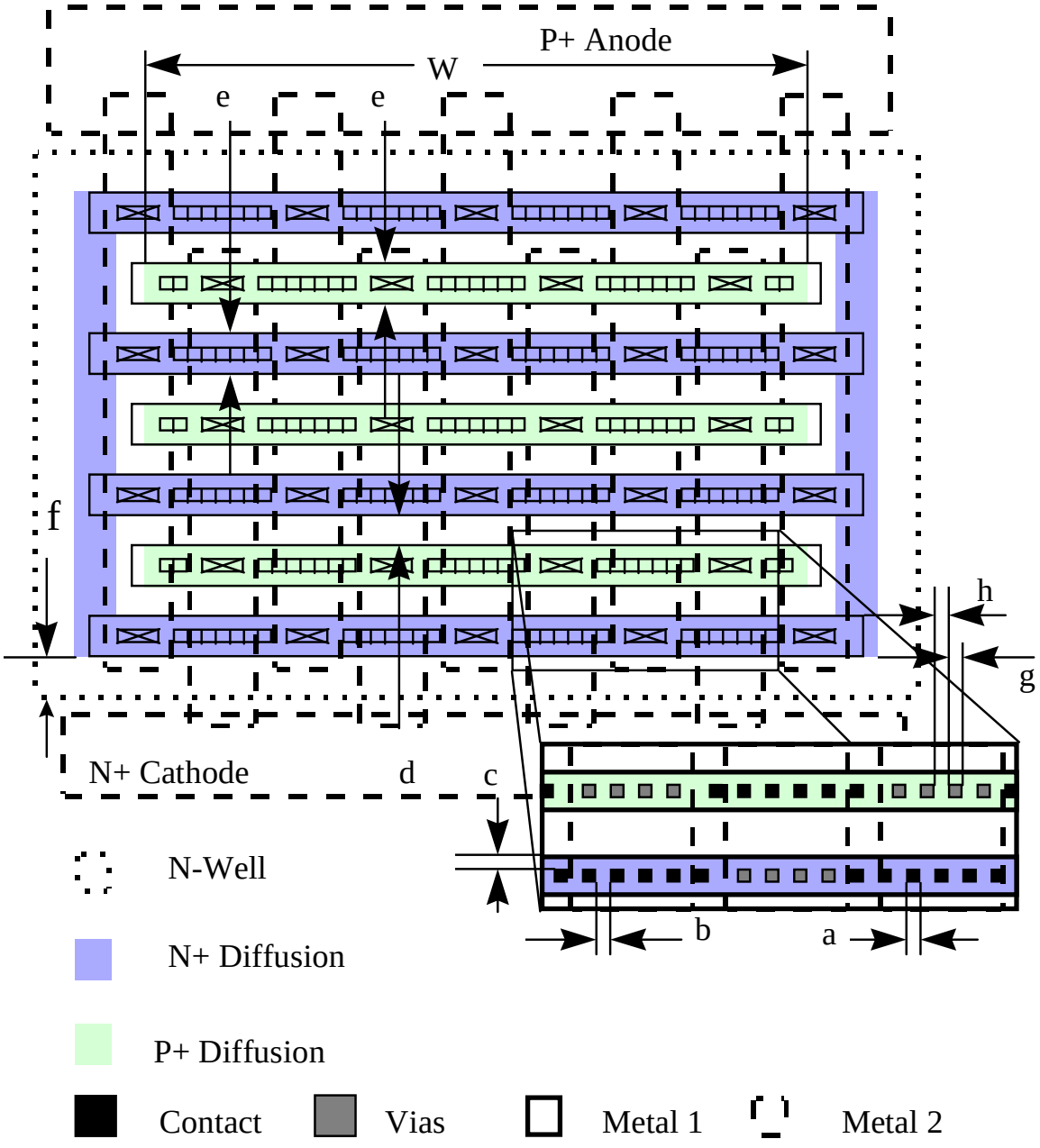

Figure 7 Three-Finger P+ to N-Well Diode

Table 13 Layout Parameters for P+ to N-Well Diode

Variable	Description of Layout Variable	Range of Layout Variable
a	N+ and P+ Contact Width	mdr
b	Contact to Contact Space	mdr
c	Contact to Diffusion Edge	mdr
d	N+ to P+ Separation	mdr
e	N+ and P+ Diffusion heights	a+2c
f	N+ inside N-well	mdr
g	Via size	mdr
h	Via to Via space	mdr
W	Width of N+ and P+ Diffusions	See Table 13

Notes:
1. Metal 2 to Metal 1 vias over N+ and P+ diffusions should have 4 vias per Metal 2 finger at mdr.
2. Stack vias and contacts to N+ and P+ diffusions if allowed by technology. Otherwise use maximum number of contacts which will fit between the groups of 4 vias.
3. Metal width from structure to bond pad greater than 25 µm.
4. Metal 1 height over N+, minimum width allowed by design rules.
5. Metal 1 height over P+, maximum allowed by design rules consistent with M1-M1 space.
6. Number of M2 fingers shown is for illustration only. Maximum number of fingers of M2 consistent with 4 via per finger should be used.

Table 14 Matrix of Variable Parameters for Three-Finger P+ to N-Well Diode

Name	W (µm)
PDIODE_2	50

5.4 N+ Diode Structure

N+ to substrate diodes are contained inherently in n-channel MOSFETS and can be placed explicitly. N+ diodes are used for ESD networks between pad and the VSS substrate and other applications. Understanding the N+ diode is essential to understanding the ESD robustness of a full I/O circuit. The structures shown in Figure 8 and Figure 9 are targeted to a p- on P+ epitaxial process. In an n- on N+ epitaxial process or a non-epitaxial (bulk) technology, the structures have N+ and P+ diffusions interchanged.

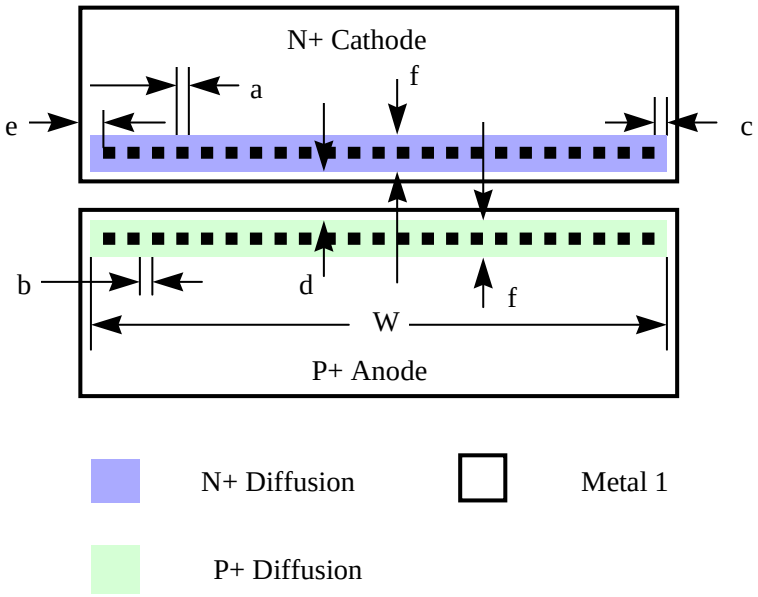

Figure 8 N+ to Substrate Diode

Table 15 Layout Parameters for N+ Diode to Substrate

Variable	Description of Layout Variable	Range of Layout Variable
a	N+ and P+ contact width	mdr
b	Contact to contact space	mdr
c	Contact to diffusion edge	mdr
d	N+ to P+ separation	mdr
e	Metal 1 extension beyond contact	mdr
f	N+ and P+ diffusion heights	a+2c
W	Width of N+ and P+ diffusions	See Table 15

Table 16 Matrix of Variable Parameters for N+ Diode to Substrate

Name	W (µm)
NDIODE_1	50
NDIODE_2	100
NDIODE_3	150

5.5 N-Well Diode Structure

N-well diodes are used for ESD networks between pad and the V_{SS} substrate. The N-well diode is also a parasitic of the N-well resistor.

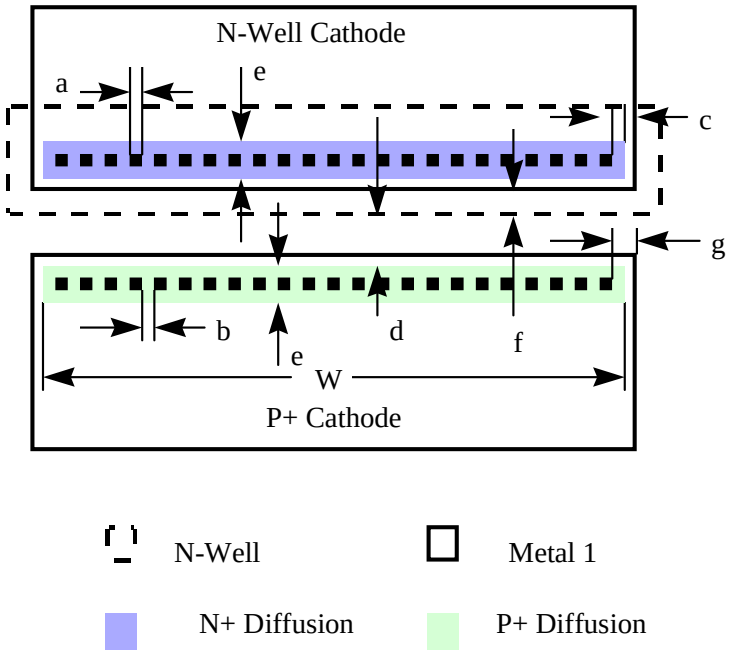

Figure 9 N-Well to Substrate Diode

Table 17 Layout Parameters for N-Well to Substrate Diode

Variable	Description of Layout Variable	Range of Layout Variable
a	N+ and P+ contact width	mdr
b	Contact to contact space	mdr
c	Contact to N+ and P+ diffusion edges	mdr
d	N-well to P+ edge	mdr
e	N+ and P+ diffusions heights	a+2c
f	N+ inside N-well	mdr
g	Metal overlap of contact	mdr
W	Width of N+ and P+ diffusions	See Table 17

Note: 1. Metal width from structure to bond pad greater than 25 µm

Table 18 Matrix of Variable Parameters for N-Well Diode

Name	W (µm)
NWELLDI_1	10
NWELLDI_2	20
NWELLDI_3	40

6 PARASITIC NPN BIPOLAR BENCHMARK STRUCTURES

Parasitic bipolar NPN elements are used as ESD protection circuits and are present in peripheral circuits. Parasitic NPN interactions occur in negative and positive ESD pulses causing ESD failure mechanisms. The following types of structures are defined:

- N-well to N-well structure
- N+ to N-well structure
- N+ to N+ structure

Some measurements of interest from these structures are as follows:

- Power-to-failure versus pulse width
- Current-to-failure versus pulse width
- ESD metric of volts/µm of layout width
- ESD metric of amps/µm of width
- Forward bias voltage
- On-resistance, R_{on}
- Reverse breakdown voltage, V_{br}

6.1 Non-Gated Thick Oxide Well-Well Device/Parasitic

Thick oxide well-to-well devices are important for ESD analysis because of their use as an ESD device as well as a parasitic element. For example, well-to-well devices are used as punch-through ESD device, and are present in thick oxide triggered silicon controlled rectifiers. These also represent the parasitic between an N-well diode and an adjacent guard ring structure. The thick oxide well-to-well benchmark structure is shown in Figure 14. The thick oxide well-to-well structure has the following design characteristics.

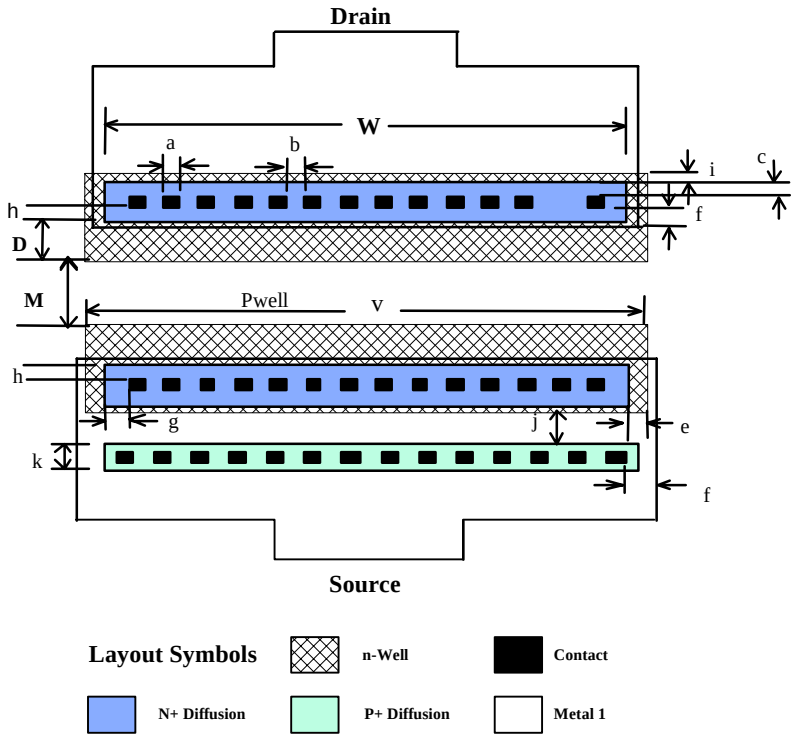

Figure 10 Non-Gated Thick Oxide Well-Well Device

Table 19 Layout Parameters for Thick Oxide Well-Well Device

Variables	Description of Layout Variables	Ranges of Layout Variables
a	N+ and P+ contacts width	mdr
b	N+ and P+ contacts to contact spacing distance	mdr
c	N+ and P+ contacts to back side N+/P+ diffusion edge	mdr
D	N+ diffusion edge distance to front side edge of N-well	See Table 19
e	N+ diffusion edge distance to lateral side edge of N-well	mdr
f	Metal 1 overlap of contact	mdr
g	N+ and P+ contacts to lateral side of N+/P+ diffusion edge	mdr
h	N+ and P+ contacts to front side of N+/P+ diffusion edge	mdr
I	N+ diffusion edge distance to back side edge of N-well	mdr
j	N+ diffusion spacing to P+ diffusion spacing	mdr
k	P+ and N+ diffusions heights	a+2c
M	N-well spacing to N-well	See Table 19
v	N-well widths	W+2e
W	N+ and P+ diffusion widths	See Table 19

Notes: 1. M1 Width greater than 25 µm.

Table 20 Variable Parameters for N-Well to N-Well Structure (Gated and Non-Gated)

Name	W (µm)	M	D
NWNW_1	25	mdr	mdr
NWNW_1A	25	2 x mdr	mdr
NWNW_1B	25	3 x mdr	mdr
NWNW_1C	25	mdr	mdr + 1 µm
NWNW_1D	25	mdr	mdr + 2 µm
NWNW_2	50	mdr	mdr
NWNW_3	75	mdr	mdr

6.2 Gated Thick Oxide Well-Well Device/Parasitic

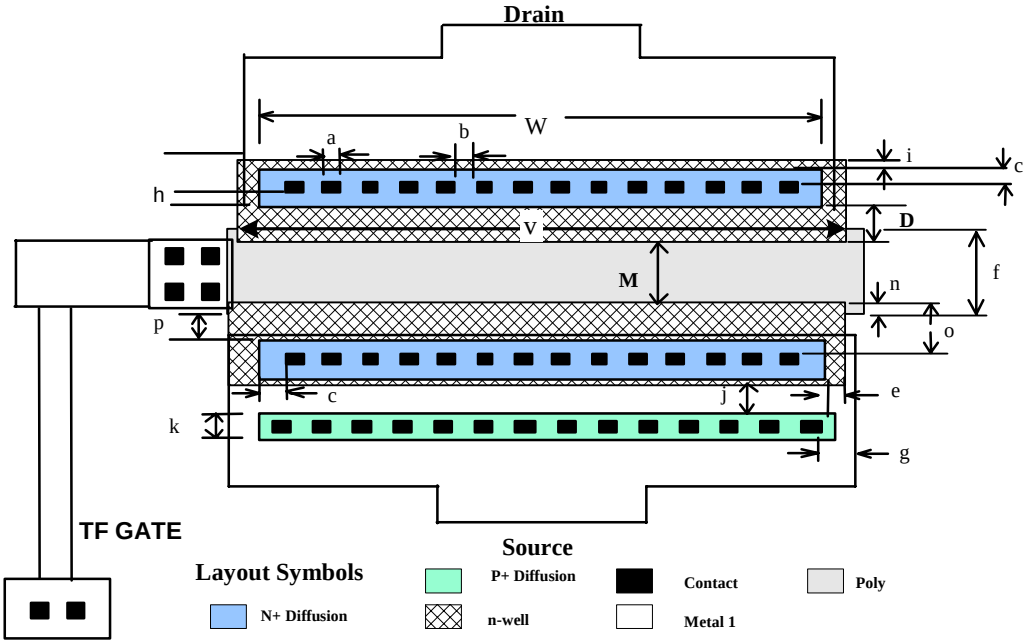

Figure 11 Gated Thick Oxide Well-Well Device

Table 21 Layout Parameters for Gated Thick Oxide Well-Well Device

Variable	Description of Layout Variables	Ranges of Layout Variables
a	N+ and P+ contacts widths	mdr
b	N+ and P+ contacts to contact spacing distance	mdr
c	N+ and P+ contacts to N+/P+ diffusion edge	mdr
D	N+ diffusion edge distance to front side edge of N-well	See Table 21
e	N+ diffusion edge distance to lateral side edge of N-well	mdr
f	Poly length	M+2n
g	Metal 1 overlap of contact	mdr
h	N+ and P+ contacts to front side of N+/P+ diffusion edge	mdr
i	N+ diffusion edge distance to back side edge of N-well	mdr
j	N+ diffusion spacing to P+ diffusion spacing	mdr
k	P+ and N+ diffusions heights	a+2c
M	N-well spacing to N-well	See Table 21
n	Poly overlap on N-well	0.5 µm
o	Contact to edge of forward N-well edge	p + h
p	N+ diffusion edge distance to poly	D – n
v	N-well width	W+2e
W	N+ and P+ diffusion widths	See Table 21

Table 22 Variable Parameters for N-Well to N-Well Structure (Gated and Non-Gated)

Name	W (µm)	M	D
NWNWG_1	25	mdr	mdr
NWNWG_1A	25	2 x mdr	mdr
NWNWG_1B	25	3 x mdr	mdr
NWNWG_1C	25	mdr	mdr + 1 µm
NWNWG_1D	25	mdr	mdr + 2 µm
NWNWG_2	50	mdr	mdr
NWNWG_3	75	mdr	mdr

6.3 Non-Gated Thick Oxide N+ to N-Well Device/Parasitic

Thick oxide N-well to N+ devices are important for ESD analysis because of its use as an ESD device as well as a parasitic element. For example, N+ to N-well devices are used as punch through ESD devices, and are present in thick oxide triggered silicon controlled rectifiers. These also represent the parasitic between an N+ MOSFET drain and an adjacent guard ring structure.

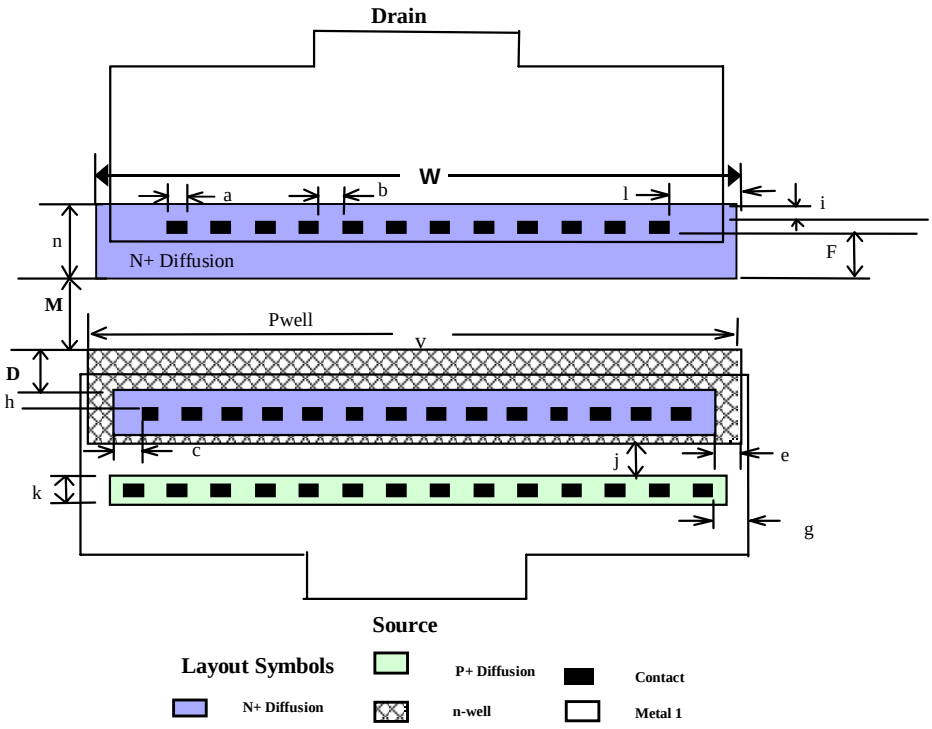

Figure 12 Non-Gated Thick Oxide N+ to N-Well Device

Table 23 Layout Parameters for Thick Oxide N+ to N-Well Device

Variable	Description of Layout Variables	Ranges of Layout Variables
a	N+ and P+ contacts widths	mdr
b	N+ and P+ contacts to contact spacing distance	mdr
c	N+ and P+ contacts to lateral side N+/P+ diffusion edge	mdr
D	N+ diffusion edge distance to front side edge of N-well	See Table 23
e	N+ diffusion edge distance to lateral side edge of N-well	mdr
F	N+ contact distance to front edge of N+ diffusion	See Table 23
g	Metal 1 overlap of contact	mdr
h	N+ and P+ contacts to front side of N+/P+ diffusion edge	mdr
i	N+ and P+ contacts to back side N+ diffusion edge	mdr
j	N+ diffusion spacing to P+ diffusion spacing	mdr
k	P+ and N+ ground diffusion heights	a+2c
l	Last N+ contact to N+ diffusion edge (See note below)	3X mdr
M	N+ diffusion spacing to N-well	See Table 23
n	Drain N+ diffusion heights	a + i + F
v	N-well widths	W+2e
W	N+ and P+ diffusion widths	See Table 23

Notes: 1. M1 width greater than 25 µm.
2. Chamfer corners not required, use 3X mdr for last N+ contacts at each end of the diffusion.

Table 24 Matrix of Variable Parameters for the N+ to N-Well Structure (Gated and Non-Gated)

Name	W (µm)	M	D	F
NWN_1	25	mdr	2X mdr	mdr
NWN_1A	25	1.5 x mdr	2X mdr	mdr
NWN_1B	25	2 x mdr	2X mdr	mdr
NWN_1C	**25**	mdr	4X mdr	mdr
NWN_1D	25	mdr	6X mdr	mdr
NWN_1E	25	mdr	2X mdr	mdr + 2 µm
NWN_1F	25	mdr	2X mdr	mdr + 4 µm
NWN_2	50	mdr	2 x mdr	mdr
NWN_3	75	mdr	2 x mdr	mdr

6.4 Gated Thick Oxide N+ to N-Well Device/Parasitic

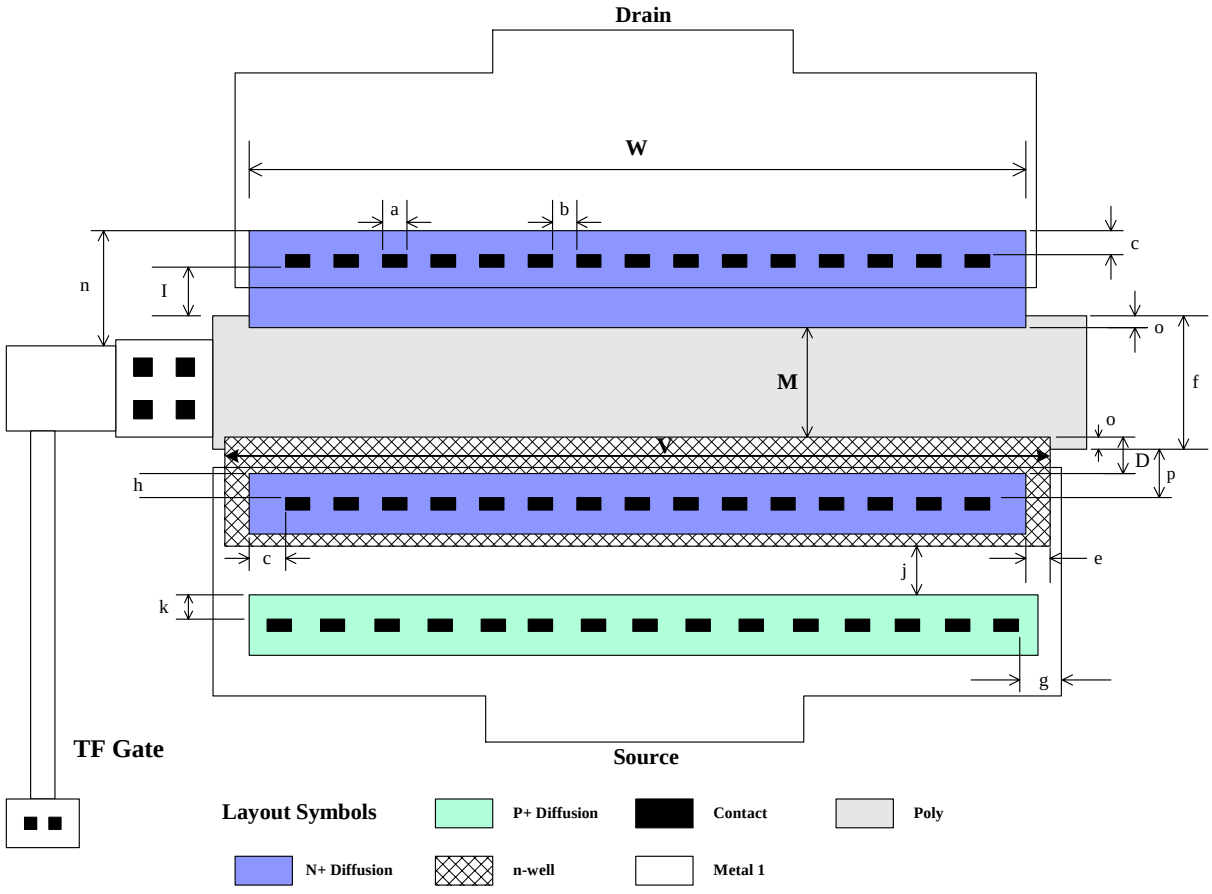

Figure 13 Gated Thick Oxide N+ to N-Well Device

Table 25 Layout Parameters for N+ to N-Well Device

Variable	Description of Layout Variables	Ranges of Layout Variables
a	N+ and P+ contacts widths	mdr
b	N+ and P+ contacts to contact spacing distance	mdr
c	Source N+ /P+ contacts to diffusion edge	mdr
D	N+ diffusion edge distance to front side edge of N-well	See Table 25
e	N+ diffusion edge distance to lateral side edge of N-well	mdr
f	Poly length	M+2n
g	Metal 1 overlap of contact	mdr
h	N+ and P+ contacts to front side of N+/P+ diffusion edge	mdr
I	N+ drain contact to edge of poly	See Table 25
j	N+ diffusion spacing to P+ diffusion spacing	mdr
k	P+ and N+ ground diffusion heights	a + 2c
M	N+ spacing to N-well	See Table 25
n	Drain N+ diffusion heights	a + c+ i
o	Poly overlap on N-well/N+ diffusion	0.5 µm
p	Contact to edge of forward N-well edge	h + c + n
v	N-well lengths	W + 2e
W	N+ and P+ diffusion lengths	See Table 25

Table 26 Variable Parameters for N-Well to N-Well Structure (Gated and Non-Gated)

Name	W (µm)	M	D	I
NWNG_1	25	mdr	mdr	mdr
NWNG_1A	25	2X mdr	mdr	mdr
NWNG_1B	25	3X mdr	mdr	mdr
NWNG_1C	25	mdr	mdr + 1 µm	mdr
NWNG_1D	25	mdr	mdr + 2 µm	mdr
NWNG_1E	25	mdr	mdr	mdr + 1 µm
NWNG_1F	25	mdr	mdr	mdr + 2 µm
NWNG_2	50	mdr	mdr	mdr
NWNG_3	75	mdr	mdr	mdr

6.5 Non-Gated Thick Oxide N+ to N+ Device/Parasitic

Thick oxide N+ to N+ devices are important for ESD analysis because of their use as an ESD device as well as a parasitic element. For example, N+ to N+ devices are used as punch-through ESD devices and are present in thick oxide triggered silicon controlled rectifiers. These also represent the parasitic between an N+ MOSFET drain and an adjacent N+ shape. The thick oxide N-to-N benchmark structure is shown in Figure 16. The thick N+ to N+ structure has the following design characteristics.

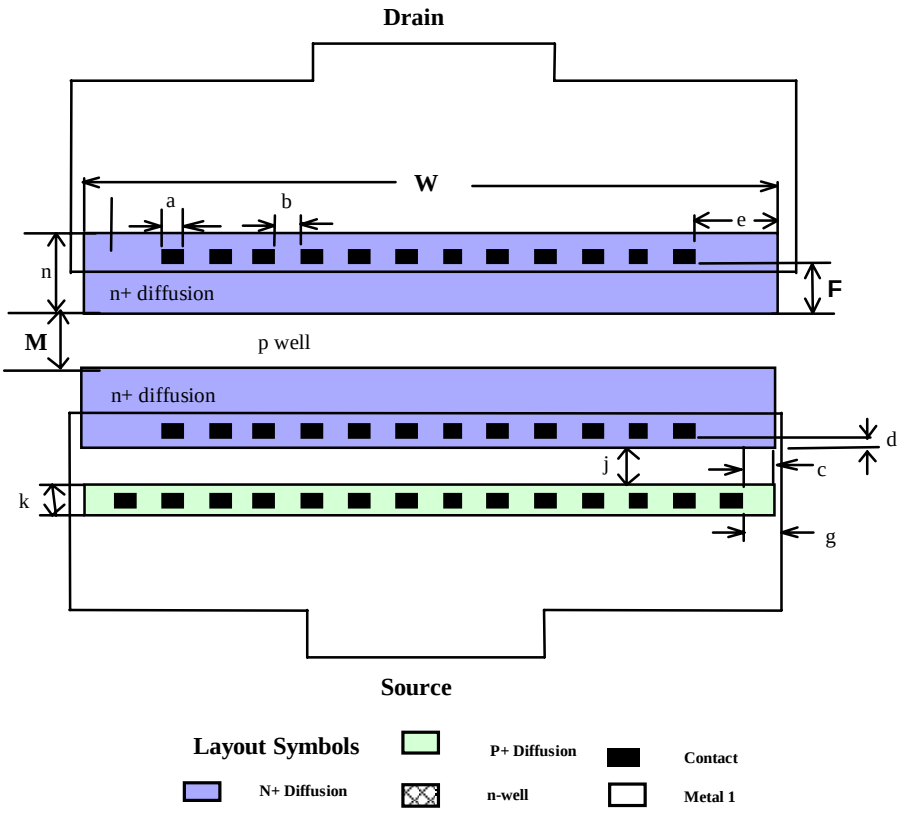

Figure 14 Thick Oxide N+ to N+ Structure

Table 27 Layout Parameters for Thick Oxide N+ to N+ Structure

Variable	Description of Layout Variables	Ranges of Layout Variables
a	N+ and P+ contacts widths	mdr
b	N+ and P+ contacts to contact spacing distance	mdr
c	P+ contacts to lateral side P+ diffusion edge	mdr
d	N+ and P+ contacts to back side N+ diffusion edge	2X mdr
e	N+ contacts to lateral side N+ diffusion edge (note 2)	3X mdr
F	N+ contact distance to front edge of N+ diffusion	See Table 27
g	Metal 1 overlap of P+ contact	mdr
h	Metal 1 overlap of N+ contact	a + b + g
j	N+ diffusion spacing to P+ diffusion spacing	mdr
k	P+ ground diffusion heights	mdr
M	N+ spacing to N-well	See Table 27
n	N+ diffusion heights	a + d + F
W	N+ and P+ diffusion widths	See Table 27

Notes: 1. M1 width greater than 25 µm.
2. Chamfer corners not required, use 3X mdr for last N+ contacts at each end of the diffusion.

Table 28 Matrix of Variable Parameters for the Thick Oxide N+ to N+ Structure (Gated and Non-Gated)

Name	W (µm)	M	F
NN_1	25	mdr	2 x mdr
NN_1A	25	1.5X mdr	2 x mdr
NN_1B	25	2X mdr	2 x mdr
NN_1C	25	mdr	4 x mdr
NN_1D	25	mdr	6 x mdr
NN_2	50	mdr	2 x mdr
NN_3	75	mdr	2 x mdr

6.6 Gated Thick Oxide N+ to N+ Device/Parasitic

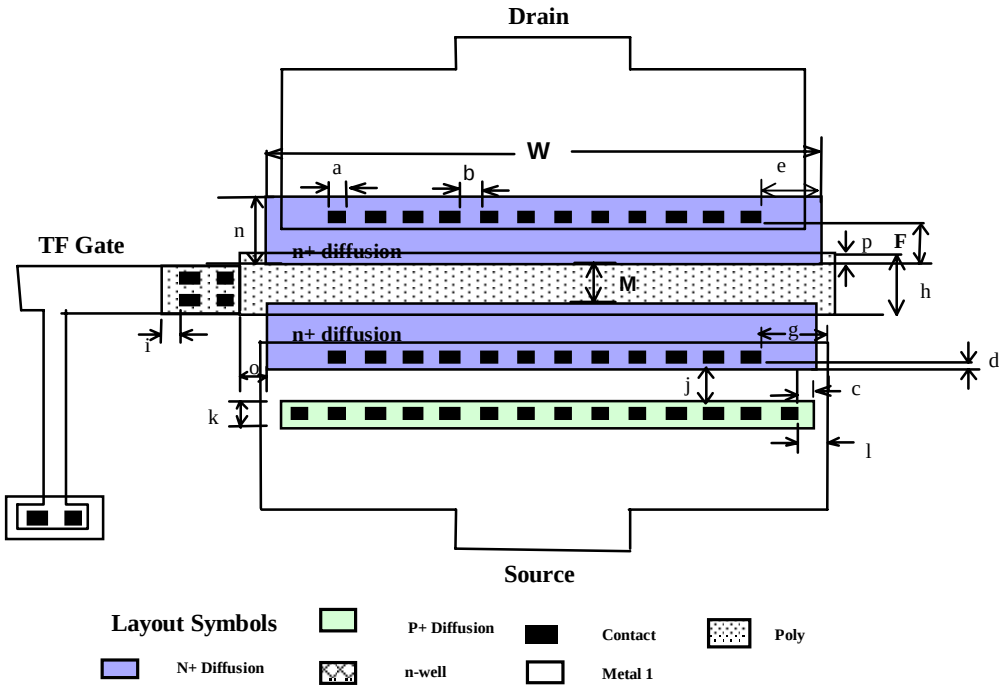

Figure 15 Gated Thick Oxide N+ to N+ Structure

Table 29 Layout Parameters for Gated Thick Oxide N+ to N+ Structure

Variable	Description of Layout Variables	Ranges of Layout Variables
a	N+ and P+ contacts widths	mdr
b	N+ and P+ contacts to contact spacing distance	mdr
c	P+ contacts to lateral side P+ diffusion edge	mdr
d	N+ and P+ contacts to back side N+ diffusion edge	2X mdr
e	N+ contacts to lateral side N+ diffusion edge	3X mdr
F	N+ contact distance to front edge of N+ diffusion	See Table 29
g	Metal 1 overlap of N+ contact	a + b + e
h	Poly length	M + 2p
i	Contact to edge of poly	mdr
j	N+ diffusion spacing to P+ diffusion spacing	mdr
k	P+ ground diffusion heights	a + 2c
l	Metal 1 overlap of P+ contact	mdr
M	N+ - N+ spacing distance	See Table 29
n	N+ diffusion heights	a + d + f
o	Poly overlap of N+ diffusion	mdr
p	Poly overlap of N+ drain source diffusions	mdr
W	N+ and P+ diffusion lengths	See Table 29

Table 30 Matrix of Variable Parameters for the Thick Oxide N+ to N+ Structure (Gated and Non-Gated)

Name	W (µm)	M	F
GNN_1	25	mdr	2 x mdr
GNN_1A	25	1.5X mdr	2 x mdr
GNN_1B	25	2X mdr	2 x mdr
GNN_1C	25	mdr	4 x mdr
GNN_1D	25	mdr	6 x mdr
GNN_2	50	mdr	2 x mdr
GNN_3	75	mdr	2 x mdr

7 MOSFET BENCHMARK STRUCTURES

MOSFET transistors are used as ESD protection circuits in peripheral circuits. Analyzing MOSFETs is important in understanding ESD robustness. The following structures are included to evaluate the MOSFET:

- Single finger N-channel MOSFET
- Multiple-finger N-channel MOSFET
- MOSFETs with integrated N-well resistors
- Single finger P-channel MOSFET
- Multiple-finger P-channel MOSFET
- P-channel MOSFETs with local well taps

The measurements of interest from these structures are as follows:

- DC and pulsed I-V curves to measure the following parameters:
  - First trigger voltage, V_{t1}
  - First trigger current, I_{t1}
  - Snapback on resistance, R_{on}
  - Second trigger voltage, V_{t2}
  - Second trigger current, I_{t2}
- ESD metric of volts/µm of MOSFET device width
- Power-to-failure versus pulse width, P_f
- Current-to-failure versus pulse width, I_f
- Diode series resistance, R_{diode}
- Snapback Voltage, Vsb
- Holding Voltage, Vh

7.1 Single Finger N-Channel MOSFET

Single finger N-channel MOSFETs are used in receiver (buffer) circuitry as half pass and full pass transistors and in driver/bi-directional circuits as pull-up and down devices. Single finger N-channel MOSFETs are also used as ESD networks.

Some processes contain an explicit masking step to block formation on the diffusions. Other processes do not contain salicide. Both salicided and non-salicided designs have been incorporated into the variations of this structure. In processes with no salicide block, parameters dealing with this layer can be ignored.

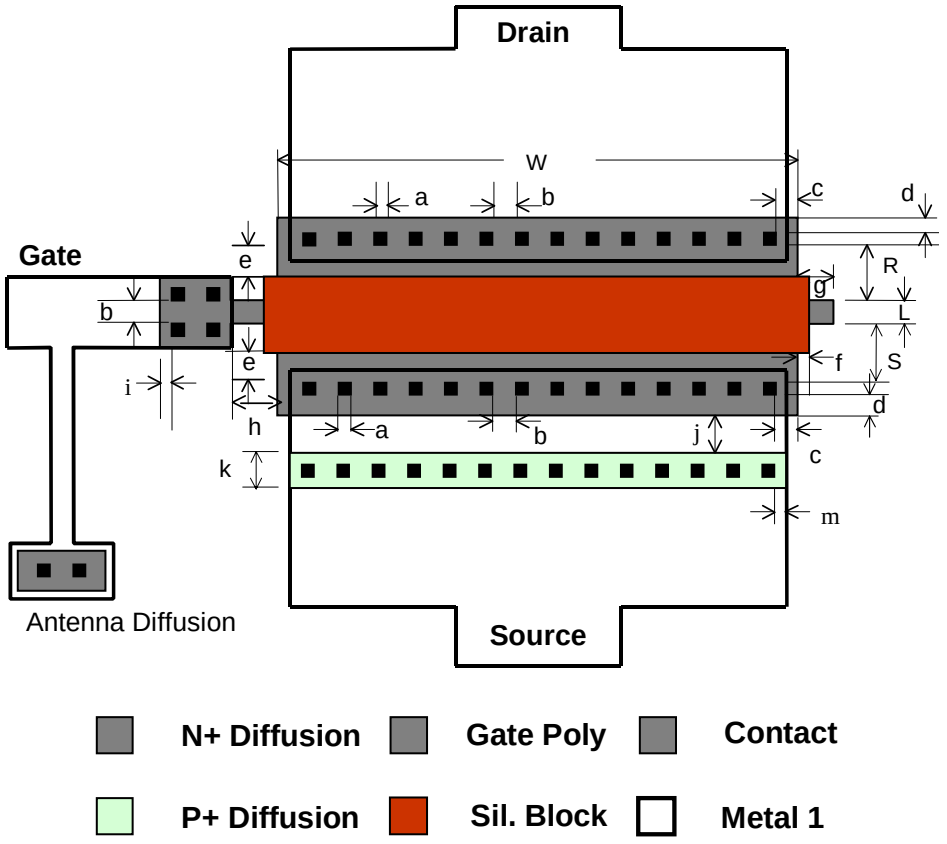

Figure 16 Single Finger N-Channel MOSFET with Salicide Block Option

Table 31 Layout Parameters for Single Finger N-Channel MOSFET with Salicide Block Option

Variable	Description of Layout Variables	Value
a	contact width	mdr
b	Contact to contact spacing	mdr
c	Contact to lateral side of N+ diffusion edge	3 x mdr
d	N+ contact to back side of N+ diffusion edge	mdr
e	N+ contact to salicide block spacing	mdr
f	Salicide block extension outside diffusion	mdr
g	Poly end overlap onto field or overhang	2 x mdr
h	Poly contact pad to diffusion spacing	2 x mdr
i	Contact to edge of poly contact pad	mdr
j	P+ to N+ diffusion spacing	mdr epi, 2 µm bulk
k	P+ substrate tie height	mdr to cover contacts
L	Poly gate length	see Table 31
m	Metal 1 to contact overhang	mdr
R	Drain contact to poly spacing	see Table 31
S	Source contact to poly spacing	see Table 31
W	N+ diffusion width	see Table 31

Notes: 1. M1 width must be at least 25 µm.
2. Polysilicon finger should be contacted only on one side.
3. Polysilicon contact area has 4 contacts.
4. Polysilicon gate tie-down is 2 µm by 1 µm rectangle with two contacts.

Table 32 Matrix of Variable Parameters for Single Finger N-Channel MOSFET

Name	W (µm)	L	R	S
NFET_1	25	mdr	mdr	mdr
NFET_1A	25	1.2 x mdr	mdr	mdr
NFET_1B	25	1.5 x mdr	mdr	mdr
NFET_1C	25	mdr	1 µm	1 µm
NFET_1D	25	mdr	3 µm	3 µm
NFET_1E	25	mdr	5 µm	5 µm
NFET_2	50	mdr	mdr	mdr
NFET_3	50	mdr	1 µm	3 µm
NFET_4	75	mdr	mdr	mdr

7.2 Multi-Finger N-Channel MOSFET

Multi-finger N-channel MOSFET devices are important for evaluating ESD robustness of I/O (driver) circuitry, multi-finger pass transistors, other peripheral circuits, and usage as ESD networks.

Some processes contain an explicit masking step to block silicide formation on the diffusions. Other processes do not contain silicide. Both silicided and non-silicided designs have been incorporated into the variations of this structure. In processes with no silicide block, parameters dealing with this layer can be ignored.

Figure 17 shows an example of a two-finger MOSFET. For added fingers, add the required number of poly lines above the source and alternate source and drain contacts to each N+ diffusion.

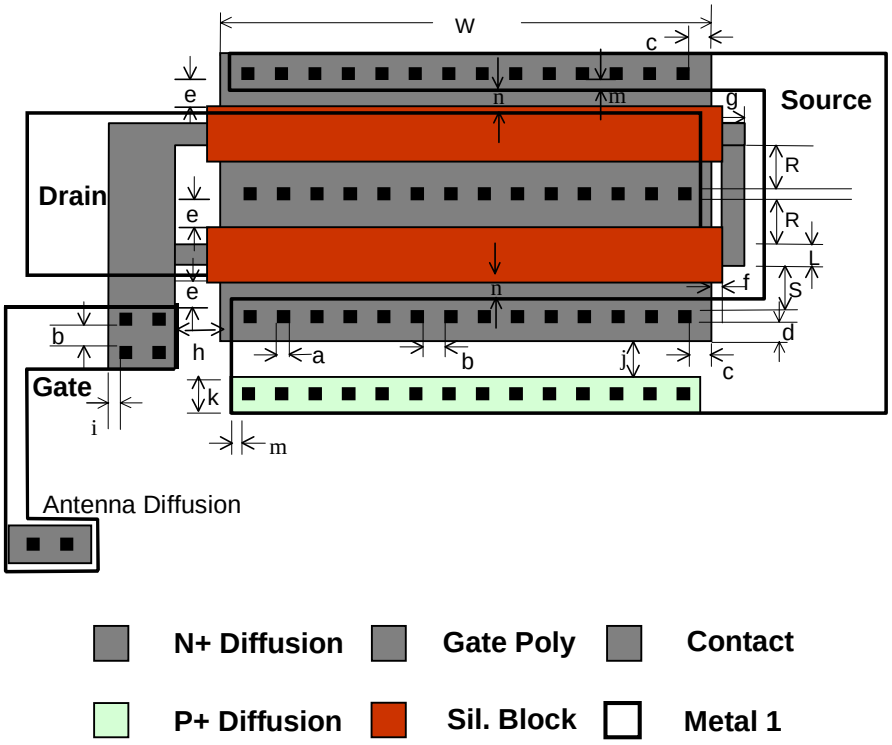

Figure 17 Multi-Finger N-Channel MOSFET

Table 33 Layout Parameters for Multi-Finger N-Channel MOSFET

Variable	Description of Layout Variables	Value
a	Contact width	mdr
b	Contact to contact spacing	mdr
c	Contact to lateral side of N+ diffusion edge	3 x mdr
d	N+ contact to back side of N+ diffusion edge	mdr
e	N+ contact to silicide block spacing	mdr
f	Silicide block extension outside diffusion	mdr
g	Poly end overlap onto field or overhang	2 x mdr
h	Poly contact pad to diffusion spacing	2 x mdr
i	Contact to edge of poly contact pad	mdr
j	P+ to N+ diffusion spacing	mdr epi, 2 µm bulk
k	P+ substrate tie height	mdr to cover contacts
L	Poly gate length	see Table 33
m	Metal 1 to contact overhang	mdr
n	Metal 1 to Metal 1 spacing	mdr
R	Drain contact to gate spacing	see Table 33
S	Source contact to gate spacing	see Table 33
W	N+ diffusion width	see Table 33

Notes: 1. Source and drain metal should increase to at least 25 µm as close to the device as possible.
2. Polysilicon finger should be contacted only on one side.
3. Polysilicon contact area has 4 contacts.
4. Polysilicon gate tie-down is 2 µm by 1 µm rectangle with two contacts.

Table 34 Matrix of Variable Parameters for Multi-Finger N-Channel MOSFET

Name	W	# Fingers	Total Width	L	R	S
MULTINFET_1	50 µm	2	100 µm	mdr	3 µm	1 µm
MULTINFET_2	50 µm	4	200 µm	mdr	3 µm	1 µm

7.3 N-Channel MOSFETs with Integrated Resistors

MOSFETs with an integrated resistor are a common ESD practice known as resistor ballasting. Benchmark structures are defined using the single finger n-channel MOSFET benchmark structure and the benchmark resistor structures.

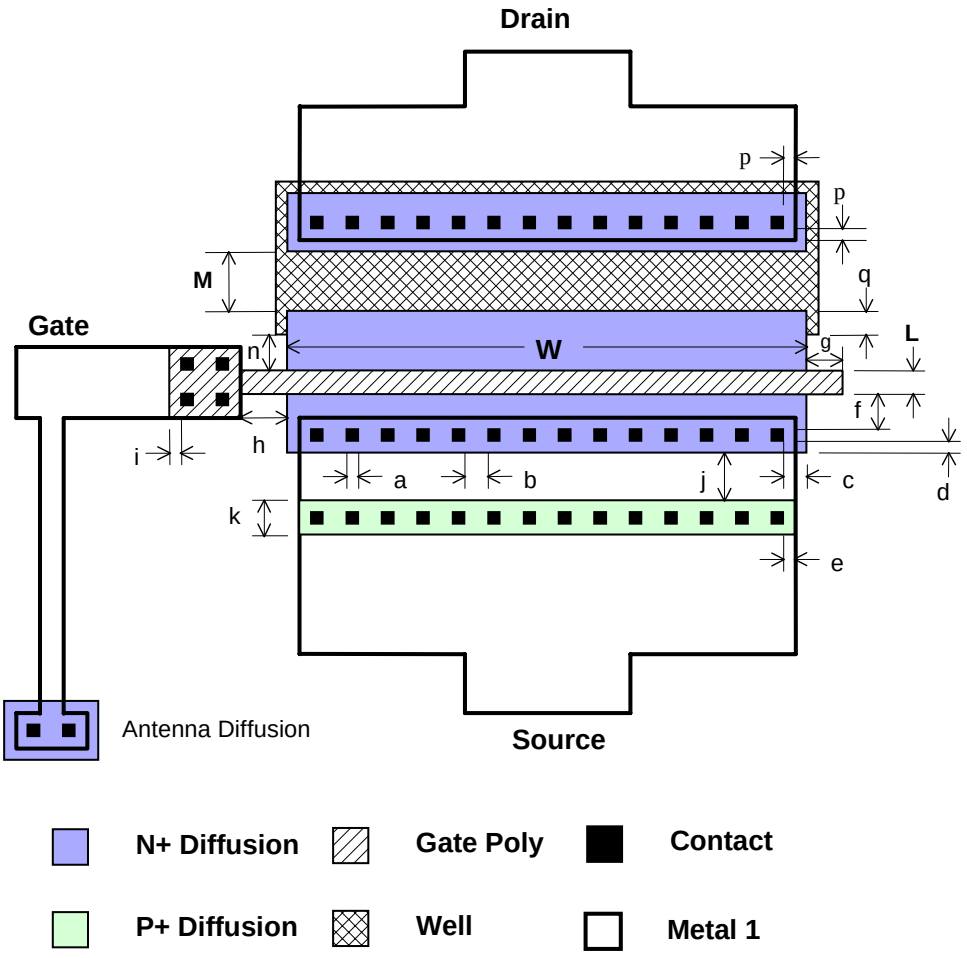

Figure 18 N-Channel MOSFET with Integrated Resistor

Table 35 Layout Parameters for N-Channel MOSFET with Integrated Resistor

Variables	Description of Layout Variables	Ranges of Layout Variables
a	N+/P+ contact width	mdr
b	N+ and P+ and poly contact to contact spacing	mdr
c	N+ contact to lateral side of N+ diffusion edge	2 x mdr
d	N+ contact to back side of N+ diffusion edge	2 x mdr
e	P+ contact to diffusion edge spacing	mdr
f	Source N+ contact to gate spacing	1.5 x mdr
g	Poly end overlap onto field or overhang	2 x mdr
h	Poly contact pad to diffusion spacing	2 x mdr
I	Contact to edge of poly contact pad	mdr
j	P+ to N+ diffusion spacing	mdr for epi; 2 µm for bulk
k	P+ substrate tie height	mdr
L	Gate length	See Table 35
M	N+ to N+ spacing of well resistor	See Table 35
n	N-well edge to drain gate separation	mdr
p	Metal 1 to contact overhang	mdr
q	N+ diffusion overlap onto well	mdr
W	Diffusion width	See Table 35

Notes:
1. Metal 1 width must be at least 25 µm.
2. Polysilicon finger should be contacted only on one side.
3. Polysilicon contact area has 4 contacts.
4. Polysilicon gate tie-down is 2 µm by 1 µm rectangle with two contacts.

Table 36 Matrix of Variable Parameters for N-Channel MOSFET with Integrated Resistor

Name	W (µm)	L	M (µm)
NWRESFET_1	25	mdr	1.0
NWRESFET_2	25	mdr	1.5
NWRESFET_3	25	mdr	2.0
NWRESFET_4	50	mdr	1.5
NWRESFET_5	75	mdr	1.5
NWRESFET_6	25	1.2 x Lmin	1.5
NWRESFET_7	25	1.5 x Lmin	1.5

7.4 Single Finger P-Channel MOSFET

Single finger P-channel MOSFETS are used in receiver (buffer) circuitry as full pass transistors and in driver and bidirectional circuits as pull-up and down devices. Single finger MOSFETs are also used in ESD networks.

Note that in this structure it is possible to bring the well tap to a separate pad to allow the source and drain terminals to be reversed. Such a structure should allow the effects of well tap placement on parasitic PNP series resistance to be studied.

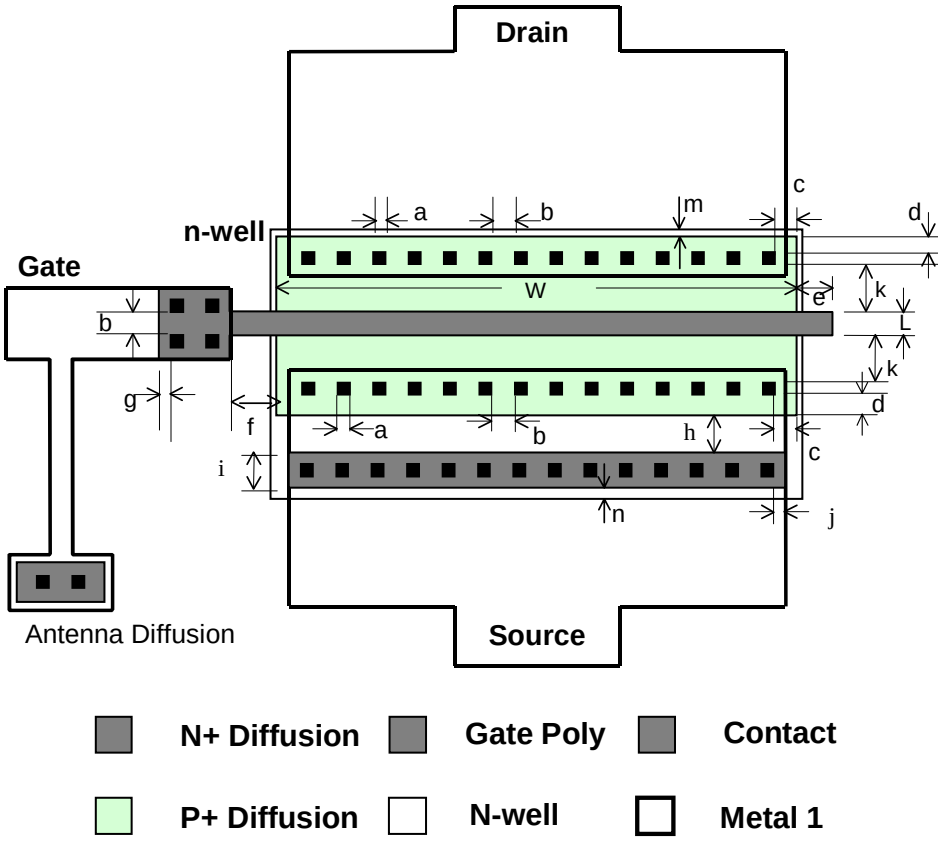

Figure 19 Single Finger P-Channel MOSFET

Table 37 Layout Parameters for Single Finger P-Channel MOSFET

Variable	Description of Layout Variables	Value
a	Contact width	mdr
b	Contact to contact spacing	mdr
c	Contact to lateral side of P+ diffusion edge	mdr
d	P+ contact to back side of P+ diffusion edge	mdr
e	Poly end overlap onto field or overhang	2 x mdr
f	Poly contact pad to diffusion spacing	2 x mdr
g	Contact to edge of poly contact pad	mdr
h	P+ to N+ diffusion spacing	mdr
i	N-well plug height	mdr to cover contacts
j	M1 to contact overhang	mdr
k	Source and drain contact to gate spacing	mdr
L	poly gate length	see Table 37
m	N-well extension outside P+ diffusion (all sides)	mdr
n	N-well extension outside N+ diffusion (all sides)	mdr
W	P+ diffusion width	see Table 37

Notes:
1. Metal 1 width must be at least 25 µm.
2. Polysilicon finger should be contacted only on one side.
3. Polysilicon contact area has 4 contacts.
4. Polysilicon gate tie-down is 2 µm by 1 µm rectangle with two contacts.

Table 38 Matrix of Variable Parameters for Single Finger P-Channel MOSFET

Name	W (µm)	L
PFET_1	25	mdr
PFET_1A	25	1.2 x mdr
PFET_1B	25	1.5 x mdr
PFET_2	50	mdr
PFET_3	75	mdr

7.5 Multi-Finger P-channel MOSFET

Multi-finger P-channel MOSFET devices are important for evaluating ESD robustness of I/O (driver) circuitry, multi-finger pass transistors, other peripheral circuits, and usage as ESD networks.

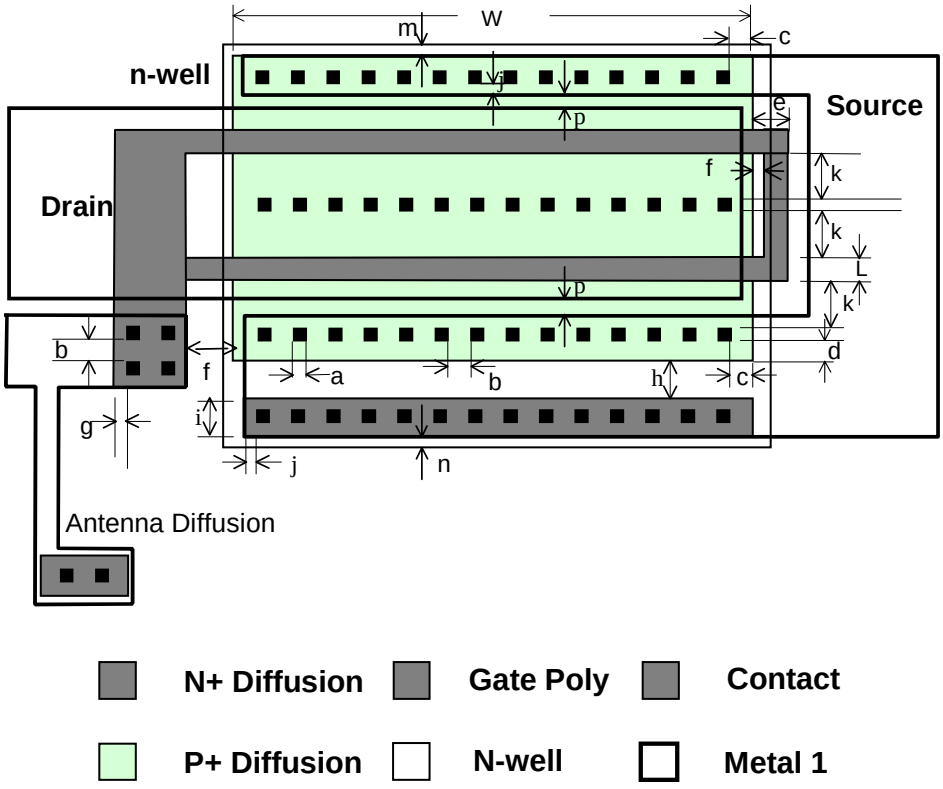

Figure 20 Multi-Finger P-Channel MOSFET

Table 39 Layout Parameters for Multi-Finger P-Channel MOSFET

Variable	Description of Layout Variables	Value
a	Contact width	mdr
b	Contact to contact spacing	mdr
c	Contact to lateral side of P+ diffusion edge	mdr
d	P+ contact to back side of P+ diffusion edge	mdr
e	Poly end overlap onto field or overhang	2 x mdr
f	Poly contact pad to diffusion spacing	2 x mdr
g	Contact to edge of poly contact pad	mdr
h	P+ to N+ diffusion spacing	mdr
i	Well plug height	mdr to cover contacts
j	Metal 1 to contact overhang	mdr
k	Source and drain contact to gate spacing	mdr
L	Polysilicon gate length	see Table 39
m	N-well surround of P+ diffusion (all sides)	mdr
n	N-well surround of N+ well plug (all sides)	mdr
p	Metal 1 to Metal 1 spacing	mdr
W	P+ diffusion width	see Table 39

Table 40 Matrix of Variable Parameters for Multi-Finger P-Channel MOSFET

Name	W	# fingers	Total Width	L
MULTIPFET_1	50 µm	2	100 µm	mdr
MULTIPFET_2	50 µm	4	200 µm	mdr

7.6 Multi-Finger PMOS with Local Well Taps

Multi-finger P-channel MOSFETs using local well taps is important in peripheral circuit designs. In multi-finger P-channel MOSFET with local well taps, the on-resistance R_{on} of the P-channel MOSFET in a forward bias mode is the electrical parameter of interest.

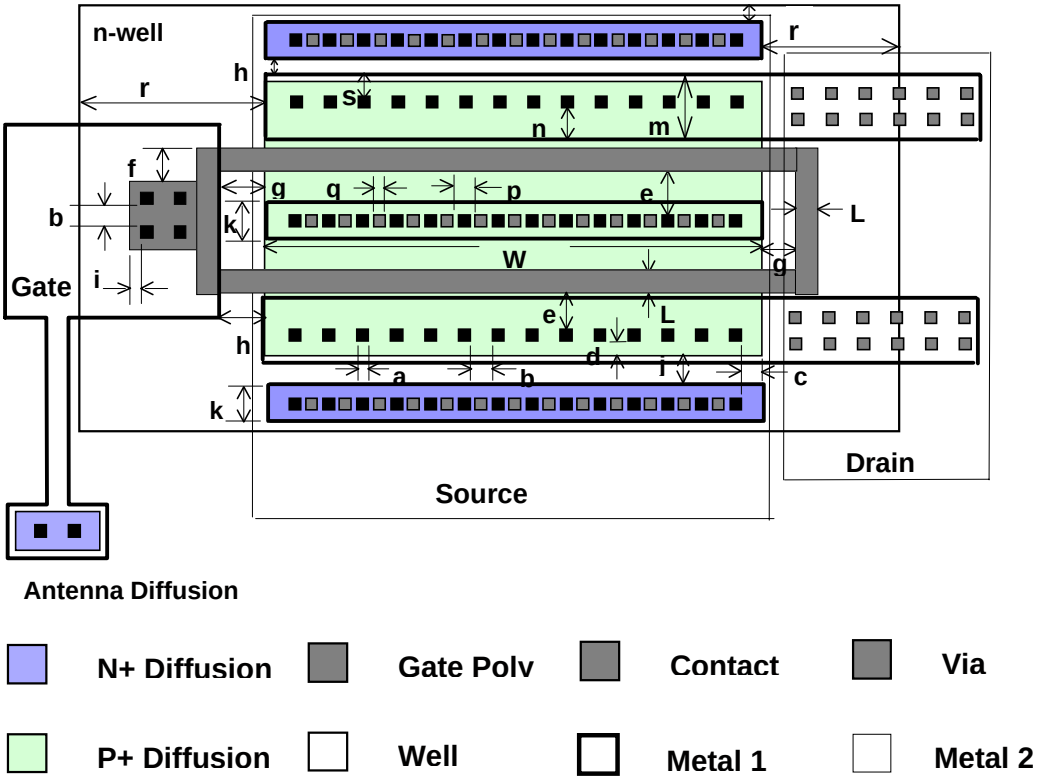

Figure 21 Multi-Finger PMOS with Local Well Taps

Table 41 Layout Parameters for Multi-Finger PMOS with Local Well Taps

Variables	Description of Layout Variables	Ranges of Layout Variables
a	N+ and P+ contact width	mdr
b	N+ and P+ and poly contact to contact spacing	mdr
c	N+ and P+ contacts to lateral side of N+/P+ diffusion edge	mdr
d	N+ and P+ contact to back side of P+ diffusion edge	mdr
e	P+ contact to gate spacing	mdr
f	Poly contact head to outer gate edge	centered; 2f=2L+2e-a-b-2i
g	Poly end cap to cross bar space	2 x mdr
h	Metal 1 to Metal 1 spacing at closest approach	mdr
I	Poly contact to edge of poly gate head	mdr
j	P+ drain to N+ well tap spacing	mdr
k	Metal 1 height at P+ source and N+ well tap	mdr to enclose contacts
L	Gate length	mdr
m	Metal 1 height at source	as wide as possible, to allow capture of current from contacts
n	P+ contact to metal edge spacing, drain facing gate	n=m-a-s
p	Via to via spacing	mdr
q	Via width	mdr
r	N-well enclosure of diffusions	mdr
s	P+ contact to metal edge, drain opposite gate; also N+ contact to metal edge	mdr (s=(k-a)/2), or for P+ drain, max. consistent with close approach of P+ and N+ metal

Notes:
1. If vias can be stacked on contacts, maximum density of contacts and vias can be achieved and is desirable. Otherwise, vias and contacts on the source and well taps may be interspersed as shown.
2. Metal 2 picks up source and drain current as shown; overlaps of vias are not critical.
3. Structure may be stepped and repeated, to form any number of fingers. Well taps on top and bottom are merged with those of the next cell.
4. Gate tie-down for polysilicon is a 2 µm x 1 µm N+ diffusion rectangle with two contacts.

Table 42 Matrix of Variable Parameters for Multi-Finger N-Channel MOSFET with Local Taps

Name	W/finger	# fingers	Total W	L	e
MULTITAPPFET_1	50 µm	2	100 µm	mdr	mdr
MULTITAPPFET_2	50 µm	4	200 µm	mdr	mdr

8 SILICON CONTROLLED RECTIFIERS

Silicon controlled rectifiers (PNPN structures) are used as ESD protection circuits and are contained in peripheral circuits as parasitic devices. Analysis of these structures is important to understand the ESD robustness where silicon controlled rectifiers (SCRs) are used.

The following structures are included to evaluate the MOSFET:

- Thick oxide triggered SCR
- Low voltage triggered N-channel MOSFET SCR

Some measurements of interest from these structures are as follows:

- DC I-V curves to measure:
  - Trigger voltage, V_{tr}
  - Trigger current. I_{tr}
  - Holding voltage, V_h
  - Holding current, I_h.
  - ESD metric of volts/µm of device width

8.1 Thick Oxide NPN Triggered SCR

A thick oxide NPN triggered SCR uses a lateral NPN to trigger the SCR. Details of the structure's operation can be found in the references [15.5 – Rountree, *ESD Symp. Proc.* 1988, 15.5 – Duvvury, *ESD Symp. Proc.* 1991].

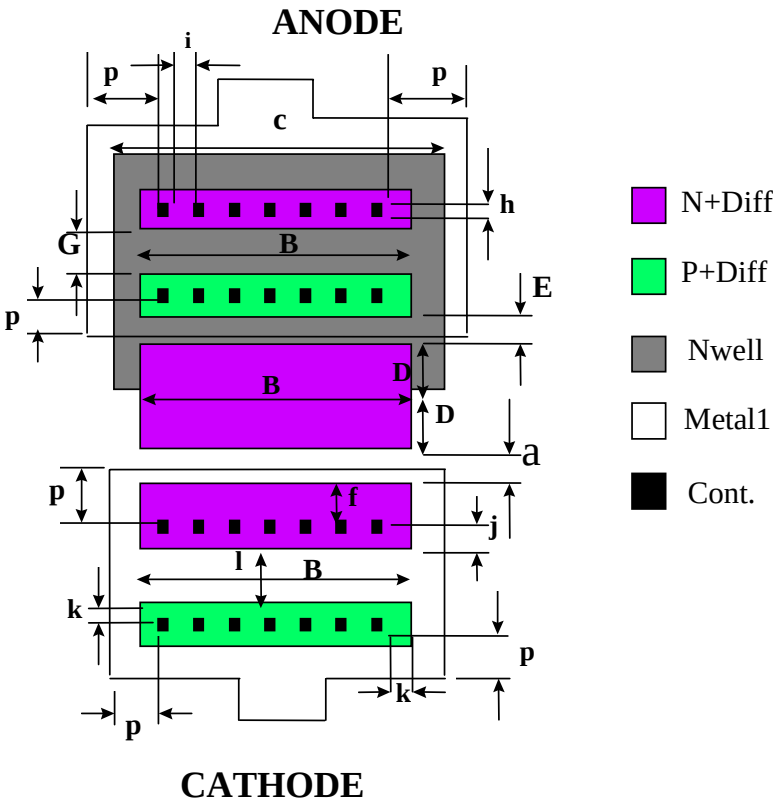

Figure 22 Thick Oxide NPN-Triggered SCR

Table 43 Layout Parameters for Thick Oxide NPN-Triggered SCR

Variables	Description of Layout Variables	Ranges of Layout Variables
a	Channel length (N+ to N+ space)	mdr
B	Structure width	See Table 43
c	Width of N-well	B + 4 µm
D	Trigger diffusion underlap/overlap of N-well	See Table 43
E	P+ anode to trigger diffusion spacing	See Table 43
f	N+ diffusion overlap of contact towards anode	mdr
G	P+ anode to N-well contact spacing	See Table 43
h	Contact size	mdr
i	Contact to contact spacing	mdr
j, k	N+ or P+ diffusion overlap of contact (all sides)	mdr
l	N+ diffusion V_{SS} to P+ tap spacing	mdr (epi) 2 µm (bulk)
p	Lateral metal overlap of contact	mdr

Notes: 1. Metal 1 width must be at least 25 µm.

Table 44 Matrix of Variable Parameters for Thick Oxide NPN-Triggered SCR

Name	B (µm)	D	E	G
MLSCR_1	25	mdr	mdr	mdr
MLSCR_1A	25	2 x mdr	mdr	mdr
MLSCR_1B	25	mdr	2 x mdr	mdr
MLSCR_1C	25	mdr	3 x mdr	mdr
MLSCR_1D	25	mdr	mdr	0
MLSCR_1E	25	mdr	mdr	2 x mdr
MLSCR_1F	35	mdr	mdr	mdr
MLSCR_1G	50	mdr	mdr	mdr

8.2 Low Voltage N-Channel MOSFET Triggered SCR (LVTSCR)

A low voltage N-channel MOSFET triggered SCR (LVTSCR) uses an N-channel MOSFET to trigger the SCR. Details of this structure's operation can be found in the references [16.5-Chatterjee IEEE El. Dev. Letters, 1991].

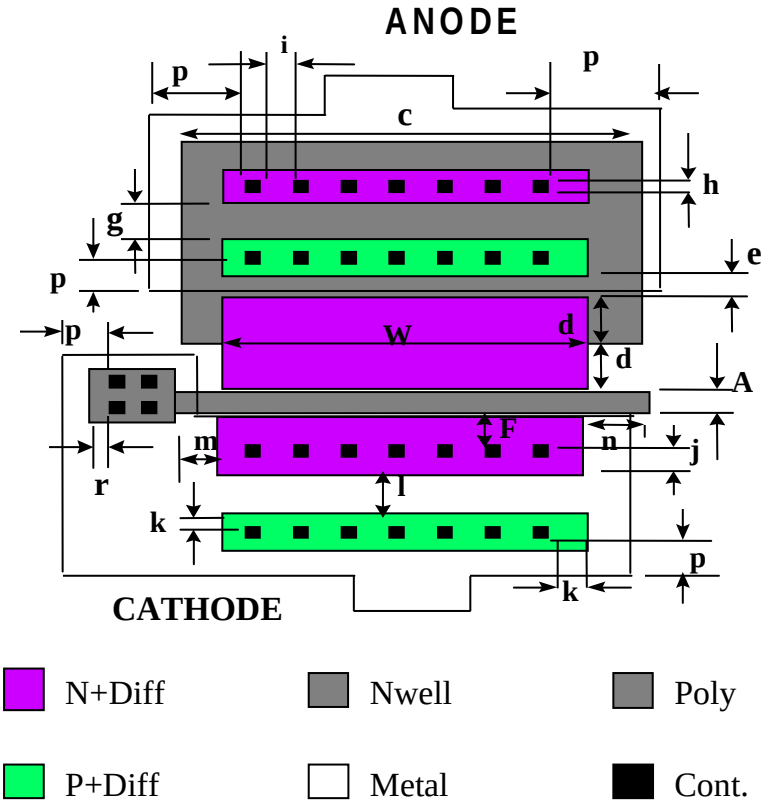

Figure 23 Low Voltage N-MOSFET Triggered SCR (LVTSCR)

Table 45 Layout Parameters for Low Voltage N-Channel MOSFET-Triggered SCR (LVTSCR)

Variables	Description of Layout Variables	Ranges of Layout Variables
A	Channel length	See Table 45
B	Structure width	See Table 45
c	Width of N-well	B + 4 µm
D	Trigger diffusion underlap/overlap of N-well	See Table 45
E	P+ anode to trigger diffusion spacing	See Table 45
F	N+ diffusion overlap of contact towards anode	See Table 45
G	P+ anode to N-well contact spacing	See Table 45
h	Contact size	mdr
i	Contact to contact spacing	mdr
j, k	N+ or P+ diffusion overlap of contact (all sides)	mdr
l	N+ diffusion V_{SS} to P+ tap spacing	mdr
m,n	Overhang of poly gate	2 x mdr
p	Metal overlap of N-well	mdr
r	Poly overlap of contact	mdr

Notes: 1. Metal 1 width must be at least 25 µm.

Table 46 Matrix of Variable Parameters for Thick Oxide NPN-Triggered SCR

Name	B (µm)	A	D	E	F	G
LVTSCR_1	25	mdr	mdr	mdr	mdr	mdr
LVTSCR_1A	25	1.2 x mdr	mdr	mdr	mdr	mdr
LVTSCR_1B	25	mdr	2 x mdr	mdr	mdr	mdr
LVTSCR_1C	25	mdr	mdr	mdr	3 x mdr	mdr
LVTSCR_1D	25	mdr	mdr	mdr	mdr	0
LVTSCR_1E	25	mdr	mdr	mdr	mdr	2 x mdr
LVTSCR_2	35	mdr	mdr	mdr	mdr	mdr
LVTSCR_3	50	mdr	mdr	mdr	mdr	mdr
LVTSCR_4	25	mdr	mdr	2x mdr	mdr	mdr
LVTSCR_5	25	mdr	mdr	3x mdr	mdr	mdr

9 ESD MODULE/PAD CONFIGURATION

For the benchmark structures, module (e.g., pad configurations, bussing, wiring, etc.) definitions and recommendations are provided to avoid problems of implementations in specific corporations, laboratories, or test houses. Guidelines are provided to avoid the module definition from influencing the ESD results of the benchmark structure.

The following guidelines are recommended:

- A dedicated substrate pad should be local to the ESD benchmark structures.
- The substrate resistance between substrate and the benchmark structure should be less than the MOSFET "on" resistance.
- Pads should not be shared between ESD benchmark structures.
- The wire width from the pad to ESD benchmark structure should follow the wire width as defined in the individual ESD benchmark structure.
- The wire width from the ESD benchmark structure to the substrate or V_{DD} pad should either follow the width defined in the benchmark structure or exceed it by 20 µm for M1 metal level and by 10 µm for any higher metallurgical level.

The ESD technology benchmark structures will be provided in sub-macros configurations.

10 TABULATION OF THE ESD ROBUSTNESS OF THE TECHNOLOGY

For cross-evaluation of the ESD robustness, the different ESD technology benchmark structures according to the extracted ESD metrics can be tabulated as demonstrated below.

11 GLOSSARY OF TERMS

Avalanche voltage: The voltage at which a diode structure or MOSFET drain undergoes avalanche multiplication and breakdown.

Avalanche breakdown: A phenomenon where a reverse-biased P-N junction conducts as a result of electron-hole pair creation in the high electric field region of the junction's depletion layer.

Critical current-to-failure: The current magnitude under which destructive damage occurs to the tested structure. Where this parameter scales with structure width, it's often given in units of width: mA/µm, for example.

Dielectric breakdown: The voltage at which a dielectric interface looses its dielectric integrity. Generally, this is defined by the dielectric conducting current either grossly or by leakage above a specified limit.

Forward bias voltage: The voltage at which a diode structure allows the passage of current.

Holding voltage, V_h: the lowest voltage at which a structure can maintain a regenerative phenomenon. For example, in latchup, the holding voltage is defined as the lowest voltage at which a PNPN structure operates in its low voltage/high current state. In some cases, it may be necessary to trigger the regenerative phenomenon and reduce the voltage or current to find the holding point.

Holding current, I_h: the lowest current under which a structure can maintain a regenerative phenomenon.

Latchup: A phenomenon in which a PNPN structure switches from a high voltage/low current state to a low voltage/high current state.

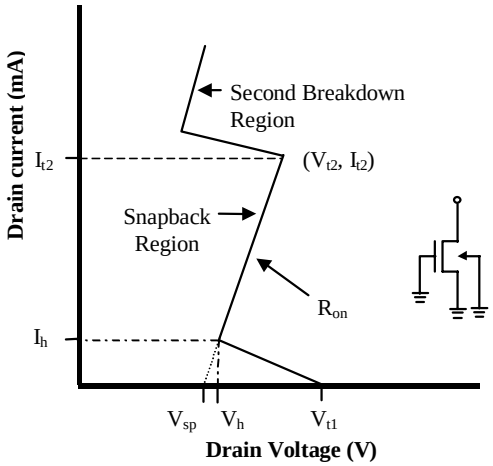

Figure 24 Example of N-MOSFET Snapback and Second Breakdown Behavior

MOSFET snapback: A phenomenon in which a MOSFET switches from a high voltage/low current state to a low voltage/high current state by activating the parasitic bipolar device between source, body, and drain.

MOSFET second breakdown: A condition under which a MOSFET becomes permanently damaged due to high drain current, generally through thermally-activated localized current runaway.

MOSFET trigger voltage, V_{t1}: The voltage at which the regenerative effects associated with MOSFET snapback begin.

MOSFET trigger current. I_{t1}: The current at which the regenerative effects associated with MOSFET snapback begin. In Figure 24, it is shown occurring at 0.

MOSFET second breakdown current, I_{tr2}: The maximum drain current which a MOSFET can handle in snapback before becoming permanently damaged.

MOSFET second breakdown voltage, V_{tr2}: The maximum drain current which a MOSFET can handle in snapback before becoming permanently damaged.

On-resistance R_{on}: The resistance of the device-under-test. Dynamic resistance: The resistance of the device-under-test during the testing process.

Power-to-failure P(t): is defined as the product of Idrain * Vdrain integrated over a given transmission pulse width, t = 100 ns for example, which leads to device failure.

Velocity saturation current magnitude: The maximum current reached after carriers reach velocity saturation.

12 PAD CONFIGURATION

Use EIA/JEDEC Publication No. 128, *Guide For Standard Probe Pad Sizes And Layouts For Wafer Level Electrical Testing*, standard as a way to configure the benchmark structures. This is a 2 x 16 pad configuration that is used in the industry as a standard.

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