Boundary Scan Advanced Diagnostic Methods

Christopher Cain
Agilent Technologies
Loveland, Colorado USA
christopher_cain at agilent dot com

Abstract:

Boundary-scan (1149.1) technology was originally developed to provide a far easier method to perform digital DC testing to detect intra-IC interconnect assembly faults, such as solder shorts and opens. Today's advanced IC technology now includes high-speed differential interfaces that include AC or DC coupling components loaded on the printed circuit assembly. Simple stuck-at-high/low test methods are not sufficient to detect all assembly fault conditions, which includes shorts, opens and missing components. Improved diagnostics requires detailed circuit analysis, predictive assembly fault simulation and more complex testing to isolate and accurately detect all possible assembly faults.

Several cases will be presented to illustrate how usage of circuit information and predictive analysis of potential assembly faults will provide more precise and accurate diagnostic information. Special attention will be paid to the increasing usage of high-speed differential logic interfaces and their associated discrete components and connectors, which increasingly have no probing access and then traditional incircuit test cannot be accomplished.

The material will also include a discussion of future challenges and their potential impact on diagnosis of assembly faults. Many in the industry are very much aware of the decline in probing access and are wisely skeptical of claims that providing a function test will provide an accurate and useful diagnostic indication upon failure. This material is intended to further the development and evaluation of solutions that not only detect, but usefully diagnose assembly faults….which clearly are not disappearing any time soon!

Background

What is Boundary-Scan?

Boundary-Scan is a test technique that involves Integrated Circuit (IC) devices designed with shift registers placed between each device pin and the internal logic as shown in Figure 1. Each shift register is made up from Boundary cells. These cells allow you to control and observe what happens at each input pin and control the state of each output pin of the IC device. When these cells are connected together within the IC device, they form a data register, called the Boundary Register.

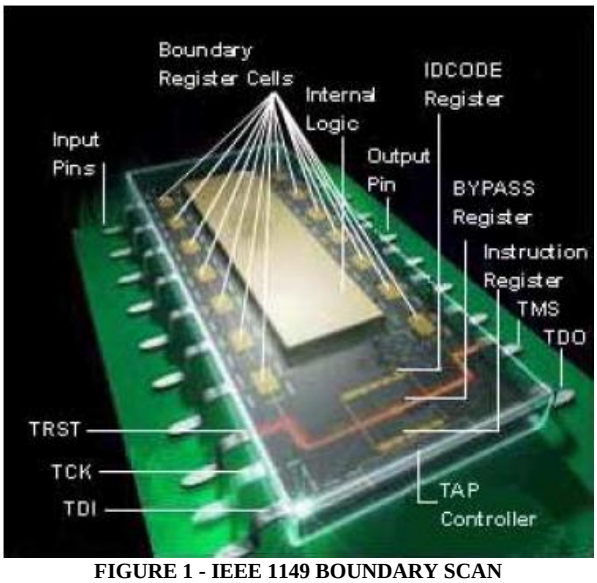


FIGURE 1 - IEEE 1149 BOUNDARY SCAN

Multiple IC's on a Printed Circuit Assembly (PCA) can be connected together to form linked boundary registers, called a boundary-scan chain and there may be multiple chains on a particular PCA. These chain(s) of boundary-scan cells provide the ability to drive/receive digital voltage levels (representing 0 and 1 values) to enable many forms of testing, programming, measurement and control that can be automated into special purpose test equipment, from just the 4-5 signals of the boundary-scan interface, called the Test Access Port (TAP).

This was instantiated as an IEEE standard in 1990, with IEEE 1149.1[reference 2]. This standard method of BIST revolutionized structural testing of printed circuit assemblies (PCAs), as IC's became so complex that traditional component and PCA-level function testing was fast becoming impossible from an economic and time-to-develop viewpoint. This also provided a very useful serial port on the IC that many CPU/MCU designers' utilized to provide an externally accessible "debug port". Increasingly, the 1149.1 interface is being utilized to access very sophisticated "embedded measurement / test" capability.

Since the standard was initially ratified by IEEE in 1990, many improvements and enhancements have been made to provide new standards for Programmable Device programming (IEEE 1532) memory testing (IEEE 1581), high-speed differential interconnects (IEEE 1149.6[reference 3]). There continue to be extremely important new enhancements in the process of development and ratification and Figure 2 outlines today's predominant Boundary Scan test standards.

Test Standards	Description	Purpose/Target Device
IEEE 1149.1	▪ Boundary-scan testing methods to enable ***digital IO stuck-at fault detection*** for IC interconnect defects.	▪ Digital device with boundary-scan enabled IO pins and supports the JTAG test port of 4 pins that is accessible to probing.
IEEE 1149.4	▪ Boundary-scan controlled ***mixed-signal testing interface***	▪ Additional test pins (2 additional) to support analog AC/DC measurements through enabled IO pins.
IEEE 1149.6	▪ Boundary-scan extension to support ***testing of "Advanced" IO pins.***	▪ Enables boundary-scan testing of high-speed differential (DC or AC coupled) IO pins, especially SERDES pins.
IEEE 1532	▪ ***In-system programming (ISP)*** through boundary-scan interface	▪ Allows concurrent programming of large memories (typically non-volatile) within programmable logic devices.
IEEE 1581	▪ ***I/O Loopback testing*** for devices that commonly do not have 1149.1.	▪ Enables boundary-scan IC's to validate interconnections to attached memory devices with loopback test.
IEEE P1149.1 (INIT Revision)	▪ Boundary-scan extensions to support ***complex device initialization and post-test pin quiescence.***	▪ IO interfaces and power management features in today's IC's require more sophisticated initialization sequences to prepare the device and PCAs for safe/reliable testing.
IEEE P1149.8.1	▪ Boundary-scan extensions to support ***vector-less open fault measurements***.	▪ Enable IO pins to selectively toggle digital state to enable AC-coupled capacitive sensor (no direct electrical probe access) to measure solder open defects.
IEEE P1687	▪ Boundary-scan extensions to support ***efficient access to user-defined registers and internal instrumentation***.	▪ Enables description and much more efficient access to IC BIST and Embedded Measurement capabilities increasingly designed into complex IC's.

FIGURE 2 - BOUNDARY-SCAN STANDARDS

As with any truly useful standard, it provides the foundation for testing, but leaves the actual methods of performing test as an "exercise for the reader". Remember reading that in your college text books as a taunting challenge? It remains a daunting challenge and there are many variations on how boundary-scan is implemented for testing PCAs.

Advanced Boundary Scan for detection of assembly faults

Boundary Scan technology is ideal for complex PCA design validation and turning on early prototypes. With just a few signal pins, you can easily control and read any boundary-scan accessible IO pin. This can be combined with complex sequences of control (drive) and read (receive) actions to perform function validation activities and even complex tasks such as programming non-volatile memory or testing DDR or Static memory.

Extending this capability to drive a particular IC boundary-scan cell to the available digital states (high/low) and sensing on all other connected (through the PCB and loaded devices such as resistors, capacitors, jumpers and buffers) IC boundary-scan cell receivers is an ideal way to detect assembly faults. What are the likely assembly faults? If one assumes that assembly faults typically follow a probability of occurrence as follows:

1. Opens (this is the majority of faults on surface-mount component PCAs)
2. Shorts
3. Miss-placed components (presence, orientation)
4. Bad / wrong components (correctness, alive)

There are frameworks that establish precisely defined terminology for establishing classifications of assembly faults. This are quite useful to ensure everyone is talking about the same topic, so we have tried to remain consistent with PCOLA-SOQ terminology [references 7 and 8] which has been adopted by groups like iNEMI, so it has some redeeming value.

Of course, there are many factors that determine boundary-scan defect detection and precision assembly fault diagnosis. These include:

- Maximum usage of IC's with boundary-scan capability and each IC implements a full drive/receive cell for all IO pins on the device. This can be more complex to evaluate in the case of differential IO, especially when older non-differential 1149.1 capabilities is mixed with newer differential 1149.6 capabilities.
- Design-For-Testability (DFT) guidelines and best practices to ensure the digital signals are connected in a manner for effective and reliable use of boundary-scan test methods. There are many papers, books and tutorials on this topic.
- Advanced boundary-scan test sequences and effective extraction of boundary-scan test results that are designed to detect and precisely diagnose printed circuit assembly (PCA) faults on the maximum number of potential fault locations. This topic is the focus of this paper.

There is also a sequence to boundary-scan assembly fault detection, to ensure that faults that can cause damage are detected first and simple faults that can be detected quickly are detected next and so forth. A suggested sequence is as follows:

1. Check boundary-scan chain integrity, including device IDCODE/USER-CODE as appropraite
2. Shorts detection and precise diagnosis (physical location)
3. Simple opens, with precise diagnosis (physical location)
4. Complex opens, with precise diagnosis (physical location)
5. Component failures (typically not electrically present) by specific component
6. Opens and component failures through precision function testing (embedded test or BIST).

We'll review some interesting cases in which advanced boundary-scan diagnostic methods can be utilized to detect AND precisely diagnose assembly faults.

Advanced Shorts Fault Diagnosis

Let's start with straight-forward stuck-at fault testing, such as driving a digital high/low signal on a single interconnect between two boundary-scan cells and then detecting/receiving a high/low value on those (expected or unexpected) interconnected cells. What happens when signals are interconnected between more than two boundary-scan IC's? A straight-forward method of stuck-at fault testing will certainly capture many assembly faults, but the diagnostic message may be a long list of all potential failures or even more difficult, a detailed listing of the boundary-scan cell failures. These can take a skilled engineer quite a bit of time and correlation with the PCA schematic and understanding of boundary-scan technology to diagnose the root-cause.

Figure 3 shows an example circuit, with shared (sometimes called "bus-wire") connections between multiple boundary-scan enabled IC's. While complex interconnect faults can be easily detected, precise diagnosis requires a great deal of forethought into the extended boundary-scan test cases and interpretation of the multiple test case results and in some cases, information beyond the net list and Boundary-Scan-Description-Language files provided to perform the boundary-scan tests.

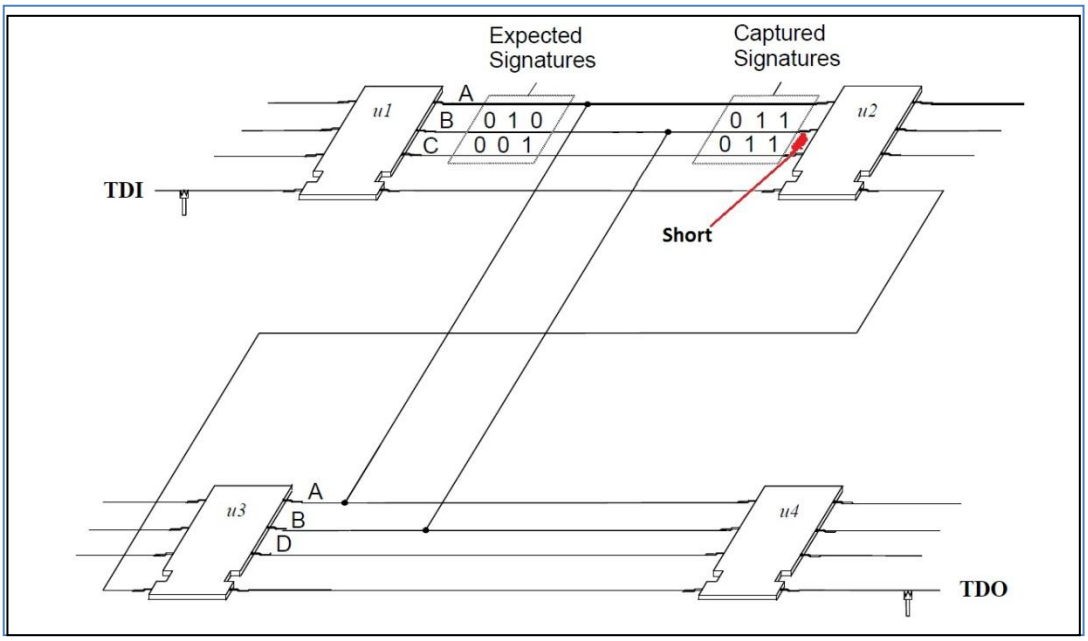


FIGURE 3 – "SHORTED" FAULT EXAMPLE

(This example shown has the boundary-scan TAP shown in a simplified representation to reduce clutter; note there are more signals required for a functioning boundary-scan chain.)

This particular example shows one specific boundary-scan test case that is driving the shared interconnect between u1, u2, u3 and u4. Unique electrical points (we'll call them "nodes") are indicated by the labels A, B, C and D. To simplify this example; boundary-scan devices u1 and u3 can only drive signals, while devices u2 and u3 can only receive signals.

You can see how a shorting fault between node B and C is detected by driving patterns of high (1) and low (0) signals from u1, received into u2 and from u3 received into u4 using boundary-scan to access those pins through the TAP and boundary-scan capability. This results in the conclusion that node B and C must be "shorted" together to explain the received boundary-scan patterns. In this case, two node patterns are in error and do not match any other pattern assigned to any other node. An example "repair ticket" of the summary diagnosis is represented in Figure 4 below:

```
-------------------------------------------
Jan 09 17:40:06 2011
-------------------------------------------
Boundary-scan shorts test u1_u4 FAILED
SHORTS FAILURE DETECTED

Short has been detected between the following nodes:
  B and C, probably near pin u2.2
-----------------------------------------
```

FIGURE 4 - REPAIR TICKET FOR "SHORTED" FAULT EXAMPLE

Now you might have noticed the phrase "probably near pin u2.2". Where did that come from? How was boundary-scan able to detect that?

This is where advanced diagnosis comes into play. The physical placement of device pins is typically defined by the component package and PCB layout information. This is typically also extracted to understand potential probing location for incircuit testing probes.

This physical location information can be used by advanced diagnostic routines with the assumption that the majority of shorting faults in most PCA processes are relatively small in size, due to the precise placement of solder paste, which is later melted (reflowed) in high temperature processing steps. We can limit the likely set of potentially shorted device pins based up on the concept of a "shorting radius", by analyzing the physical placement of solder joints. A typical "shorting radius" is 2.54mm (0.1 inches) and can be settable by the test engineer as board densities vary from board-to-board design. This

advacned diagnostics feature is not yet common on all boundary-scan test systems and can be limited to probed non-boundary-scan test signals that are used to extend the test coverage of boundary-scan testing. This is because these probe locations provide an easy way to determine "shorting radius".

In this case pins u2.2 and u2.3 are physically adjacent and thus the more precise diagnostic of "probably near pin u2.2". This level of precision is of tremendous help to the repair technician and also results in much lower repair costs. Imagine not having to replace multiple expensive BGA's and re-testing to repair a board. Precise diagnostics saves time and money!

Advanced Open Fault Diagnostics

While it would be easy to generate every possible boundary-scan accessible drive/receive/tri-state pattern, that would create an explosion of test cases (and diagnostic messages) based upon the complexity of signal interconnects on a particular PCA design and number/size of boundary-scan devices.

By close observation of all potential faults and working to keep all test cases to the minimum needed, the following algorithm can be established to provide defect detection and high precision diagnosis. This is best accomplished by automated test generation software, which simulates all possible test cases, based up on the measurement capability of each boundary-scan device (obtained through its Boundary-Scan-Description-Language file), the PCA circuit design and any non-boundary-scan components that may influence the digital operation of the boundary-scan accessible nodes. This includes devices such as resistors, capacitors (in the case of differential signals), buffers and digital logic devices.

The following pattern table (Figure 8) demonstrates the generation of 1's and 0's bits to detect shorts to power and ground pins, counting bits to distinguishes between multiple nodes (interconnected to 2 or more pins) and complement bits to enable test cases that reduce diagnosis "aliases" for more precise diagnosis of shorting faults. Aliasing can occur if insufficient patterns are executed, allowing shorted signals to have observed patterns that match other node normal behaviors.

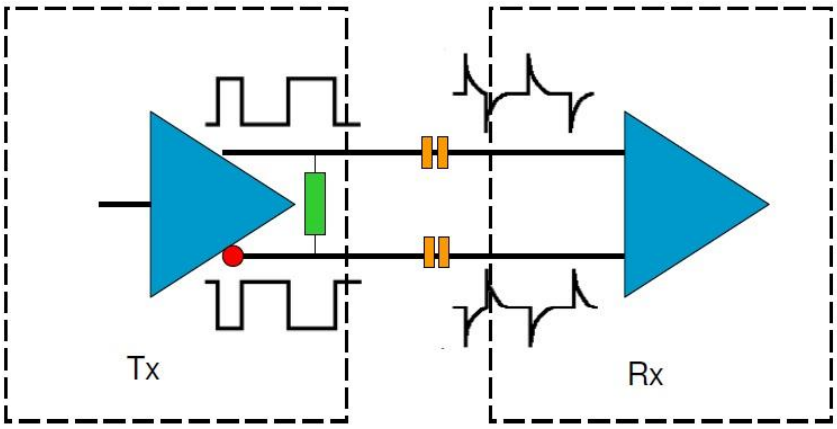
Node	Power Bits Eliminates Aliasing to Ground or VCC		Counting Bits Primarily Distinguishes one Node From Another				Complement Bits Reduces Incidence of Aliasing Between Active Nodes		
A	0	1	0	0	0	1	1	1	0
B	0	1	0	0	1	0	1	0	1
C	0	1	0	0	1	1	1	0	0
D	0	1	0	1	0	0	0	1	1

FIGURE 5 - BOUNDARY-SCAN PATTERNS FOR ADVANCED DIAGNOSIS

This advanced boundary-scan diagnostics all sounds dandy, but how does one determine the diagnostic performance of a boundary-scan tester? That is the subject of our next section, which describes complex detection and diagnosis challenges raised by differential signal pins. These signals were made much more boundary-scan testable through the development and adoption of the IEEE 1149.6 standard. The fault injections described in the next section can be used to determine the assembly fault detection and precision of diagnosis for circuit using IEEE 1149.6 compliant devices. This is critical in the case un-accessible (not electrically probable) differential signal pins that operate at speeds that cannot afford any test points or signal path deviations.

Fault Detection Experiments using IEEE 1149.6

The growing use of high-speed differential interconnections has produced some very interesting challenges for assembly testing. These interconnections typically operate at very fast (Gigahertz) operating frequencies and frequently are coupled between devices through capacitor devices. This was termed "Advanced I/O" by the IEEE. The following Figure 9 shows how fundamental different these signals are compared to "singled-ended" digital logic supported by the IEEE 1149.1 standards.



Here is the definition of "Advanced I/O" taken directly from IEEE standard 1149.6.

Advanced I/O: Input/Output (I/O) circuits and protocols that are designed to convey digital information, The interconnections of which cannot , either by design or by common usage, be adequately tested with static digital signals such as those provided for in IEEE STD 1149.1

FIGURE 6 - IEEE 1149.6 DEFINITIONS

These IEEE 1149.6 boundary-scan tests mostly follow the high-level methods previously described and are designed to detect shorts, opens through applying test cases. Figure 10 shows two "simple" 1149.6 devices, each with a differential transmitter and receiver "pair", one that is interconnected to the other device.

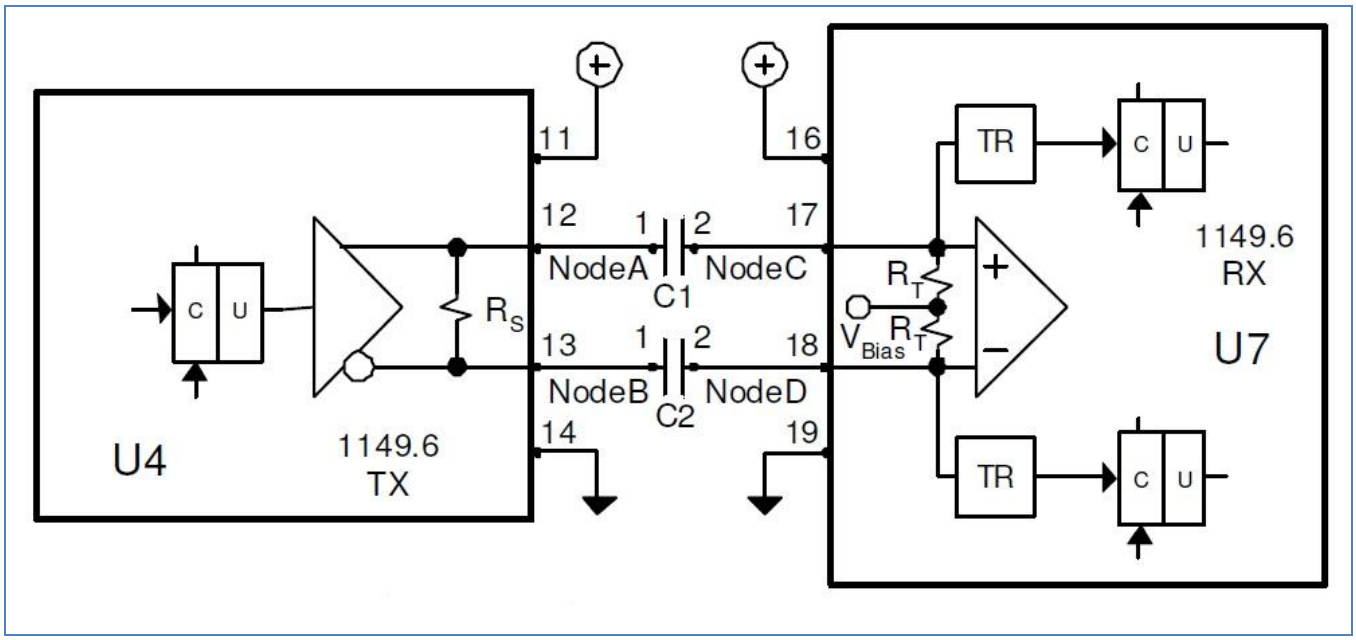


FIGURE 7 – IEEE 1149.6 EXAMPLE

In the case of a simple IEEE 1149.1 interconnect, the tested circuit topically would be four solder joints / pads, one for each device.pin and the power / ground pins if there are adjacent to the signal pins. In the case of this IEEE 1149.6 example, there are typically 12 solder joints and 4 devices involved, which include: coupling capacitors (C1 and C2), boundary-scan accessible differential interfaces (U4 pins 12, 13 and U8 pins 17, 18) and power (U4 pin 11, U7 pin 16) and ground (U4 pin 14 and U7 pin 19). Received signals utilize the concept of hysteresis because the high-speed signal is a self-clocking interface, which typically requires a continuous signal present to support timing synchronization (i.e. phase-lock). This means that the test receivers (TR) "remember" their previous signal state (hysteresis implies memory of what happened previously).

This fact is quite important for defect detection and effective diagnosis of assembly defects, especially in the case where boundary-scan is essentially running this in DC mode.

There can also be more assembly defects than just component shorts and opens. What if the coupling capacitor is not present or electrically connected on one end? What if the wrong value of coupling capacitor is loaded?

Experience has shown that claiming support of IEEE 1149.6 testing capability does not necessarily automatically imply that all assembly faults will be detected, especially with precision diagnosis. The following fault injection framework provides a way to concretely determine the actual detection of expected assembly faults and precision of the diagnostic messages. Doing this for a particular board is certainly a good deal of effort and it is the only method that provides real answers, not just "it should certainly do that".

TABLE 1 - 1149.6 DEFECT AND DIAGNOSIS EVALUATION

Defect Type	Fault	Possible Cause	Detected?	Precise Diagnosis?
U4 pins 12 or 13 open (TX)	open	Open solder joint, bad IC	**YES**	**YES**, signal pair identified
U4 pins 12 and 11 shorted (TX)	Short to VCC	Adjacent pins short	**YES**	**YES**, suspected short to power / ground reported!
U4 pins 13 and 14 shorted (TX)	Short to Ground	Adjacent pins short	**YES**	**YES**, suspected short to power / ground reported!
U4 pins 13 and 14 (TX)	Shorted	Adjacent pins short	**YES**	**YES**, signal pair identified
C1 pins 1 or 2 open	open	Open solder joint, missing capacitor	**YES**	**YES**, identified capacitor and signal pins as possible failures
C1 pins 1 and 2 shorted	Shorted	Adjacent pins shorted	**YES**	YES and special case failed due to IC not being fully IEEE 1149.6 compliant!
C1 and C2 adjacent pins shorted	Shorted	Adjacent pins shorted	**YES**	**YES**, identified correct capacitors and signal pins as possible failures
U7 pins 17 or 18 open (RX)	open	Open solder joint, bad IC	**YES**	**YES**, signal pair identified
U7 pins 17 and 16 shorted (RX)	Short to VCC	Adjacent pins shorted	**YES**	**YES**, suspected short to power / ground reported!
U7 pins 18 and 19 shorted (RX)	Short to Ground	Adjacent pins shorted	**YES**	**YES**, suspected short to power / ground reported!
Wrong value C1 or C2	Bad or wrong component	Miss-loaded pick and place, repair error	no	No defect reported

It is important to note that testing differential signals with boundary-scan requires much more than leveraging "high/low" test cases from IEEE 1149.1 testing. There are considerations on hysteresis setup, test cases for multiple receiver cells and detection of single solder and component faults. Note that cases have been discovered in which both differential signals would have to exhibit an assembly fault, before it might be detected! That clearly is not very likely and not obviously to anyone, until faults are injected and performance is measured.

Another item to point out is the test case for detection and diagnosis of a capacitor with shorted pins. Note, that while the absence of a capacitor is easy to detect with opens testing coverage, a shorted capacitor requires a special test that sets up hysteresis to expect AC behavior, which a shorted coupling capacitor will overwrite with its DC behavior.

The other item to note is that not every device that is labeled as IEEE 1149.6 capable means, that it supports the entire 1149.6 differential test capability. That has led to confusion and cases in which defect coverage is impacted.

Finally, due to the nature of limited information that can be extracted from the measurements, an extremely precise diagnosis is not always possible in the case of 1149.6 testing. In many cases, the diagnosis can only indict both signal interconnects, although a solder fault many only exist on one particular signal in the pair. This doesn't hamper repair, since the pair is co-located on the same devices, with the exception of the coupling capacitors. The latter are typically co-located, since signal pairs are routed close together. It is also important to note, that repair procedures can be leveraged to aid in quick fault isolation, based on physical access to component leads (such as capacitors).

Future Challenges

As IC and circuit complexity and density continue to increase (a' la "Moore's Law), this continues to challenge directly electrical test access and increase the need for access to built-in-test capability with specifically designed test access. Increasing signal speeds also are driving towards lack of external probing access and increasing need to perform not only structural, but parametric testing during manufacturing, since design margins are constantly tightened to squeeze out every bit of performance capability. Bed-of-Nail probing access will continue to be used to perform structural assembly testing with the most precise diagnosis for structural defects and will slowly decline in usage due to the aforementioned pressures on probing access.

There is a great deal of investment nowadays into utilizing IC Built-In-Self-Test (BIST) and utilizing advanced programming capabilities in CPU's and FPGA/CPLD components to extend testing capability. While claims of extensive defect detection abound, it is not always clear if precise diagnosis is a strong attribute of these forms of assembly testing. As with boundary-scan, the ability to test something may imply defect detection, but diagnosis must be engineered into the tests towards the goal of precisely identifying assembly faults. Fortunately, new measurement standards are being worked upon to facilitate development of ever more sophisticated test cases and diagnosis methods. IEEE standards in development and proposal stage include IEEE 1149.8.1, IEEE P1149.1 (for 2012) and IEEE 1687 are helping to provide the next generation of assembly test and diagnostic capability.

SUMMARY

In the context of printed circuit assembly testing, it seems common to assume that fault detection and printed circuit assembly fault diagnosis are equivalent. An advanced boundary-scan test designed to precisely detect an assembly fault requires a great deal of test circuit simulation / analysis, combined with actual boundary-scan test capability of the IC's and multiple sources of testing information. Stating that a particular circuit or assembly is "tested" doesn't mean that the resulting failure message will lead to a precise and useful diagnosis.

Fundamentally it is quite useful to validate a particular boundary-scan test solution, by thorough insertion of likely assembly faults to determine if they are truly discovered AND the resulting diagnostic message is usable by an assembly repair technician as well as the manufacturing or design engineers.

References

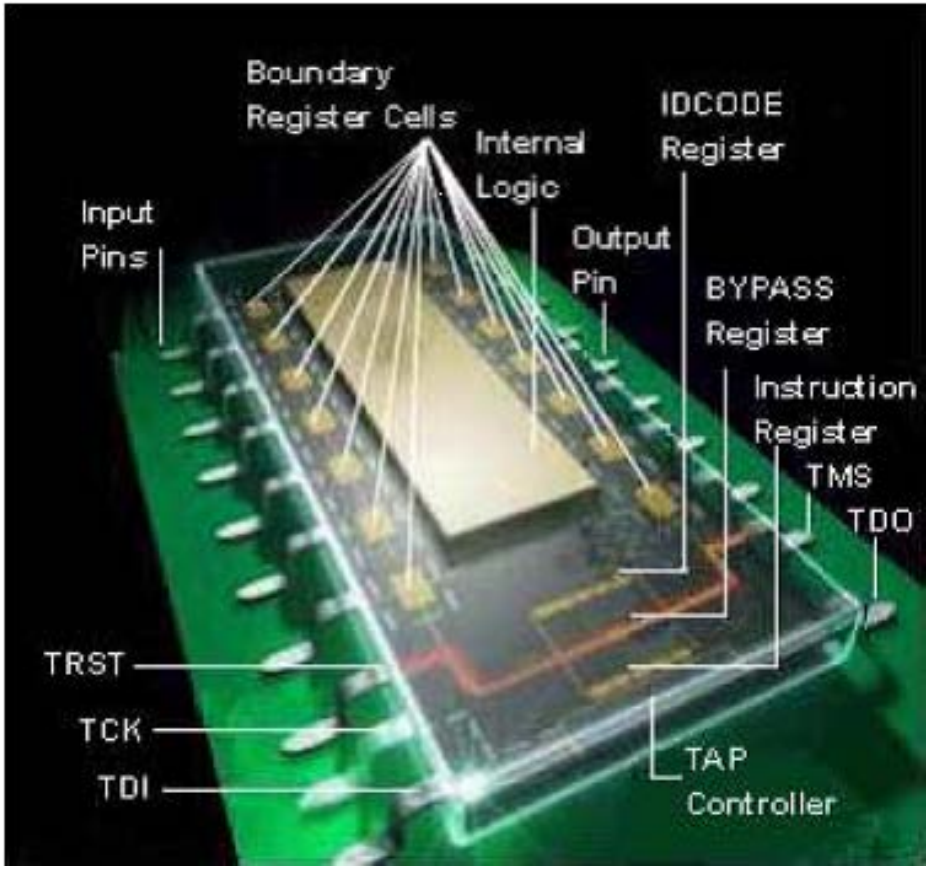
1. Agilent Technologies 3070 User Manuals – Copyright 1989-2011
2. 1149.1-1990 IEEE Standard Test Access Port and Boundary-Scan Architecture -- http://standards.ieee.org/findstds/standard/1149.1-1990.html
3. 1149.6-2003 IEEE Standard for Boundary-Scan Testing of Advanced Digital Networks -- http://standards.ieee.org/findstds/standard/1149.6-2003.html
4. Kenneth P. Parker, "The Boundary-Scan Handbook, 3rd Edition" 2003
5. Jun Balangue, "Successful ICT Boundary Scan Implementation", Circuits Assembly, September 2010
6. Jun Balangue, "Boundary Scan Development Steps", Circuits Assembly, December 2010
7. Kenneth P. Parker, "Defect coverage of boundary-scan tests: what does it mean when a boundary-scan test passes?", International Test Conference 2003.
8. K. Hird, K. P. Parker and B. Follis, "What Does It Mean when a Board Test Passes", International Test Conference 2002.

Boundary-Scan Advanced Diagnostic Methods

By Christopher Cain
Agilent Technologies

What is Boundary-Scan?

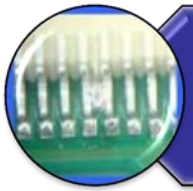
- Built-In-Test technique to support driving / receiving digital patterns between IC's without reliance on IC functions and minimal additional pins
- Standardized in 1990 as IEEE 1149.1
- Expanded to differential signals in 2003 as IEEE 1149.6
- Took many years to broadly adopt, now supported in majority of complex ICs



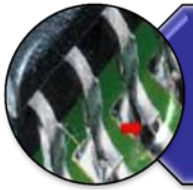
World of Boundary-Scan Expanding

Test Standards	Description	Purpose/Target Device
IEEE 1149.1	▪ Boundary-scan testing methods to enable ***digital IO stuck-at fault detection*** for IC interconnect defects.	▪ Digital device with boundary-scan enabled IO pins and supports the JTAG test port of 4 pins that is accessible to probing.
IEEE 1149.4	▪ Boundary-scan controlled ***mixed-signal testing interface***	▪ Additional test pins (2 additional) to support analog AC/DC measurements through enabled IO pins.
IEEE 1149.6	▪ Boundary-scan extension to support ***testing of "Advanced" IO pins.***	▪ Enables boundary-scan testing of high-speed differential (DC or AC coupled) IO pins, especially SERDES pins.
IEEE 1532	▪ ***In-system programming (ISP)*** through boundary-scan interface	▪ Allows concurrent programming of large memories (typically non-volatile) within programmable logic devices.
IEEE 1581	▪ ***I/O Loopback testing*** for devices that commonly do not have 1149.1.	▪ Enables boundary-scan IC's to validate interconnections to attached memory devices with loopback test.
IEEE P1149.1 (INIT Revision)	▪ Boundary-scan extensions to support ***complex device initialization and post-test pin quiescence.***	▪ IO interfaces and power management features in today's IC's require more sophisticated initialization sequences to prepare the device and PCAs for safe/reliable testing.
IEEE P1149.8.1	▪ Boundary-scan extensions to support ***vector-less open fault measurements***.	▪ Enable IO pins to selectively toggle digital state to enable AC-coupled capacitive sensor (no direct electrical probe access) to measure solder open defects.
IEEE P1687	▪ Boundary-scan extensions to support ***efficient access to user-defined registers and internal instrumentation***.	▪ Enables description and much more efficient access to IC BIST and Embedded Measurement capabilities increasingly designed into complex IC's.

Advanced Boundary-Scan for Detection of Assembly Faults



Shorts



Opens

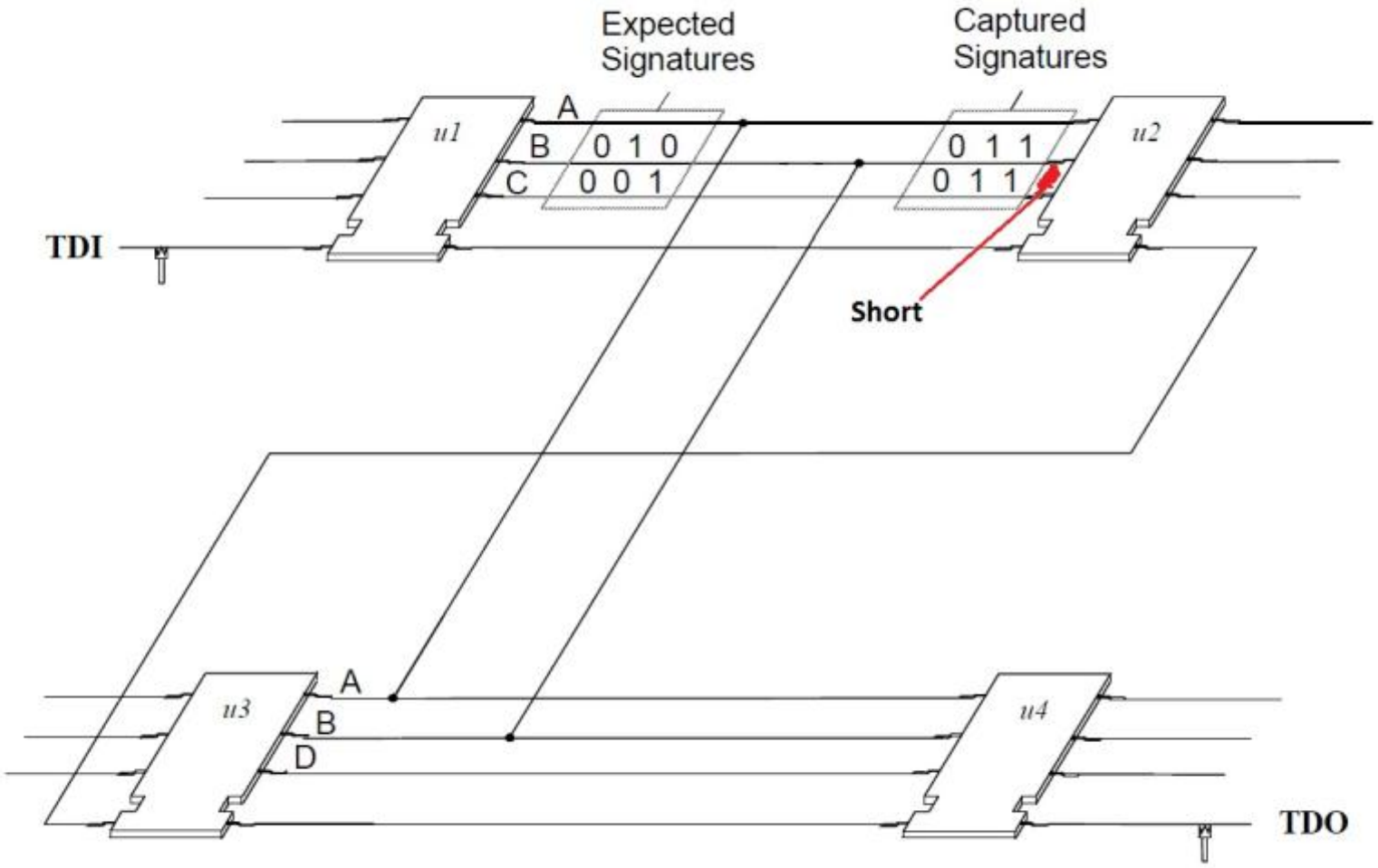
Miss-placed components

Bad / wrong components

Boundary-Scan Sequence

- Shorts detection and precise diagnostics
- Simple opens detection and precise diagnostics
- Complex opens detection and precise diagnostics
- Component defect detection and precise diagnostics
- Complex BIST and Embedded Test to extend fault detection

Advanced Shorts Detection and Precise Diagnostics

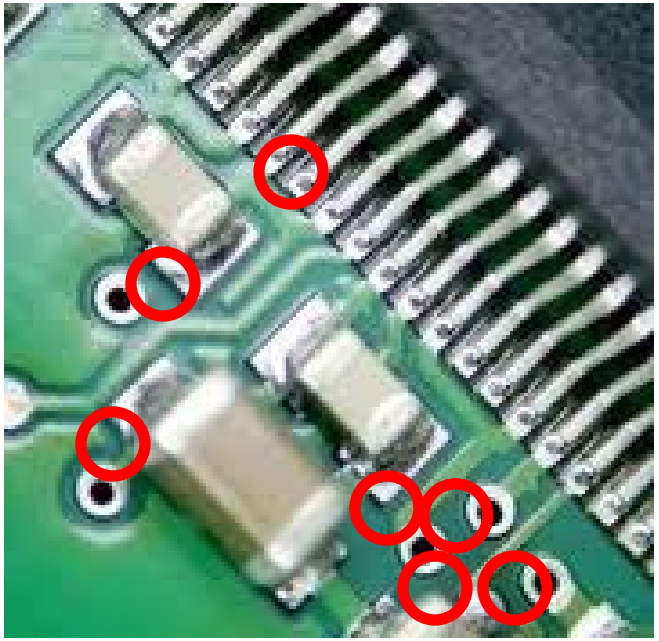


Shorts Test Diagnostics

Jan 09 17:40:06 2011

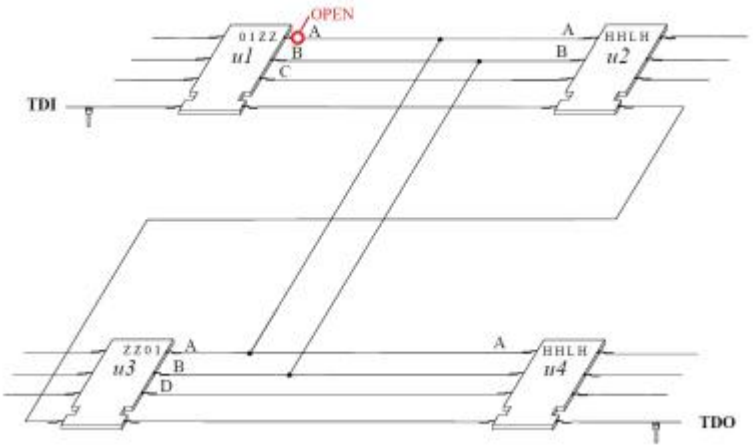
Boundary-scan shorts test u1_u4 FAILED
SHORTS FAILURE DETECTED

Short has been detected between the following nodes: B and C, probably near pin u2.2



Diagnosis precision through “shorting radius concept”

Advanced Opens Precise Diagnostics

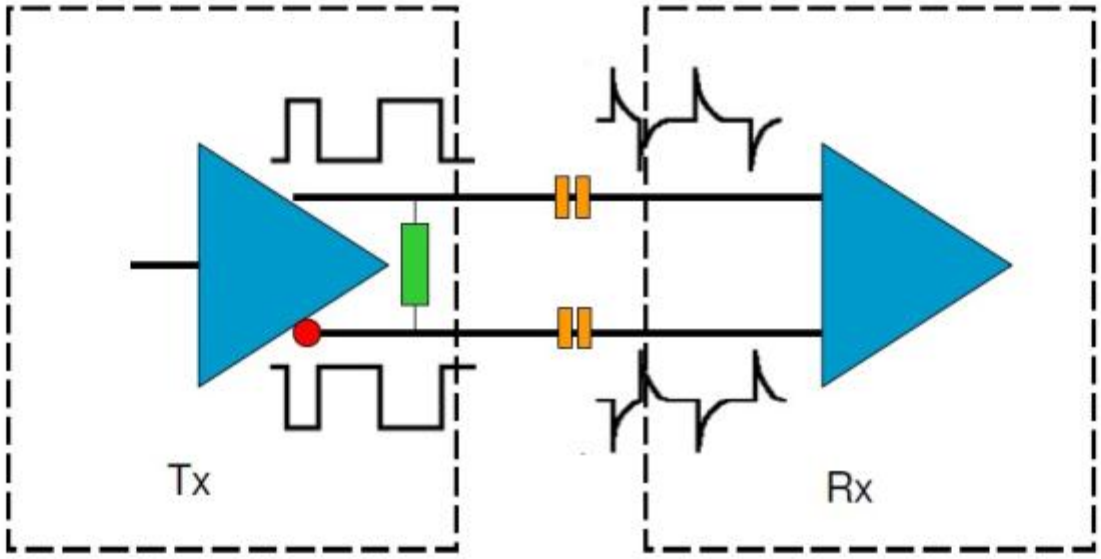



```
----------------------------------------
Jan 09 17:42:07  2011
----------------------------------------
Test  u1_u4_bus FAILED
The following pins are detected open:
u1.10
----------
```

- Test methods designed for maximized fault detection AND precise fault diagnosis
- Automatically generated from boundary-scan capability BDSL and net-list, models and extensive digital circuit simulations to generate test cases using minimum needed scans

Node	Power Bits Eliminates Aliasing to Ground or VCC		Counting Bits Primarily Distinguishes one Node From Another				Complement Bits Reduces Incidence of Aliasing Between Active Nodes		
A	0	1	0	0	0	1	1	1	0
B	0	1	0	0	1	0	1	0	1
C	0	1	0	0	1	1	1	0	0
D	0	1	0	1	0	0	0	1	1

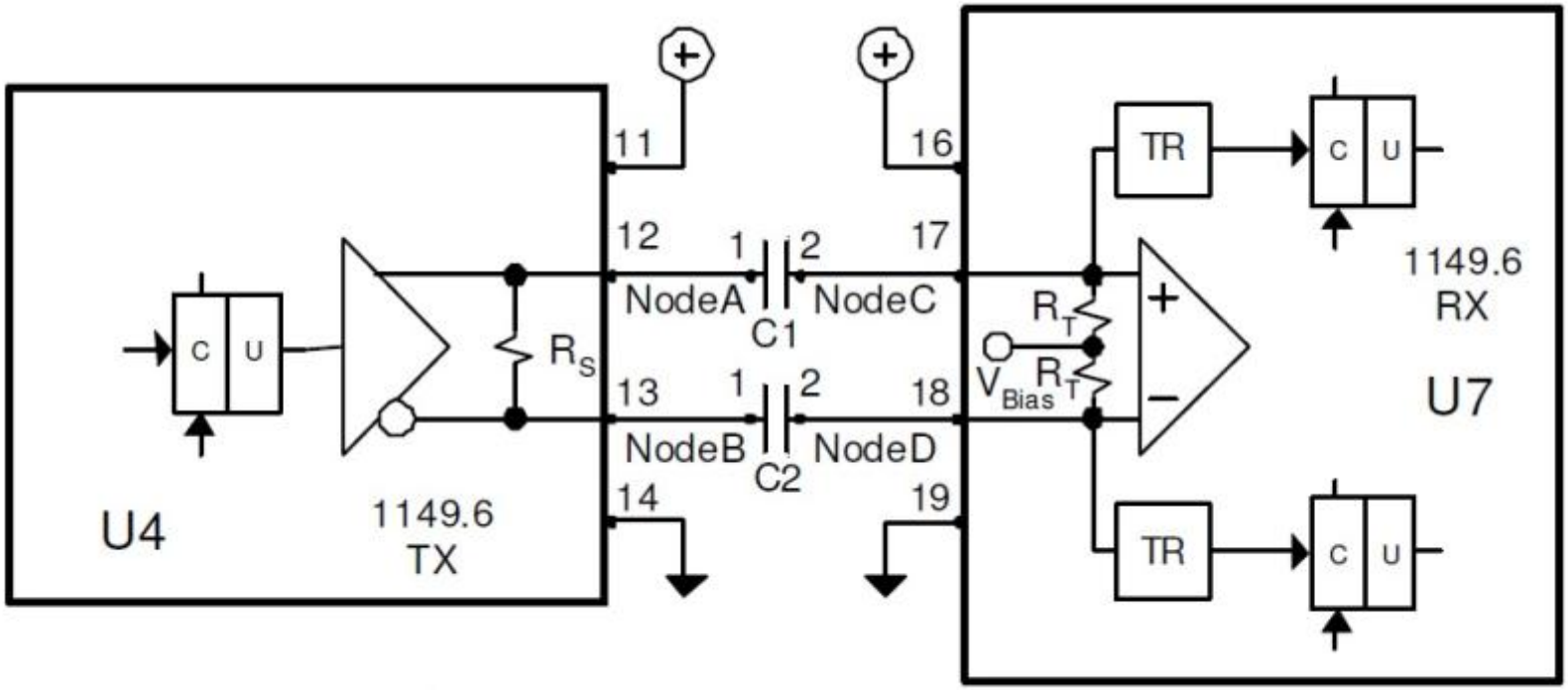
Advanced 1149.6 Boundary-Scan Testing



Here is the definition of “Advanced I/O” taken directly from IEEE standard 1149.6.

Advanced I/O: Input/Output (I/O) circuits and protocols that are designed to convey digital information, The interconnections of which cannot , either by design or by common usage, be adequately tested with static digital signals such as those provided for in IEEE STD 1149.1

Advanced 1149.6 Boundary-Scan Testing Example

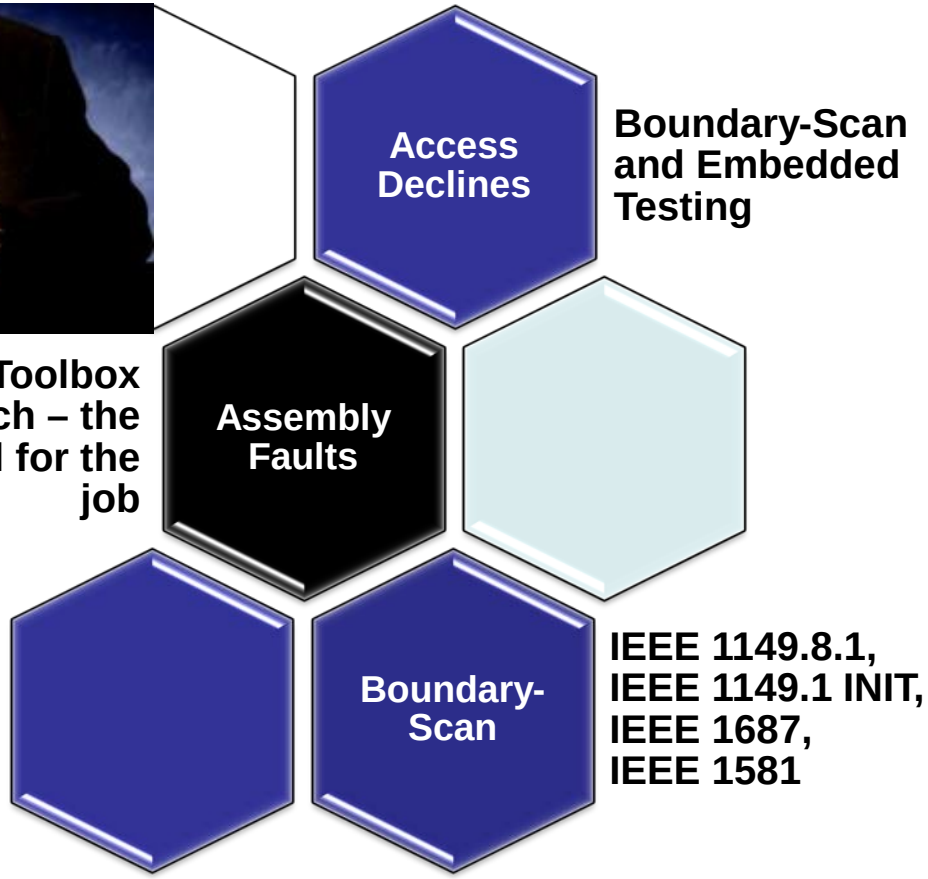


Advanced 1149.6 Boundary-Scan Assembly Fault-Injection

Defect Type	Fault	Possible Cause	Detected?	Precise Diagnosis?
U4 pins 12 or 13 open (TX)	open	Open solder joint, bad IC	**YES**	**YES**, signal pair identified
U4 pins 12 and 11 shorted (TX)	Short to VCC	Adjacent pins short	**YES**	**YES**, suspected short to power / ground reported!
U4 pins 13 and 14 shorted (TX)	Short to Ground	Adjacent pins short	**YES**	**YES**, suspected short to power / ground reported!
U4 pins 13 and 14 (TX)	Shorted	Adjacent pins short	**YES**	**YES**, signal pair identified
C1 pins 1 or 2 open	open	Open solder joint, missing capacitor	**YES**	**YES**, identified capacitor and signal pins as possible failures
C1 pins 1 and 2 shorted	Shorted	Adjacent pins shorted	**YES**	YES and special case failed due to IC not being fully IEEE 1149.6 compliant!
C1 and C2 adjacent pins shorted	Shorted	Adjacent pins shorted	**YES**	**YES**, identified correct capacitors and signal pins as possible failures
U7 pins 17 or 18 open (RX)	open	Open solder joint, bad IC	**YES**	**YES**, signal pair identified
U7 pins 17 and 16 shorted (RX)	Short to VCC	Adjacent pins shorted	**YES**	**YES**, suspected short to power / ground reported!
U7 pins 18 and 19 shorted (RX)	Short to Ground	Adjacent pins shorted	**YES**	**YES**, suspected short to power / ground reported!
Wrong value C1 or C2	Bad or wrong component	Miss-loaded pick and place, repair error	no	No defect reported

The Future

Toolbox approach – the right tool for the job



Boundary-Scan and Embedded Testing

IEEE 1149.8.1,
IEEE 1149.1 INIT,
IEEE 1687,
IEEE 1581

Summary

- Don’t assume fault coverage by itself guarantees precise assembly fault diagnostics!!
- Advanced boundary-scan can work wonders – fault injection experiments are the only way validate
- Future challenges are being addressed and you will need more tools to craft the right test strategy