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Ceramic to Plastic Packaging

As electronic products increase in functionality and complexity, there is an emphasis on affordability, miniaturization, and energy efficiency. The telecommunications, automotive, and commercial electronic markets are the leading drivers for these trends. These markets see high volume manufacturing with millions of units priced to the fraction of the cent. The choice of the packaging material for the electrical components for these markets can have a substantial effect on the cost of the final product. Therefore plastic encapsulated components are almost universally used in non-military applications over the conventional ceramic or metal electronic packages.

Traditional electronic components are hermetically sealed for environmental protection. The earliest component packages were made of glass, such as the cathode ray tube (CRT) which used a glass enclosure to seal out the atmosphere and maintain a vacuum. Today, full hermetic packages are typically made of metal, ceramic, or a combination of both. Ceramics and metals provide the only proven fully hermetic packages. While both provide a high barrier to gases and moisture, metals provide the ultimate protection. Although the raw metals can be quite inexpensive, the manufacturing methods used for metal packaging generally add substantial cost to the package. Metal packages are mostly machined, cavity style packages which are ultimately sealed with a lid. They are typically the highest cost but most reliable option for electronic packages in harsh environments.

Ceramic hermetic packages cost less than metal packages and provide most of the performance and protection of metal with a few advantages of their own. Ceramics are excellent electrical insulators and are less costly because the base material can be pre-formed before firing, forming a hard high barrier solid. Ceramics are a popular material for both hermetic and non-hermetic packages which require thermal conductivity, high temperature stability, good planarity, and smoothness. Examples of traditional ceramic cavity packages are shown in Figure 1-1. One ceramic packaging option, Low Temperature Co-fired Ceramic (LTCC), is a multi-layer, glass ceramic substrate that is co-fired with low resistance metal conductors (such as silver or copper) at a low temperature, typically under 1000°C. This technology provides embedded inductors, resistors, and capacitors for functional substrates.

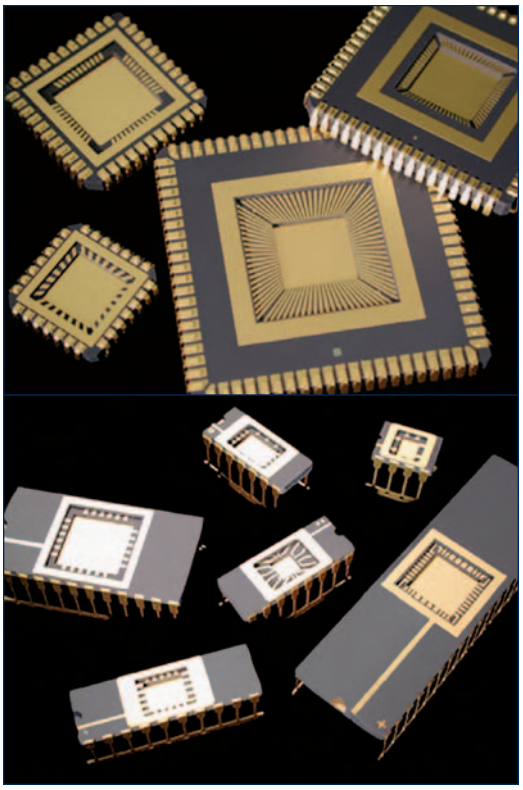

Figure 1-1: Ceramic Packages

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Ask the EMPF Helpline!

Cleaning No-Clean Fluxes Prior to Conformal Coating

Recently, a customer called the EMPF Helpline seeking advice for cleaning no-clean fluxes prior to applying a conformal coating.

The customer's assemblies were manufactured with a no-clean rosin based solder paste (ROL0) and were cleaned with an isopropyl alcohol (IPA) wash. After cleaning, a white residue was sometimes found in areas with high paste concentrations and was interfering with the adhesion of the conformal coating (Figure 2-1).

For conformal coatings to adhere properly, the printed circuit board (PCB) surface must be clean of fluxes and other residues. In addition, ionic contamination left by flux residues can lead to corrosion and dendrite growth, two common causes of electronic opens and shorts. Other residues can lead to unwanted impedance and physical interference with moving parts.

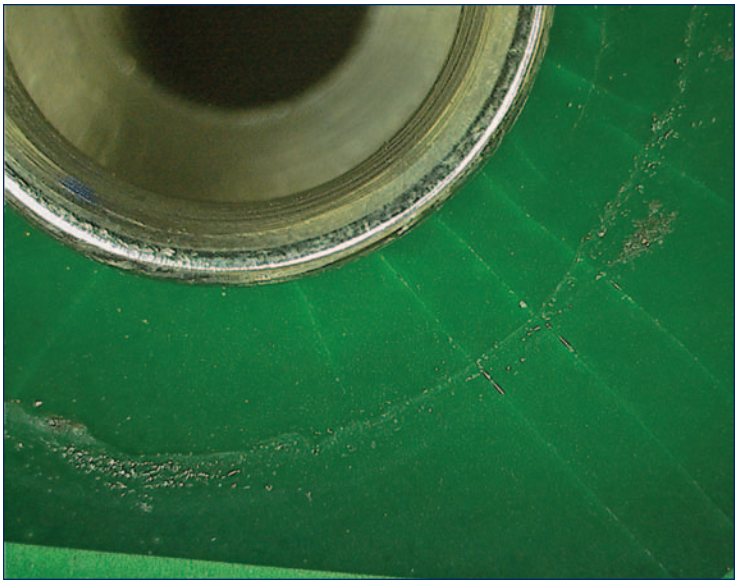

Figure 2-1: A white residue is often left after cleaning.

A conformal coating is only effective at preventing dendritic growth and corrosion if there are no ionic residues or active flux residues trapped under the coating. Since conformal coatings slowly absorb moisture, any residues that are present under the coating can facilitate the migration of metallic ions and affect PCB performance. Thus, all residues must be removed from the assembly before applying the conformal coating.

"No-clean" fluxes are also referred to as "low solid" or "low residue" fluxes. These fluxes are designed to leave a benign nonconductive and non-moisture absorbing residue behind, but only if properly heat activated. They are typically Rosin (RO) or Resin (RE) flux types with low (L) or moderate (M) activity levels. It is important to remember that "no clean" actually refers to the electronics manufacturing process where low solid fluxes are used. These electronic assemblies may or may not be cleaned.

No-clean fluxes are typically not very soluble in deionized (DI) water and IPA wash solutions since they are designed to leave behind non-moisture absorbing residues. The white residue left after cleaning a no-clean flux with IPA is essentially dehydrated flux. This white residue has the potential to be conductive and absorb moisture. The recommended cleaning method for no-clean fluxes is the use of saponifier at a 60ºC temperature and rinsing with plenty of low pressure steam and DI water. A saponifier is a soap ingredient which reacts with water to split insoluble rosin or resin esters into water soluble salts.

The EMPF generally recommends using a flux chemistry other than "no-clean" when the assembly will be cleaned. If a no-clean flux must be cleaned with IPA, the best advice is to add mechanical scrubbing to the cleaning process. Typically, this means the use of a brush and manual scrubbing. Since IPA is such a poor solvent of rosin, a better plan would be to use a solvent based aerosol cleaner. Some brands include Micro Care, 3M, Tech Spray, and Chemtronics. Some technicians prefer aerosol cleaners with "trigger grip" attachments that greatly reduce the amount of solvent required. Each specific flux has some cleaners that work best with them. The EMPF advises clients to call their local distributor for some samples and try each on the specific material that requires cleaning, then specify the use of the best material for the job.

The EMPF offers various analytical techniques (Resistivity of Solvent Extract (ROSE) Test, Ion Chromatography, Fourier Transform Infrared Spectroscopy, Surface Insulation Resistance) to determine the root cause of contaminant problems and to evaluate the effects of process or materials changes on cleanliness. More information about these services can be found on the EMPF web site, http://www.empf.org or by calling the EMPF technical staff at 610.362.1320.

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Rebecca Morris | Materials Engineer

Winning the Board Testing Task: Flying Probe versus Bed of Nails

In the world of automatic test equipment, there are two competing technologies to achieve board test: a bed of nails (BON) approach and the flying probe. Regardless of the approach, board testing itself is a key requirement for OEMs and a clear competitive advantage for contract manufacturers. For OEMs, board testing at both the component and system level is critical to assure the performance and reliability of the circuit board. If there are problems with a production build, catching and correcting these errors early saves time and money.

Contract manufacturers who possess board testing capability can offer a superior value package to their customers. This added capability helps enormously for prototype development by decreasing the time to market. First to market is often a decisive advantage. Many companies outsource all their manufacturing tasks to contractors, and if these contractors have the ability to both build and test circuit boards, the design and production can be confirmed in days rather than weeks and months.

In essence, the mechanical method of how the circuit board is presented and secured in either of the two types of electrical test machines defines the strengths and weaknesses of the two electrical test approaches.

With a BON test fixture, the circuit board is placed in a vacuum fixture or some similar device. The vacuum is turned on, the circuit board is pulled onto the conductors (or nails), and electrical contact is made simultaneously to all the test points (Figure 3-1). Input signals are sourced to the components through the conductors. Other conductors then read output signals to confirm the placement, identity, connection integrity and performance of the components and the electrical system. Usually, each circuit board requires a unique fixture.

With the flying probe test machine there is no fixture required. Circuit boards are placed and fastened in the flying probe machine. The flying probes are under computer control and move from component to component, checking electrical performance of the chips and the system. The probes are moved with three-axis, high powered linear motors to achieve electrical contact with the component under test (Figure 3-2). Electrical signals are sourced into the board with computer controlled flying probes and the resultant output signals are read with other flying probes. With the probes acceleration at seven "Gs" (224 feet per second squared), the term "flying" probe is no exaggeration. The machine then moves the probes to other test points on the board and the process is repeated. Locating the components on the board is performed with a vision system, and the machine identifies the location of the test points based on the board fiducials or other reliable locating point on the circuit board. Flying probe test machines have four or more moving electrical probes. Probes are built into the machine to access both the top and bottom of the board. The probes move extremely fast and can make up to 15 high speed tests per second. As with the BON, the probes make contact to the board to source signals to the components and read output signals.

The cost of a comprehensive test program centered on BON fixtures revolves around the base machine plus the number of different fixtures. Each unique circuit board requires a separate fixture and each modification of the circuit board usually requires modifying the matching fixture.

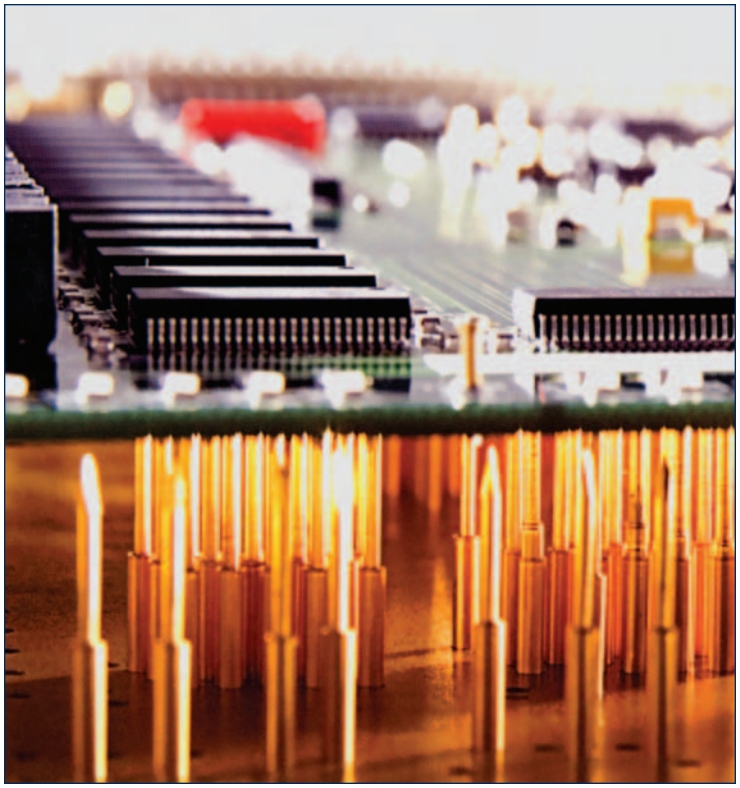

Figure 3-1: The circuit board rests on fixed, conductors or "nails."

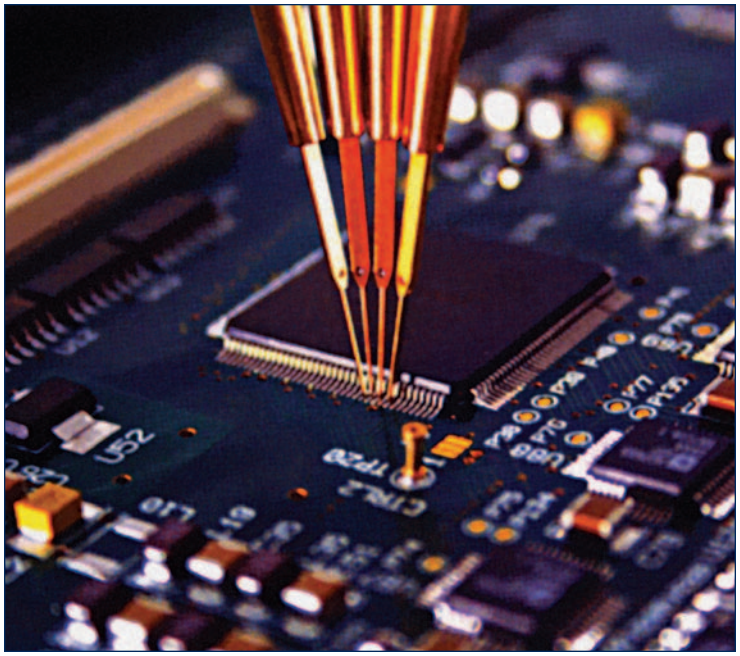

Figure 3-2: The probes are moved with three-axis, high powered linear motors to achieve electrical contact with the component under test. Photo courtesy of SPEA.

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Tech Tips: Thermal Profiling for Reflow

Reflow temperature profiling is the most important aspect of proper control of the solder reflow process. It may appear to some to be a magical art practiced by a select experienced few, who are able to divine the proper settings for a reflow oven by reading graphs as if they were tea leaves. This does not have to be true. This article outlines a systematic method by which engineers and technicians can implement a successful reflow process from scratch.

The most basic type of profile is a ramp-to-peak (RTP) profile as shown in Figure 4-1. This type of profile is one where the rate of temperature increase over time is virtually constant for the entire heated portion of the profile. An RTP profile type is very common and is the easiest type to implement. There are three critical parameters for all solder materials on an RTP profile: peak temperature, rate of temperature increase over time (slope), and time above liquidus.

The peak temperature is exactly what it appears to be: the highest temperature experienced during the reflow process. The slope is the rate of temperature increase over time during the reflow process. The time above liquidus parameter is the time spent above the temperature at which the solder alloy is fully melted. These parameters will vary based on the alloy (especially peak temperature and time above liquidus) and the flux formulation (especially slope). The primary source for these parameters is the manufacturer's data sheet for the solder paste that is used. In many cases, these specifications will provide an acceptable range. In some cases, only a minimum or maximum requirement is provided. This article will use a fictional solder paste that provides the following requirements: peak temperature of 240-255°C, profile slope of 0.8-1.0°C/second, and a time above liquidus of 30-60 seconds.

The first step of developing a reflow profile is to set the conveyor speed. This is the most important parameter to set correctly as any change during process development will invalidate all of the work accomplished to that point. The conveyor speed can be calculated as long as all the necessary information is available. The technician must know (or measure) the heated length of the oven and determine the required peak temperature and profile slope.

The next step is to calculate the time needed to reach the peak temperature by determining the difference between the peak temperature and room temperature and dividing that result by the slope. In our hypothetical example, the time to peak is (247.5 - 25) / 0.9 = 247.2 seconds. Notice that the midpoint was used for each range? This ensures that our calculated conveyor speed is near the center of the acceptable range.

Once the time to peak has been determined, the conveyor speed is calculated by dividing the heated length of the oven by the time to peak. Our hypothetical oven has 84 inches of heated length, resulting in a conveyor speed of 84 / 247.2 = 0.34 inches/second or approximately 20 inches/minute. The precision of the conveyor speed setting is not critical since the center of the range was used for peak temperature and profile slope, so rounding the value is acceptable. Once this value is determined, it will remain unchanged for the balance of the profile development.

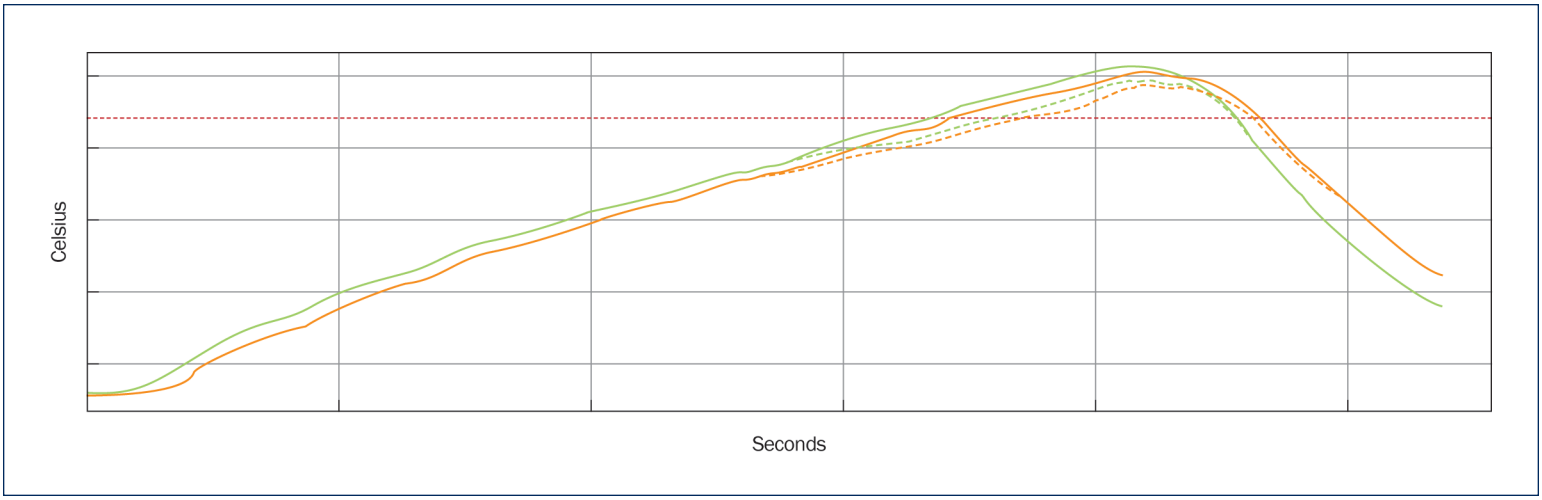

Figure 4-1:

The next task is to determine the goal temperature for the assembly at the end of each oven zone. In order to calculate the goal temperature at the zone exit, the technician must know the number of heated zones in the oven, the peak temperature desired, and the exit temperature of the previous zone. The calculation begins by determining the desired temperature rise for each zone, which is calculated by dividing the difference between the peak temperature and room temperature by the number of heated zones. In our example the oven has seven heated zones, so the calculation is (247.5 - 25) / 7 = 31.8 or approximately 32°C per zone.

The goal temperature for zone 1 is then calculated by adding the previous zone exit temperature (room temperature for zone 1) and the temperature rise per zone. For our example, this becomes 25 + 32 = 57°C. This is the

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Manufacturer's Corner: RMD Instruments

The LeadTracer Handheld XRF (Figure 5-1) by RMD Instruments Corporation is the optimal, first line screening tool for the Restriction of Hazardous Substances (RoHS) compliance. Light weight, portable, fast, and accurate, this XRF can be used for incoming inspection, in process testing, and final assembly verification.

X-ray fluorescence (XRF) analysis is a well established, non-destructive analytical technique for elemental analysis that has been used for over half a century. A vital part of the electronic assembly process, its ability to clearly identify the presence or absence of elements in a component or assembly is important in detecting counterfeit components or validating authentic ones. When a primary x-ray from a radioactive source strikes a sample, electrons are ejected from the inner shells, creating vacancies. To fill the vacancies and return to a stable state, outer shell electrons drop to the inner shell and give off a characteristic x-ray whose energy is the difference between the two shells. This energy is unique to each element and can be used to non-destructively measure the elemental composition of a sample. This process of emitting characteristic x-rays is called "X-ray Fluorescence," or XRF. By using a radiation source instead of an x-ray tube, the LeadTracer XRF system produces the higher energy K-shell characteristic x-rays that are not masked by some common elements which could cause a false negative. The handheld unit can provide the spectrometric data through components and packaging without needing to disturb the actual component or the packaging materials.

The need for screening incoming materials and monitoring the assembly process against intrusion of non-RoHS compliant materials is essential and must be done in an efficient, non-destructive yet accurate way. In addition to the critical task of measuring and confirming the presence or absence of trace materials in a specimen (such as certain RoHS restricted elements: Cr, Br, Pb, Hg, and Cd), XRF analysis can help prevent counterfeit electronic components from entering the supply chain.

Components manufactured under false trade names are creating another type of challenge for the electronics manufacturing industry. These components are often made from the same external materials as real parts and pass electronic functionality tests. However, material compositions of this group may be substandard, thus compromising capabilities in extreme temperature and pressures. In the majority of cases, the substandard components do not contain expensive elements such as gold (Au), bismuth (Bi), tantalum (Ta), and silver (Ag). Instead, the more expensive elements are often replaced by less costly materials such as lead (Pb) or palladium (Pd).

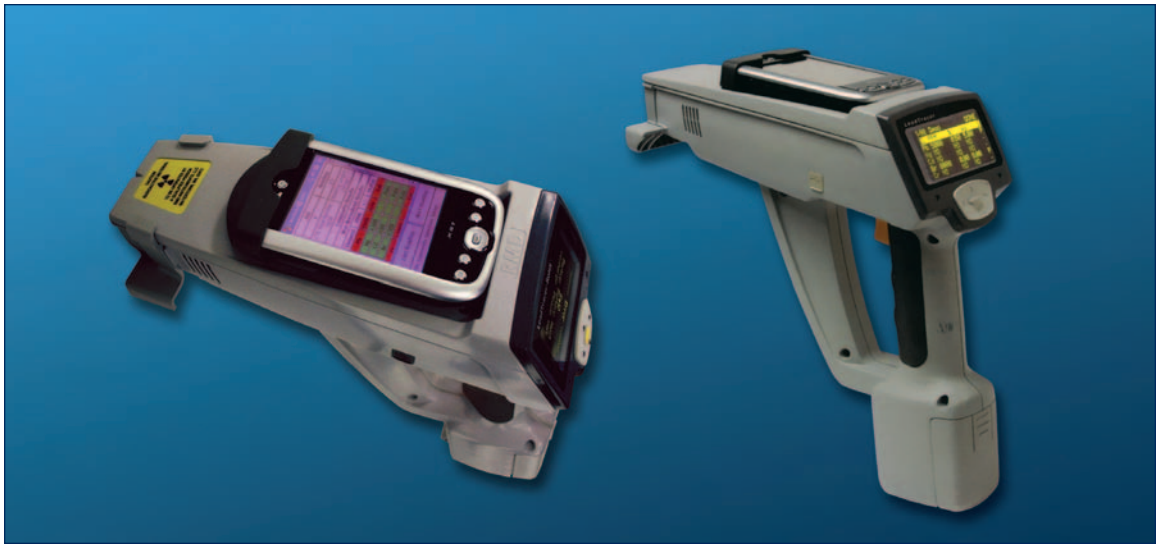

Figure 5-1: LeadTracer Handheld XRF

Whether the information sought from x-ray fluorescence is to qualify materials for RoHS or another critical analysis, the data provided by XRF is a pre-requisite for such conclusions. The portable, handheld XRF analyzer by RMD Instruments is a very good choice when considering a tool to provide quick and easy elemental analysis.

For more information on the LeadTracer handheld XRF unit by RMD Instruments or to schedule a demonstration, please contact the EAB Coordinator, Ken Friedman, at 610.362.1200, extension 279 or via email at kfriedman@aciusa.org.

Ken Friedman | EAB Coordinator

Design of Experimentation for Affordability

Affordability is not exactly the primary word which comes to mind when discussing the use of design of experiments (DOE) principles, but is generally accepted as a necessary part of the engineering activities required in the development of a product or process. However, a number of studies have indicated that the cost savings derived from a well deliberated experimental design can be substantial in the initial stages where the conditions or parameters of a process are determined. Some studies have shown a greater than 50% cost savings compared to the more conventional means of trial and error approaches to process development. At the EMPF, we have found the use of DOE techniques fundamental in eliminating extraneous costs otherwise spent on unnecessary testing.

Case Study

Recently a project was undertaken at the EMPF to qualify a surface mount technology (SMT) process to meet the IPC Class 3 qualifications for solder wetting, ionic cleanliness, and visible flux residue. The contract manufacturer had introduced a new SMT solder process that subsequently exhibited electrical failures after production of the first articles. The following is an anatomy of the investigation and experimental process used to determine the acceptable process parameters.

1. Failure Summary

The preliminary investigations that led to this study revealed that the first articles produced by the contract manufacture had evidence of the following:

- Electrical failure after *biased highly accelerated stress test* (HAST) testing due to electromigration causing *corrosion*.
- Unacceptable amounts of *voiding* in the BGA devices.
- Occasionally, severe cases of solder *de-wetting* on surface pads.

2. Causes - Brainstorming Session

Through this experiment, it was determined that 10 factors (Table 6-1) in the SMT process could possibly account for the various failures that were identified. If two term interactions are taken into consideration, the amount of experimental runs would exceed 1000; a very costly and time consuming experiment. When so many combinations and iterations are involved, it is critical to choose a good software program that will evaluate the probability of detecting variability on the basis of the factors and interactions chosen for the experiment. This will allow you a minimum amount of experimental runs to maintain a statistically valid experiment. It is important to note that decreasing the number of experimental runs will decrease your probability of detecting a response, as you increase the number of factors and interactions. Therefore, it is important to choose a program that gives you the flexibility to design an experiment around the interactions and main effects most likely to affect the process or product quality.

3. Type of Designs

There are a number of experimental design variations that can be tailored specifically to the type of data that is required.

A *D-Optimal* Design (Figure 6-1A) places the majority of its experimental runs at the extremes (70-80%), with a few in the center regions. This model is appropriate for *screening designs* where a bolder approach in assigning factorial levels may be warranted. The average variance, relative to error, would be lower on the extremes, but this model would be inappropriate for quadratic effects.

The *I-Optimal* Design (Figure 6-1B) minimizes the average variance prediction within the interior regions of the experiment, making it more appropriate for *Response Surface Designs*. Most of its runs are located in

Factors				
Name	**Role**	**Values**		
Belt Speed	Continuous	1		3
Peak Temperature	Continuous	230		260
Ramp Rate	Continuous	5		20
Cool Rate	Continuous	1		3
Paste	Categorical	X		Y
Surface Finish	Categorical	Tin	OSP	Gold
Solder Volume	Continuous	2		6
Cleaner Temperature	Continuous	40		75
Cleaner Concentration	Continuous	5		20
Cleaner Type	Categorical	Aqueous		Semi-Aqueous

Table 6-1: Factorial Values

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Ceramic to Plastic Packaging

(continued from page 1)

Plastic packaging uses organic materials for environmental protection. In contrast to hermetically sealed packages, organic material usually contacts the active element (or a thin inorganic barrier layer) in the plastic package.

Post molded and pre-molded plastic packaging is the dominant technology in packaging today. Post molded plastic packages are formed after chips are attached to the mounting surface, such as a metal leadframe, and electrically connected. Typically, a thermosetting epoxy resin is used to form the package body around the chip and mounting surface. There are many types of post molded packages due to the popularity and versatility of polymers. However, this process does subject the die and wire bonds of the package to the harsh molding environment.

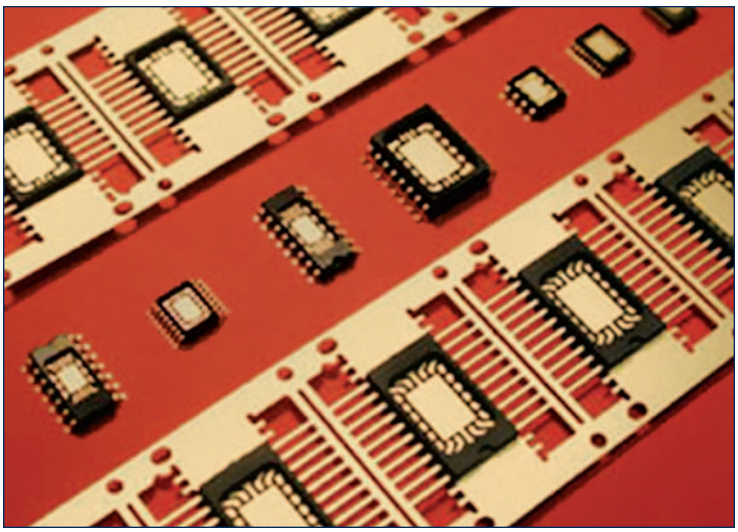

Figure 1-2: Pre-Molded Plastic Packages

Pre-molded packaging, as seen in Figure 1-2, provides a less harsh environment for packaging sensitive chips requiring a low cost assembly. The main element is that the chip and interconnects are decoupled from the molding process. The package is made by either a transfer molded process using a thermosetting epoxy resin or an injection molding process. The chip and interconnects are then encapsulated to protect them from the environment. This can be a die coating or a flow coating to fill the entire cavity. In some cases, a plastic lid is used to seal the plastic package. The injection molding process easily produces cavity style packages that are increasingly useful for newer optical and electromechanical chips (MEMS). The injection molding process allows for precise cavity packages to be manufactured automatically. Injection molding typically has a faster throughput than transfer molding and is less labor intensive.

The drive towards plastic packing in the commercial electronics industries is due to three inherent advantages of plastic packaging: cost, size, and weight. Plastic packaging designs are amenable to a high volume, automated process, which in conjunction with the low cost of the material, result in low manufacturing costs per unit. In addition, there is a well established, high volume manufacturing infrastructure for plastic packaging technologies, which also reduces the unit cost of plastic packaging.

The constant trend in electronics is to become smaller and lighter as evident in the cell phone and the consumer electronics industries. Plastic packages, on average, weigh approximately half of a ceramic or metal package of the same type. This reduction in weight and package footprint helps designers reduce the overall weight of their electronic product. The short lead times for plastic packages result in greater availability of the packages in the market, especially in surface mounted devices (SMD).

As with any growing technology, there are concerns with plastic packaging technologies. Unlike metal and ceramic packages, plastic packages are not hermetic. Recent advancements have developed polymeric materials that can reach nearly hermetic levels of environmental protection. These packages can pass the required helium leak tests, however, they are not considered hermetic because moisture can diffuse into the package over time. This is of concern for hermetic applications, specifically in the military. The ability of moisture to penetrate the plastic package causes reliability and storage life issues. Another concern is the long term reliability of plastic packages when exposed to the harsh environments and higher temperatures seen in military applications.

The use of liquid crystal polymer (LCP) has become a popular low cost, near hermetic packaging option. LCP is a thermoplastic which can withstand temperatures of 260°C or more without melting or distorting. Because LCPs are thermoplastic, they can be injection molded around leadframes to create a cavity. After the die and interconnects are added to the package, the air cavity can be sealed with a ceramic, plastic, metal, or glass lid. The lid can be sealed with an epoxy or some other method, such as heat or laser.

LCP has a 10 times lower moisture diffusion barrier than epoxy and absorbs only 0.02% moisture. LCP also has excellent dimensional stability when molding and creates precision parts having flat surfaces right out of the mold, without rework. Dimensional uniformity is a problem with ceramic packaging because of its high shrinkage during the co-firing process. In addition, LCP has a low dissipation factor and a dielectric constant of 3 to 4 compared to ceramics which have a dielectric constant of 4-13. LCP also has a low coefficient of thermal expansion (CTE) value.[1]

LCP has begun displacing some of the more expensive ceramic packaging applications and typically cost about 40% less than a ceramic package of the same package type. LCP has also begun to replace some of the high performance transfer molded applications.[1] Table 1-1 shows some of the properties of Vectra® C115 LCP from Ticona Engineering Polymers.

Testing of LCP packages have shown that they will pass the traditional gross and fine leak testing per the MIL-STD-883E standard. However, these tests do not consider outgassing, absorption, or permeability. As a result, LCP packages are considered near hermetic packages as compared to the fully hermetic ceramic and metal packages.[2]

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Ceramic to Plastic Packaging

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Property	Vectra® C115 LCP
Density	1.5g/cc
Melting Temperature	325°C
Coefficient of Thermal Expansion (Linear)	3.0 µm/m°C
Heat Deflection Temperature	250°C
Dissipation Factor	0.020 @ 1MHz
Dielectric Constant	3.1 @ 1MHz
Water Absorption	0.005%

Table 1-1: Properties of Vectra® C115 LCP

Hermetic packages, typically ceramic, have traditionally been used by the military. These ceramic packages provide high reliability under the severest environmental conditions. The rapid shift in the commercial industry to plastic components has caused defense contractors to evaluate the use of plastic packages in military applications. However, as the defense industry slowly makes the conversion from traditional hermetic packages to plastic encapsulated packages, it is not relaxing their expectations or specifications for performance. The defense contractor needs to know the limitations of the packages as it pertains to the specific application. Military applications that have extreme temperature variations, long storage life, hermeticity issues, or are considered mission critical should consider the proven ceramic technology. Other applications that are man-portable, ground based, or in a controlled environment can take advantage of plastic packaging technology.

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[1] Ross, Dick, John Roman, and Edson Ito. "Choosing the Right Material for RF Packaging." *Electronic Products.* 1 Nov. 2007. <http://www2.electronicproducts.com/Choosing_the_right_material_for_RF_packaging-article-farcrjrticona-nov2007-html.aspx>

[2] Riley, George. "Wafer Level Hermetic Cavity Packaging." *Advanced Packaging Magazine.* May 2004. <http://www.flipchips.com/tutorial43.html>

Paul Bereznycky | Senior Packaging Engineer

Winning the Board Testing Task: Flying Probe versus Bed of Nails

(continued from page 3)

Delivery time to purchase a BON fixture usually runs about two to four weeks with prices from $5,000 to $10,000.

For prototype work, the delivery time associated with acquiring the fixtures can be a problem. Large size fixtures can be especially expensive and difficult to acquire promptly. Test points are a necessity for a BON vacuum fixture. On high density boards with very small components (e.g., 0402s) bunched close together, circuit boards must have enough room for the pins on the bed of nails fixture to make contact with the pads on the boards.

The BON fixture requires test points or test pads on the circuit boards to assure a good electrical contact. Special attention must be given to board layout to assure access to the components and a comprehensive test program. Also for BON testing, these test pads should be flat and parallel to the circuit boards. This is required since the conductor nails are stationary and the circuit board is moved vertically to make electrical contact. If the conductors are forced to make contact on an angled surface, the conductor can be deformed and the electrical contact will be intermittent and unreliable.

A key characteristic of the flying probe machines is that they can achieve reliable electrical contact on non-flat surfaces and can target very small areas with good repeatability. The probes themselves are under direct machine control and are constructed on an angle. The probe point has a targeting accuracy of +/-3 mils (.003"), so the probe point can be programmed to land on the leg of a component or any other point on the circuit board.

The cost of the two approaches (flying probe versus fixed bed of nails) can differ widely. If a manufacturer has a single modest complexity board with low to medium volumes of production, the start-up cost for the bed of nails is far less than a flying probe machine. If a company has large production runs and a low mix of boards, the bed of nails would be the most cost effective approach. If board throughput is the decisive issue, the bed of nails has a performance advantage since all the test points make contact immediately.

The BON testing approach is less favorable when there are short runs of individual products but high overall volume of these products. Rapid changeover favors the flying probe because a fixture is not required and all the required component set-up information is provided in the CAD (computer aided design) data.

It is not uncommon for OEMs to outsource both circuit board layout and construction while controlling the design tasks themselves. This avoids the cost of acquiring manufacturing capabilities. The contract assembly house that has the ability to offer testing and documentation of the performance of the customer's circuit board can provide the necessary assurance of a quality build.

To summarize, where the project requires dedicated testing of large quantities of circuit boards and board throughput is the decisive requirement, a test strategy utilizing a BON may clearly be the most compelling. The initial cost is reasonable, and test coverage can be complete assuming the test points are designed into the board. Also, where low initial cost is critical a BON will be the best choice.

The flying probe machines excel in a test environment where there is a high mix and low quantities of different circuit boards to test and where turnaround time does not allow for building a dedicated fixture. The flying probe is also a superior choice where several revisions of a design are expected and the time between prototype designs must be held to a minimum. The initial cost of a flying probe machine is substantially higher than the initial cost of a base machine using the BON approach. Due to the exceptional flexibility and speed of the flying probe, it may be the more cost effective approach; however, the cost of the machine is higher than a BON based machine.

A state of the art SPEA Flying Probe machine with four test probes and the capability of performing up to 15 tests per second is available for demonstration at the EMPF factory facility. Please contact Ken Friedman at 610.362.1200, extension 279 or via email at kfriedman@aciusa.org.

Mike Prestoy | Senior Applications Engineer

Upcoming Course

Boot Camp

A: March 1-5 | ***B***: March 8-12

Designed to provide electronics manufacturing personnel with intense, hands-on training in every aspect of the electronics manufacturing process. Experience setting up screen printers, programming and placing components using automated equipment, profiling reflow ovens and wave soldering machines, and selecting various types of cleaning processes. Engage in decision-making exercises relating to process options including flux considerations, cover process control tools, troubleshooting and cause/effect.

Contact the Registrar via:
phone at **610.362.1295**, email at **registrar@empf.org**
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Tech Tips: Thermal Profiling for Reflow

(continued from page 4)

temperature the assembly should reach by the end of the first zone, but the oven should be set to a higher value. There will be a difference between the oven set point and the temperature of the assembly during the reflow process. A good starting point is approximately 20°C higher, so the oven's first zone should be set to 80°C. The subsequent zones can remain at their default value (typically room temperature) for now. Once the first zone has reached operating temperature, a measurement can be taken by passing an assembly with thermocouples and a data logger through the oven. After each pass, the assembly's temperature is compared to the goal and the oven set point is adjusted, as necessary, until the assembly exits the first zone at approximately 57°C. This process is repeated for each zone in sequence.

It is important to ensure that the slope of the profile curve remains constant throughout the zone. A profile that flattens at the end of any zone indicates the assembly is nearly reaching temperature equilibrium in that zone. This can be due to a high convection rate which should be reduced, if possible. If the oven does not have adjustable convection rates, the conveyor speed will need to be increased. If the conveyor speed is changed, the expected slope needs to be recalculated to ensure it is within specification. This is accomplished in the same manner as the determination of the conveyor speed, except the conveyor speed is now a known value, and the expected slope is the unknown value. If the conveyor speed is changed, the entire zone setting process should start again from zone 1.

The final two (or three) zones, typically, are where reflow occurs and is where the profile should exceed the liquidus point of the solder. The entire time the profile spends over the liquidus point of the solder is counted towards the time above liquidus parameter. This includes the time after the peak temperature (which will occur at the end of the last heated zone). The peak temperature and time above liquidus are typically adjusted by modifying the temperatures of the last two or three zones. This is accomplished through trial and error. However, by following the system described in this article the trial and error portion of developing a profile is limited to minor changes in a limited number of zones at the end of the process.

The EMPF can provide assistance developing reflow processes; call the Helpline at 610.362.1320, email helpline@empf.org, or visit http://www.aciusa.org/forms/helpline_form.php.

Jason Fullerton | Sr. Product and Applications Engineer

Design of Experimentation for Affordability

(continued from page 6)

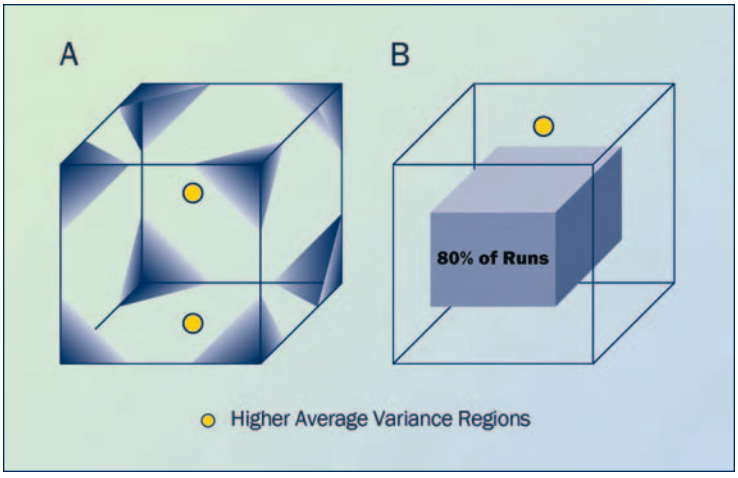

Figure 6-1: A shows D-Optimal Design. B depicts I-Optimal Design

the inner regions of the design space, making it better to predict responses in the inner region

4. Choosing Factorial Values

The number of factors involved in the DOE can be either categorical or continuous in nature. If conducting a screening experiment, the continuous variables should be assigned values which represent the reasonable extremities of the process parameters. It is always easier to interpolate predictive responses than to extrapolate, where quadratic or cubic effects are not taken into account.

5. Responses

The three response variables for this experiment were wetting, cleanliness, and flux residue. The responses were numerically assigned a number from one through 10, determined through a combination of visual

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(continued from page 10)

Summary of Fit	
RSquare	0.975486
RSquare Adj	0.909096
Root Mean Square Error	0.535099
Mean of Response	7.268889
Observation (or Sum Wgts)	90

Analysis of Variance				
Source	**DF**	**Sum of Squares**	**Mean Square**	**F Ratio**
Model	65	273.46094	4.20709	14.6931
Error	24	6.87195	0.28633	**Prob > F**
C. Total	89	280.33289		< .0001

Table 6-2: Wetting Response

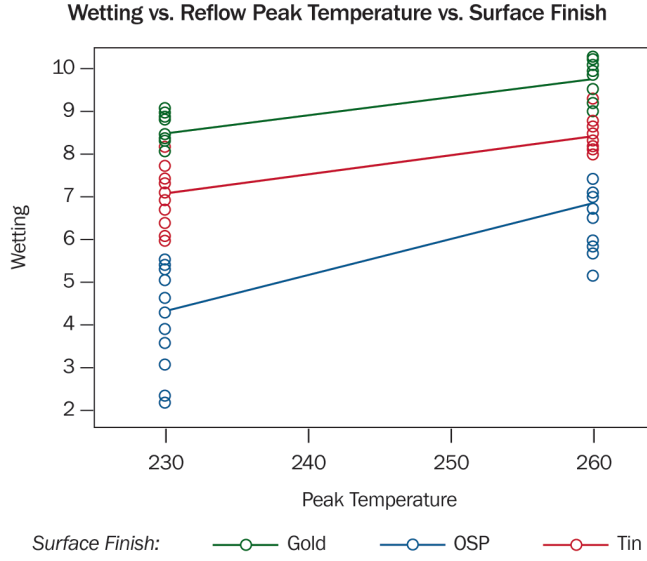

Figure 6-2: Surface Finish vs. Peak Temperature

inspection and ionographic testing. It may be beneficial at times to assign a numerical value to a categorical response to obtain the necessary statistical data to determine variability. In the case of this experiment, a numerical metric was easily adaptable. The value of one indicated the worst case response, with the value of 10 indicating the best response. For example, the best wetting, the cleanest assembly, and the least amount of residue all had values of 10.

6. Interpreting the Model Data

Assuming a general linear model is used, there are two important statistical tables to consider. The *summary of fit* and *analysis of variance* (Table 6-2) will present the statistical relevance of the experimental model based on the particular response variable and factors used in the DOE. In this example the wetting response was used.

The three key areas to look at are:

- *F-Ratio 14.693* Which indicates the wetting response produced a high signal to baseline noise.
- *Prob<.0001* Which indicates a very strong probability that the wetting responses were not random in nature.
- *R-Square adj* In this case, the 0.909 indicates that 90% of all the variance around the means is accounted for within the model.

Essentially, the model showed a very strong response in wetting for the assigned factorial values.

7. Interpreting Factorial Data

Using similar metrics to the model, it was determined that the greatest wetting response was produced by changing the peak temperature, followed by the ramp rate. The interaction between Peak Reflow Temperature and Surface Finish (Figure 6-2) also had a significant response. For this customer's particular assembly, an electroless nickel immersion gold (ENIG) finish at a higher process temperature improved wetting to the surface pads.

8. Conclusion

There were other elements to this experiment, but for the purpose of this article, it suffices to show that with the use of DOE techniques, the engineers at the EMPF were able to determine the proper process conditions for a valued customer. This enabled them to save time and money on their product development.

The EMPF conducts training classes on various aspects of DOE, design for manufacturability (DFM), and statistical process control (SPC). For more information please contact the Registrar at 610.362.1295, via email at registrar@empf.org or visit the web at www.aciusa.org/courses.

Carmine Meola | R&D Projects Manager

ACI Technologies, Inc.

2010 Class Schedule

National Electronics Manufacturing Technology Center of Excellence

IPC Training Center

Electronics Manufacturing

Boot Camp A
March 1-5
May 3-7
September 13-17
November 1-5

Boot Camp B
March 8-12
May 10-14
September 20-24
November 8-12

CIS/Operator

IPC J-STD-001
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IPC A-610
Call for Availability

IPC 7711/7721
Call for Availability

IPC/WHMA-A-620A
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April 19-21
June 28-30
September 27-29
December 20-22

High Reliability Addendum

IPC J-STD-001 DS
CIT Certification
January 15
February 26
April 16
May 28
August 27
October 8

IPC CIT Challenge Test

January 29
February 19
April 23
June 18
July 16
August 20
October 15
November 19
December 17
Call for Additional Availabilities

IPC Certifications CIT/Instructor

IPC J-STD-001
CIT Certification
January 4-8
February 1-5
March 15-19
April 26-30
June 7-11
July 19-23
August 30 - September 3
October 18-22
December 6-10

IPC J-STD-001
CIT Recertification
January 13-14
February 24-25
April 14-15
May 26-27
July 14-15
August 25-26
October 6-7
November 17-18
December 15-16

IPC A-610
CIT Certification
January 4-7
February 8-11
April 19-22
June 14-17
August 16-19
October 11-14
December 6-9

IPC A-610
CIT Recertification
January 11-12
February 22-23
April 12-13
May 24-25
July 12-13
August 23-24
October 4-5
November 15-16
December 13-14

IPC A-600
CIT Certification
January 26-28
March 22-24
June 21-23
September 7-9
November 29 - December 1

IPC 7711/7721
CIT Certification
January 25-29
March 22-26
July 26-30
October 25-29

IPC 7711/7721
CIT Recertification
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Contact the Registrar for course information and pricing: *phone:* 610.362.1295 *email:* registrar@empf.org

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