DOE FOR PROCESS VALIDATION INVOLVING NUMEROUS ASSEMBLY MATERIALS AND TEST METHODS

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ABSTRACT:
Selecting products that have been qualified by industry standards for use in printed circuit board assembly processes is an accepted best practice. That products which have been qualified, when used in combinations not specifically qualified, may have resultant properties detrimental to assembly function though, is often not adequately understood. Printed circuit boards, solder masks, soldering materials (flux, paste, cored wire, rework flux, paste flux, etc.), adhesives, and inks, when qualified per industry standards, are qualified using very specific test methods which may not adequately mimic the assembly process ultimately used. It is recommended that products used in combination on a printed circuit assembly be qualified in combination to the extent necessary to provide a full understanding of interactions that may occur in the product. IPC J-STD-001 provides good guidance with regards to process validation testing although said testing is limited to the Appendix of the document.

J-STD-001D, Appendix C focuses on process validation via Surface Insulation Resistance (SIR) Testing. The limitation to relying solely on SIR testing is its inherent inability to detect possible assembly issues which could result from employed combinations of printed circuit boards, solder masks, soldering materials (flux, paste, cored wire, rework flux, paste flux, etc.), adhesives, and inks. The authors' intention with this paper is to describe two Designs of Experiments (DOE's) that were developed for process validation. The first relies on SIR testing as the sole means of qualifying the final assembly. The second explores the use of a broad range of tests chosen to closely represent the end use application.

DOE #1 was based upon the SIR testing procedure as per ANSI/J-STD-004, IPC-TM-650 2.6.3.3A the method which is also specified in J-STD-001. The scope of the test method is to determine the degradation of electrical insulation resistance of PCB specimens after exposure to specified materials. Since during the normal manufacturing process, a board assembly is exposed to a number of chemicals, for this DOE the standard SIR test coupons were prepared in such a way as to mimic a "typical" chemical mix that a board assembly may come in contact with during assembly. This involved applying the appropriate chemicals in the typical process order using appropriate process conditions.

Table 1 outlines the types of products that were used in combination.

Variable	Number of Suppliers
FR4 SIR test boards with HASL traces	1
Solder Paste	3
Solder Mask	1
Adhesive	2
Cored Repair Wire	3
Wave Flux	4
Wash	Y/N
Repair Flux	2
Encapsulant	1

Table 1. DOE #1

The one-week static 85°C / 85%RH SIR test was performed although frequent monitoring of the insulation resistance (IR) values was added. One of the more significant findings as a result of this experiment was an interaction between the solder mask and a specific solder paste that was not observed between any of the other product combinations. Although both the mask and the paste individually met the IPC standards, the combination of the two, led to the formation of corrosion products.

DOE #2 included various combinations of materials but it also included numerous test methods due to the types of products being utilized. Table 2 outlines the types of products that were used in combination

Variable	Number of Suppliers
FR4 Test Boards with Bare Copper Traces and HASL Traces	1 (Single and Double-sided)
Conductive Ink Traces	With and without
Solder Masks	4

Table 2. DOE #2

The following tests were run on the boards to determine process compatibility and the ability of the materials to withstand pre-determined environmental exposures:

- Visual Examination
- Resistance to Electromigration
- Surface Insulation Resistance
- High Temperature Life
- Thermal Shock
- Gaseous Contaminants
- Tape Adhesion
- Continuity
- Insulation Resistance

Telcordia, ASTM and IPC standards were used as guidelines for all of the testing. The Electromigration test was run for 500 hours at 85°C / 85%RH with a 10 V_{DC} bias. The SIR test was run for four days at 35°C / 85%RH. IR measurements were performed at 50 V_{DC}. The test was extended to 1000 hours for some coupons due to an adverse outcome observed. The high temperature life test was run for 500 hours at 135°C. One thousand thermal shock cycles were run between -65°C and +125°C with 15-minute dwells and immediate transfer between temperature extremes. The gaseous contaminants exposure was performed per Telcordia GR-63-CORE, requirement R4-61 for equipment exposed to outdoor air. The most significant find based on this series of tests was a corrosion reaction observed in relation to placement of the conductive ink traces.

Key words: Assembly Process Validation, Compatibility Matrix, Compatibility Testing, Compatibility Design of Experiment (DOE)

INTRODUCTION

Original Equipment Manufacturers (OEMs) and Contract Manufacturers (CMs) typically invest significant amounts of time and money deciding which material sets will work best in their assembly processes. They investigate and decide upon a list of potential materials that have been approved per industry standards, such as, laminates approved per IPC-4101, solder masks approved per IPC-SM-840, conformal coatings approved per IPC-CC-830, and soldering materials approved per J-STD-004, 005 and 006. Once the list of potential materials is developed, initial studies are run on the assembly line to determine if the products function well together and should be considered for inclusion in the list of potentials. The combinations are processed together and the best sets of materials are selected. For some, this is the end of the process validation. Often, there is no testing performed to prove the long-term reliability of the new process materials used in combination.

Industry use of conductive inks has grown in recent years. Development of low resistance, high conductance inks, using primarily silver, curing at relatively low temperatures and in very short times, have allowed the technology to spread from electronic packaging applications such as RFID and tamper seals and flexible current carrying traces, to printed circuit board technology and populated communications circuitry. The increased use of this technology has led to particular challenges in determining proper manufacturing techniques to ensure long-term product reliability. Obstacles to successful implementation include the increased likelihood of corrosion and possible negative interactions with other materials. These concerns make even stronger the case for testing to determine interaction characteristics and ensure process validation.

The first DOE that will be discussed involves performing compatibility testing on selected assembly materials. This compatibility testing was performed by application of the products to customer-supplied solder mask coated IPC-B-24 boards. The test boards were built by the OEM's supplier and the laboratory applied the products in specified combinations. In the second DOE, processing was performed by the OEM, and the laboratory performed the subsequent testing.

BACKGROUND

Numerous industry experts with various fields of experience have reported the importance of compatibility testing and process validation. The following was presented in a Polyclad-Enthone *Imaging Technologies Update* Bulletin: "True system compatibility of a conformal coating and solder mask is determined by subjecting a solder masked test vehicle to ***all*** chemical and thermal conditions present in the assembly process. It is especially important to evaluate conformal coating adhesion on PWBs that have experienced the particular assembly production process employed. ….the post-solder paste reflow residues, post-wave solder flux residues, and other intermediate chemistries that remain on the PWB surface in no-clean assembly operations may interfere with conformal coating cure and adhesion. EACH step of the assembly process may impact the adhesion between a soldermask and the subsequent conformal coating materials placed on the board."[1] In actuality, the assembly chemicals can affect more than conformal coating adhesion; they can affect assembly function.

For those concerned with the move to RoHS (Restriction of Hazardous Substances) compliance, compatibility testing and process validation has been more generally accepted as a necessary evil. Lead-free processing was a very new endeavor, and it was understood that the standard materials used for tin-lead processes may not withstand the lead-free processes, thereby, affecting the long-term reliability of the product. As described in the *EMS Forum on Lead-Free PCB Assembly: Guidelines for Suppliers Transitioning to*

RoHS Compliant Components, there should be several compatibility/reliability tests performed when moving to a lead-free process including the following[2]:

- Handling, Packing, Shipping and Use (per IPC/JEDEC J-STD-033A)
- Solderability testing (per IPC/EIA J-STD-002, current revision)
  a) Both no-clean and aqueous clean solder paste and wave solder flux should be included.
- Solder joint reliability testing (per IPC-A-9701)
- Mechanical shock and vibration (per AEC-Q100-Rev E/Mil-Std 883)
- High temperature storage (per AEC-Q100-Rev E/JESD22-A103-A)
- Tin whisker growth (Reference document: "Test Method for Evaluating Tin Whisker Growth on Plated Surfaces, Rev. 6.1", until applicable industry standards become available

The DOE that is developed to validate the assembly process, as well as confirm compatibility and long-term reliability, will differ based upon your material set, your process characteristics and your end-use application. Industry standards should be used as a guideline to develop a DOE that fits the assembler's needs.

DOE #1: PROCESS MATERIAL COMPATIBILITY

DOE #1 was based upon the IPC J-STD-001 Appendix and used SIR testing to determine assembly process compatibility issues. The IPC-TM-650, Method 2.6.3.3 one-week static 85°C / 85% RH SIR test was performed although frequent monitoring of the insulation resistance (IR) values was added to one SIR run. The test matrix is outlined in Appendix A. Table 3 includes the number of products tested in DOE #1. Table 4 provides additional details about the products tested.

Products Tested	Number of Suppliers
FR4 SIR test boards with HASL traces	1
Solder Paste	3
Solder Mask	1
Adhesive	2
Repair Wire	3
Wave Flux	3
Wash	Y/N
Repair Flux	2
Encapsulant	1

Table 3. Products Tested in DOE #1

Table 4. DOE #1 Product Details

Product	Description
Solder Paste 1	No-clean ROL0 63/37 Tin-Lead Type 3 Paste
Solder Paste 2	No-clean REL1 63/37 Tin-Lead Paste (Datasheet unclear)
Solder Paste 3	No-clean ROL0 63/37 Tin-Lead Type 3 Paste
Solder Mask	Liquid Photoimageable (LPI)
Adhesive 1	Epoxy Heat-cure Surface Mount Adhesive
Adhesive 2	Epoxy Heat-cure Surface Mount Adhesive
Repair Wire 1	No-clean ROL0 63/37 Tin-Lead Cored Wire
Repair Wire 2	No-clean ROL0 63/37 Tin-Lead Cored Wire
Repair Wire 3	No-clean ROL0 63/37 Tin-Lead Cored Wire
Wave Flux 1	Organic water-soluble, waterbased, no-clean ORL0 Wave Flux
Wave Flux 2	Organic water-soluble, water-based, no-clean ORL0 Wave Flux
Wave Flux 3	Organic no-clean ORL0 Wave Flux
Wave Flux 4	Organic no-clean ORL0 Wave Flux
Repair Flux 1	Halide-free No-clean Flux (No J-STD-004 classification)
Repair Flux 2	No-clean Water soluble flux
Encapsulant	Two-Part High Purity Liquid Epoxy Encapsulant

Table 4 continued. DOE #1 Product Details

Optimal process compatibility testing requires the assembler to prepare the test boards using standard assembly procedures. When this is not possible, typically due to lack of adequate equipment or time or due to cost considerations, the test laboratory may prepare the samples. The following procedure was used by the test laboratory to prepare the HASL IPC-B-24 for SIR testing:

1. The test coupons were scrubbed with a soft bristle brush for 60 seconds under running deionized (DI) water. The coupons were then rinsed thoroughly with 2-propanol and dried in an oven for 2 hours at 50°C.
2. A 0.2 mm thick stencil was used to print each sample solder paste onto the clean test coupons
3. Solder Paste 1 and Solder Paste 2 were reflowed by bringing the board from ambient temperature to 145ºC in approximately 1 minute. Each coupon was transferred to a second oven, and taken from 150ºC to 183ºC in approximately 2.3 minutes. Each coupon was then transferred into a third oven and ramped from 183ºC to 217ºC in approximately 45 seconds
4. Solder Paste 3 was reflowed by bringing the coupon from ambient to 150ºC in approximately 2 minutes, 45 seconds. Each coupon was then transferred to a second oven and was ramped from 183ºC to 215ºC in approximately 60 seconds
5. All repair wires were applied to two-thirds of the length of the first five traces of each pattern with the solder iron tip set at 650ºF

6. Fluxes 2, 3 and 4 were applied by submerging the comb side of the board in the appropriate flux. Each coupon was then allowed to drain in a vertical
7. position for 60 seconds. Each coupon was then preheated to a peak temperature of 105ºC in 45 seconds, and was then floated on a solder pot set at 260ºC for 3±1 seconds
8. Flux 1 was applied by spraying an equal amount of flux onto each comb pattern. Each coupon was then allowed to drain in a vertical position for 60 seconds. Each coupon was preheated to a peak temperature of 105ºC in 45 seconds, and was then floated on a solder pot set at 260ºC for 3±1 seconds
9. The rework fluxes were applied by adding one small drop to the center of the repaired traces. Repair wire was applied with the solder tip temperature at 650ºF. Each repaired trace that required Repair Flux 2 to be applied was touched with a clean solder tip set at 600ºF after application of the flux
10. The adhesive products were applied in two thin parallel lines crossing the central area of all traces. The adhesive was then cured at 150ºC for 4 minutes
11. The encapsulant was applied in a diagonal line across the repaired traces when Repair Flux 1 was NOT applied. When Repair Flux 1 was used, the encapsulant was applied at the end of the comb opposite of the repaired traces, and did not make contact with the Repair Flux 1. The encapsulant was allowed to thaw for 1.5 hours before application and was cured at 125ºC for four hours
12. Fluxes that required cleaning were held under a DI water faucet for 1 minute, and then were submerged in each of three 2-liter beakers holding 1800 milliliters of DI water at 60ºC and agitated for 1 minute. Each coupon was submerged in a final rinse beaker filled with DI water at 60ºC to complete the cleaning process.

Figure 1 depicts a typical SIR curve that was observed on the passing groups. Figure 2 depicts a failure that was observed on Groups HH through KK. In these groups, leakage current developed when the solder mask was used in combination with Paste 2. This particular combination was pinpointed as the problem as all other failing combinations had no products in common, yet all groups containing this paste/mask combination failed to meet the minimum SIR requirement of $1x10^8$ ohms. Paste 2 was eliminated from consideration because the OEM wanted to stay with their current mask supplier.

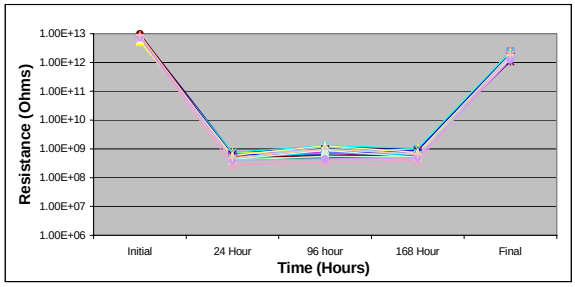


Figure 1. Typical Passing SIR Curve

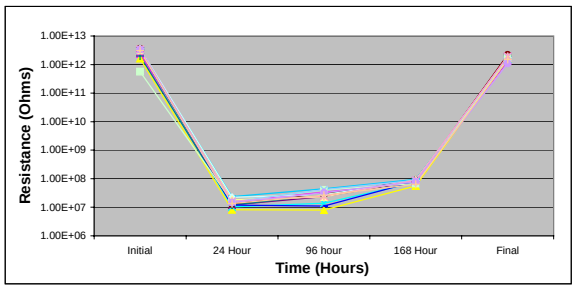


Figure 2. Low SIR Results Observed With Paste/ Mask Combination

DOE #2: PROCESS VALIDATION

DOE #2 involved a significant amount of testing based on the end-use needs and concerns of the OEM. The OEM had test boards produced that were a custom design and included SIR comb patterns.

Each single-sided (designated S) or double-sided (designated W) board tested was produced with one (1) of four (4) different solder masks, designated A, B, C, or D. Half of the boards were subjected to Mechanical Flex testing (20 mils/inch of length) (designated F) and half were not (designated N). Additionally, some boards underwent an "Acid Flex" test which was a more severe flex of 90 mils/inch of length.

All of the boards tested, with the exception of the sixteen (16) control boards, were also subjected to additional testing, designated E, L, T, or G, as follows:

E - Resistance to Electromigration, 85°C/85%RH with a $10V_{DC}$ bias for 500 hours (extended to 1,000 hours for some boards). Eight (8) of the "E" boards were subjected to Surface Insulation Resistance instead of Electromigration testing

L - High Temperature Life, 135°C for 500 hours

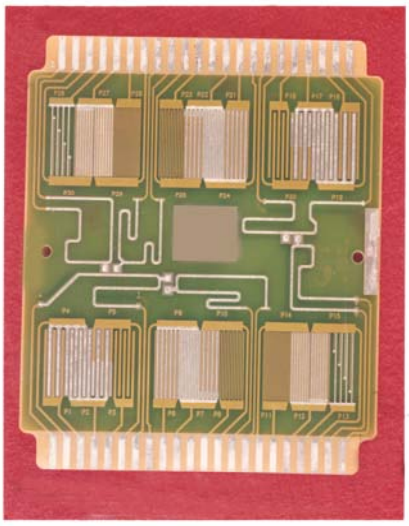
T - Thermal Shock, 1,000 cycles between -65°C and 125°C with 15-minute dwells

G - Gaseous Contaminants per Telcordia GR-63-CORE

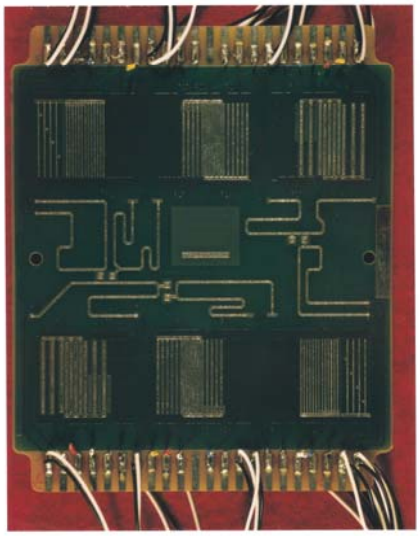
Each board was identified by solder mask (A, B, C, or D); flex or no flex (F or N); additional test, if any (E, L, T, or G); single or double sided (S or W); and a two-digit number

(01 through 26). For example, boards ANEW05 and ANEW06 were double-sided boards manufactured with solder mask A. They were not subjected to mechanical flex testing, but were subjected to Electromigration (or SIR) testing. Board CFS01 was a single-sided board manufactured with solder mask C. It was subjected to mechanical flex testing, but was not subjected to any further tests (a Control board).

Test patterns on each board (present on one or both sides of the board) included "snake" patterns to test the continuity of additive conductors, and "comb" patterns to test insulation resistance. The comb patterns had spacing ranging from 6 mils (0.152 mm) to 25 mils (0.635 mm).



Photograph 1: Overview of the test vehicle.



Photograph 2: Test vehicle with leads.

RELIABILTY CONCERNS UNCOVERED

The test plan performed to determine the reliability of an additive conductive ink process presently used by the customer (and under consideration for additional use) over four (4) different solder mask types, resulted in unacceptable increases in resistance of some additive traces. In addition, many of the test patterns developed visible corrosion during electromigration testing.

Three distinct failure mechanisms – corrosion, extraneous copper particulate, and loss of continuity were identified through failure analysis.

MECHANISM #1 - CORROSION

Based on the visual observations, SEM/EDS analyses, and additive process information, it was determined that the most likely source of the chlorine found in the corrosion products along the top edges of the copper traces in native Cu to ink test areas is the solder paste flux that was used to apply solder to the surface of the ink traces. Both paste fluxes that were tested contained very large quantities of chlorine. The primary constituents of the visible corrosion products on the electromigration test boards were found to be chlorine, copper, and oxygen.

The presence of the corrosion was found only on traces that lay next to additive traces (and, even more significantly, only on one edge of traces that have an additive trace on one side but not the other). It was determined that the additive process itself supplied the chlorine (or an unknown catalyst) to the corrosion process.

The supplier indicated that the chlorine was intended to "burn off" during the reflow process, and flux residues remaining on the boards were then removed with a hot tap water wash. Flux residues as a source of the chlorine also explains the increased severity of corrosion in more dense native Cu to ink areas. These areas receive more flux per unit area, and also have an exaggerated topography that is harder to clean.

The fact that the corrosion occurred primarily at the top edges of the native Cu traces (in native Cu to ink areas) can be attributed to the proximity of the copper and solder flux, thinner protective barrier, rougher topography, and higher energy levels and electric fields in these locations.

The fact that the severity of the corrosion varied with the polarity of the electrical bias indicated that the electric field is a key player in the chemical reaction process and/or transport of chlorine and copper.

Ion chromatography demonstrated that the additive process boards contain extremely high levels of chloride ions compared with boards which have not undergone the additive process. However, it appeared that much of the soluble chlorine was immobilized by the corrosion that occurred during the electromigration testing. The amount of chlorine extracted from the electromigration boards, though still high by industry standards, was much lower than that extracted from the control boards.

The 500 hour and 1,000 hour Electromigration test results and subsequent visual examinations indicated that the metal migration tended to occur vertically rather than horizontally. It is possible that the isolation material chemistry or topography inhibits dendrite formation. Some of the 1,000-hour boards began to show horizontal growth of the corrosion, but it still did not extend far from the top edges of the copper traces.

Microsections of boards with solder masks A, C, and D after 1,000 hours of electromigration testing showed that the corrosion had consumed less than 10% of the native copper depth. Even on boards with solder mask B, where the protection provided by the solder mask was completely lost, the corrosion depth was approximately 10%, except in isolated spots near the trace edges. Based on these test results, the additive process should be avoided on boards using solder mask B. Corrosion on these test boards was severe enough that conductive corrosion products could dislodge and cause shorts between assembly component leads.

Under the test conditions, the copper consumption appeared to be limited. However, different environmental conditions and extended durations may have differing effects.

MECHANISM #2 – EXTRANEOUS COPPER PARTICULATE

Generally low surface insulation resistance (SIR) values of the test boards, even before a bias was applied, and the low resistances recorded at a crossover point on the production boards tested for electromigration, present a larger threat to functionality under adverse conditions. The low SIR values may be related to the large numbers of copper particles left in between isolated traces by the additive process, or may indicate an intrinsically low SIR value of the additive process itself. With spacing at just over 5 mils, very little copper particle contamination was necessary to support a sizable leakage current under high temperature and humidity.

MECHANISM #3 – LOSS OF CONTINUITY

Based on the information presented, the greatest threat to long-term reliability of assemblies using the additive ink process is loss of continuity of the additive lines. This process provides conductivity by embedding Cu particles in a phenolic resin, then coating the exposed copper with solder. All of the High Temperature Life and EM snake patterns that experienced unacceptable increases in resistance during testing contained spots or areas where the solder coating (and possibly copper layer) appeared to be extremely thin, allowing oxidation of the underlying copper particles. The large surface area of the Cu particles compared to a solid copper trace makes them very vulnerable to oxidation. And this oxidation occurs at the particle surface, where Cu-to-Cu physical contact is essential to uninterrupted continuity. Very thin solder also allows essentially all of the tin in the solder to be bound up into brittle Cu_3Sn intermetallic that is vulnerable to cracking.

The additive lines performed very poorly during Thermal Shock testing. The thermal shock boards received no additional analysis, but probable reasons for the poor performance include the following:

- The different CTEs of solder, copper, phenolic, and isolation material created interfacial stresses that, over the course of temperature cycling, produced interfacial separation and/or cracking.
- The high temperature half of each cycle promoted Cu surface oxidation and growth of brittle Cu_3Sn intermetallic. Areas or spots of thin solder were especially vulnerable to cracking of the brittle intermetallic.

Acid Flex tests were conducted on control boards and on boards that had undergone Electromigration or Thermal Shock testing. Results of the Acid Flex tests suggested that occasional mechanical flexing by itself was not likely to cause loss of continuity of the additive lines. The control boards and boards that had undergone Electromigration testing experienced no loss of continuity during flexure. Damage experienced by the snake patterns during Thermal Shock testing, however, was evident during the Acid Flex tests. The majority of the Thermal Shock boards experienced unacceptable increases in resistance of the snake patterns during and after the Acid Flex tests.

CONCLUSION

Based on the case studies presented above, it is evident that compatibility testing and process validation should be performed on assembly materials to assure long term reliability. SIR allows assemblers to detect the possibility of leakage current development that may occur with various combinations of products that may not occur with each product when tested individually. With the observation that dendrites, the cause of short circuits, can form and burn off in a matter of minutes, it is imperative that frequent monitoring of the insulation resistance readings be added to detect possible intermittent short circuits.[3]

Additionally, when developing a DOE, the assembler should consider any extremes of the end-use environment or any special characteristics of the process that may require specialized testing to determine their effects on long term reliability.

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Appendix A: DOE #1

MATRIX SIR TEST

Coupons : IPC-B-24

Quantity	#	Solder paste	Solder mask	Adhesive	Repair wire	Wave flux	Wash	Repair flux	Repair wire	Wash	Encap.
2	A1,2	Board-washed	Mask 1	No	No	No	No	No	No	No	No
2	B1,2	Paste 1	Mask 1	No	No	No	No	No	No	No	No
2	C1,2	Paste 1	Mask 1	No	Repair Wire 1	No	No	No	No	No	No
2	D1,2	Paste 1	Mask 1	No	Repair Wire 1	Wave Flux 1	Yes	No	No	No	No
2	E1,2	Paste 1	Mask 1	No	Repair Wire 1	Wave Flux 2	No	No	No	No	No
2	F1,2	Paste 1	Mask 1	No	Repair Wire 1	Wave Flux 2	No	Repair Flux 1	Repair Wire 1	No	Encap
2	G1,2	Paste 1	Mask 1	No	Repair Wire 1	No	No	Repair Flux 2	No	Yes	No
2	H1,2	Paste 1	Mask 1	No	Repair Wire 1	Wave Flux 3	No	No	No	No	No
2	I1,2	Paste 1	Mask 1	No	Repair Wire 1	Wave Flux 3	No	Repair Flux 1	Repair Wire 1	No	No
2	J1,2	Paste 1	Mask 1	No	Repair Wire 1	Wave Flux 4	No	No	No	No	No
2	K1,2	Paste 1	Mask 1	No	Repair Wire 1	Wave Flux 4	No	Repair Flux 1	Repair Wire 1	No	No
2	L1,2	Paste 1	Mask 1	No	Repair Wire 2	No	No	No	No	No	No
2	M1,2	Paste 1	Mask 1	No	Repair Wire 2	Wave Flux 1	Yes	No	No	No	No
2	N1,2	Paste 1	Mask 1	No	Repair Wire 2	Wave Flux 2	No	No	No	No	No
2	O1,2	Paste 1	Mask 1	No	Repair Wire 2	Wave Flux 2	No	Repair Flux 1	Repair Wire 2	No	Encap
2	P1,2	Paste 1	Mask 1	No	Repair Wire 2	No	No	Repair Flux 2	No	Yes	No
2	Q1,2	Paste 1	Mask 1	No	Repair Wire 2	Wave Flux 3	No	No	No	No	No
2	R1,2	Paste 1	Mask 1	No	Repair Wire 2	Wave Flux 3	No	Repair Flux 1	Repair Wire 2	No	No
2	S1,2	Paste 1	Mask 1	No	Repair Wire 2	Wave Flux 4	No	No	No	No	No
2	T1,2	Paste 1	Mask 1	No	Repair Wire 2	Wave Flux 4	No	Repair Flux 1	Repair Wire 2	No	No
2	U1,2	Paste 1	Mask 1	No	Repair Wire 3	No	No	No	No	No	No
2	V1,2	Paste 1	Mask 1	No	Repair Wire 3	Wave Flux 1	Yes	No	No	No	No
2	W1,2	Paste 1	Mask 1	No	Repair Wire 3	Wave Flux 2	No	No	No	No	No
2	X1,2	Paste 1	Mask 1	No	Repair Wire 3	Wave Flux 2	No	Repair Flux 1	Repair Wire 3	No	Encap
2	Y1,2	Paste 1	Mask 1	No	Repair Wire 3	No	No	Repair Flux 2	No	Yes	No
2	Z1,2	Paste 1	Mask 1	No	Repair Wire 3	Wave Flux 3	No	No	No	No	No
2	AA1,2	Paste 1	Mask 1	No	Repair Wire 3	Wave Flux 3	No	Repair Flux 1	Repair Wire 3	No	No
2	BB1,2	Paste 1	Mask 1	No	Repair Wire 3	Wave Flux 4	No	No	No	No	No
2	CC1,2	Paste 1	Mask 1	No	Repair Wire 3	Wave Flux 4	No	Repair Flux 1	Repair Wire 3	No	No
2	DD1,2	No	Mask 1	No	Repair Wire 1	No	No	No	No	No	No
2	EE1,2	No	Mask 1	No	Repair Wire 2	No	No	No	No	No	No
2	FF1,2	No	Mask 1	No	Repair Wire 1	No	No	Repair Flux 1	No	No	No

Total 64

The first 64, B24 boards to be monitored frequently.

Coupon	#	Solder paste	Solder mask	Adhesive	Repair wire	Wave flux	Wash	Repair flux	Repair wire	Wash	Encap.
2	A1,2	Board-washed	Mask 1	No	No	No	No	No	No	No	No
2	GG1,2	No	Mask 1	No	Repair Wire 2	No	No	Repair Flux 1	No	No	No
2	HH1,2	Paste 2	Mask 1	No	Repair Wire 1	Wave Flux 2	No	No	No	No	No
2	II1,2	Paste 2	Mask 1	No	Repair Wire 2	Wave Flux 2	No	No	No	No	No
2	JJ1,2	Paste 2	Mask 1	No	Repair Wire 1	Wave Flux 2	No	Repair Flux 1	Repair Wire 1	No	No
2	KK1,2	Paste 2	Mask 1	No	Repair Wire 2	Wave Flux 2	No	Repair Flux 1	Repair Wire 2	No	No
2	LL1,2	No	Mask 1	Adhesive 1	No	Wave Flux 3	No	No	Repair Wire 1	No	No
2	MM1,2	No	Mask 1	Adhesive 1	No	Wave Flux 3	No	Repair Flux 1	Repair Wire 1	No	No
2	NN1,2	No	Mask 1	Adhesive 1	No	Wave Flux 3	No	No	Repair Wire 2	No	No
2	OO1,2	No	Mask 1	Adhesive 1	No	Wave Flux 3	No	Repair Flux 1	Repair Wire 2	No	No
2	PP1,2	Paste 3	Mask 1	No	No	No	No	No	No	No	No
2	QQ1,2	Paste 3	Mask 1	No	Repair Wire 1	No	No	No	No	No	No
2	RR1,2	Paste 3	Mask 1	No	Repair Wire 1	Wave Flux 1	Yes	No	No	No	No
2	SS1,2	Paste 3	Mask 1	No	Repair Wire 1	Wave Flux 2	No		No	No	No
2	TT1,2	Paste 3	Mask 1	No	Repair Wire 1	Wave Flux 2	No	Repair Flux 1	Repair Wire 1	No	No
2	UU1,2	Paste 3	Mask 1	No	Repair Wire 1	No	No	Repair Flux 2	No	Yes	No
2	VV1,2	Paste 3	Mask 1	No	Repair Wire 1	Wave Flux 3	No	No	No	No	No
2	WW1,2	Paste 3	Mask 1	No	Repair Wire 1	Wave Flux 3	No	Repair Flux 1	Repair Wire 1	No	No
2	XX1,2	Paste 3	Mask 1	No	Repair Wire 1	Wave Flux 4	No	No	No	No	No
2	YY1,2	Paste 3	Mask 1	No	Repair Wire 1	Wave Flux 4	No	Repair Flux 1	Repair Wire 1	No	No
2	ZZ1,2	Paste 3	Mask 1	No	Repair Wire 2	No	No	No	No	No	No
2	AAA1,2	Paste 3	Mask 1	No	Repair Wire 2	Wave Flux 1	Yes	No	No	No	No
2	BBB1,2	Paste 3	Mask 1	No	Repair Wire 2	Wave Flux 2	No	No	No	No	No
2	CCC1,2	Paste 3	Mask 1	No	Repair Wire 2	Wave Flux 2	No	Repair Flux 1	Repair Wire 2	No	No
2	DDD1,2	Paste 3	Mask 1	No	Repair Wire 2	No	No	Repair Flux 2	No	Yes	No
2	EEE1,2	Paste 3	Mask 1	No	Repair Wire 2	Wave Flux 3	No	No	No	No	No
2	FFF1,2	Paste 3	Mask 1	No	Repair Wire 2	Wave Flux 3	No	Repair Flux 1	Repair Wire 2	No	No
2	GGG1,2	Paste 3	Mask 1	No	Repair Wire 2	Wave Flux 4	No	No	No	No	No
2	HHH1,2	Paste 3	Mask 1	No	Repair Wire 2	Wave Flux 4	No	Repair Flux 1	Repair Wire 2	No	No
2	III1,2	Paste 3	Mask 1	No	Repair Wire 3	No	No	No	No	No	No
2	JJJ1,2	Paste 3	Mask 1	No	Repair Wire 3	Wave Flux 1	Yes	No	No	No	No
2	KKK1,2	Paste 3	Mask 1	No	Repair Wire 3	Wave Flux 2	No	No	No	No	No
2	LLL1,2	Paste 3	Mask 1	No	Repair Wire 3	Wave Flux 2	No	Repair Flux 1	Repair Wire 3	No	No
2	MMM1,2	Paste 3	Mask 1	No	Repair Wire 3	No	No	Repair Flux 2	No	Yes	No
2	NNN1,2	Paste 3	Mask 1	No	Repair Wire 3	Wave Flux 3	No	No	No	No	No
2	OOO1,2	Paste 3	Mask 1	No	Repair Wire 3	Wave Flux 3	No	Repair Flux 1	Repair Wire 3	No	No
Quantity	**#**	**Solder paste**	**Solder mask**	**Adhesive**	**Repair wire**	**Wave flux**	**Wash**	**Repair flux**	**Repair wire**	**Wash**	**Encap.**
2	PPP1,2	Paste 3	Mask 1	No	Repair Wire 3	Wave Flux 4	No	No	No	No	No
2	QQQ1,2	Paste 3	Mask 1	No	Repair Wire 3	Wave Flux 4	No	Repair Flux 1	Repair Wire 3	No	No
2	RRR1,2	No	Mask 1	Adhesive 1	No	No	No	No	No	No	No
2	SSS1,2	No	Mask 1	No	Repair Wire 1	No	No	No	No	No	Encap
2	TTT1,2	No	Mask 1	No	Repair Wire 2	No	No	No	No	No	Encap
2	UUU1,2	Paste 1	Mask 1	Adhesive 1	Repair Wire 1	No	No	No	No	No	No
2	VVV1,2	Paste 1	Mask 1	Adhesive 1	Repair Wire 2	No	No	No	No	No	No
2	WWW1,2	Paste 1	Mask 1	Adhesive 2	Repair Wire 1	No	No	No	No	No	No
2	XXX1,2	Paste 1	Mask 1	Adhesive 2	Repair Wire 2	No	No	No	No	No	No
Total 90											
These 90 boards to be tested on IPC (regular measurements)											