

Influence of Nanoparticles, Low Melting Point (LMP) Fillers, and Conducting Polymers on Electrical, Mechanical, and Reliability Performance of Micro-Filled Conducting Adhesives for Z-Axis Interconnections

Rabindra N. Das, Konstantinos I. Papathomas, John M. Lauffer and Frank D. Egitto
Endicott Interconnect Technologies, Inc., 1701 North Street, Endicott, New York, USA 13760
Telephone No: 607-755-1389
E-mail: rabindra.das@eitny.com

Abstract

This paper discusses micro-filled epoxy-based conducting adhesives modified with nanoparticles, conducting polymers, and low melting point (LMP) fillers for z-axis interconnections, especially as they relate to package level fabrication, integration, and reliability. A variety of conducting adhesives with particle sizes ranging from 80 nm to 15 μm were incorporated as interconnects in printed wiring board (PWB) or laminated chip carrier (LCC) substrates. SEM and optical microscopy were used to investigate the micro-structure, and conducting and sintering mechanisms. Volume resistivity of modified adhesives is in the range of 10^5 to 10^6 ohm-cm. Adhesives formulated with a conducting polymer exhibited tensile strength with Gould's JTC-treated Cu \geq 3800 PSI, and as low as 1800 PSI for a conducting polymer- LMP based system. There was no delamination of conductive joints after 3X IR-reflow, pressure cooker test (PCT), and solder shock. Among all, the conducting polymer modified micro-filled adhesives showed the highest mechanical strength. The paper also describes a combinatorial approach to the synthesis of LMP coated particles. Several conductive adhesives were used in a z-axis interconnect construction for a laminate chip carrier and printed wiring board (PWB). The present process allows fabrication of z-interconnect conductive joints having diameters in the range of 55-300 microns. The processes and materials used to achieve smaller feature dimensions, satisfy stringent registration requirements, and achieve robust electrical interconnections are discussed.

1. Introduction

The demand for high-performance, lightweight, portable computing power is driving the industry toward miniaturization at a rate not seen before. Electronic packaging is evolving to meet the demands of higher functionality in ever smaller packages. The high end of the semiconductor marketplace appears to be standard Application-Specific Integrated Circuits (ASICs), structured ASICs, and Field-Programmable Gate Arrays (FPGAs). These devices continue to use increasing numbers of signal, power, and ground die pads, and a corresponding decrease in pad pitch is required to maintain reasonable die sizes.

Traditionally, greater wiring densities in electronic packages are achieved by reducing the dimensions of vias, lines, and spaces, increasing the number of wiring layers, and utilizing blind and buried vias. However, each of these approaches possess inherent limitations, for example those related to drilling and plating of high aspect ratio vias, reduced conductance of narrow circuit lines, and increased cost of fabrication related to additional wiring layers. As a

result, the microelectronics industry is moving toward alternative, innovative approaches as solutions for squeezing more function into smaller packages. Assembly and packaging are bridging the gap by enabling economic use of the third dimension (3D packaging). System level integration is emerging. These approaches include System-in-Package (SiP), stacked die, or package stacking solutions. In addition to the trend toward miniaturization, new materials and structures are required to keep pace with more demanding packaging performance requirements. High speed packages, for example, server and telecom applications, require low loss materials, better shielding, elimination of via stubs, and optical interconnection, both chip-to-chip and between packaging components.

It is therefore imperative to make the most efficient use of real estate used for wiring and drive the number of wiring layers to a minimum. Packaging designs that are most effective in optimizing the use of available wiring space incorporate blind and buried vias. For interconnection with traditional plated through hole (PTH) technology, two PTHs are required to complete a circuit trace. PTHs consume real estate by blocking channels that could be used for wiring (**Figure 1**). As via diameters decrease to accommodate more dense designs, plating of the vias becomes more of a challenge. This problem is alleviated to a degree by use of thinner, laser-friendly dielectric materials. Although the use of blind vias frees up wiring space, its utility is limited by the challenge of plating blind vias with aspect ratios (depth to diameter) greater than 1:1. Therefore, a means of fabricating a vertical interconnection that can be terminated at any wiring plane, at any depth, within the package is highly desirable. One method of extending wiring density beyond the limits imposed by these approaches is a strategy that allows for metal-to-metal z-axis interconnection of subcomposites during lamination to form a composite structure [1].

Conductive joints can be formed during lamination using an electrically conductive adhesive. As a result, one is able to fabricate structures with vertically-terminated vias of arbitrary depth. Replacement of conventional plated through holes with vertically-terminated vias opens up additional wiring channels on layers above and below the terminated vias and eliminates via stubs which cause reflective signal loss. Vertically terminated vias facilitate a more space-efficient package redesign for chips having a tighter pad pitch. In addition, parallel lamination of testable subcomposites offers yield improvement, shorter cycle times, and ease of incorporating features conducive to high speed data rates.

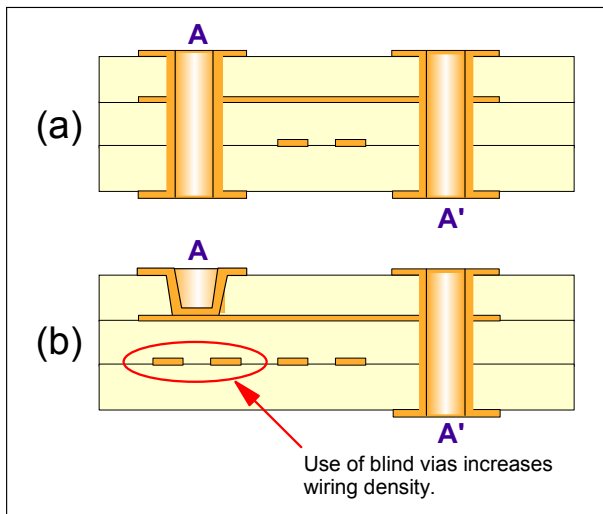


Figure 1: The use of blind vias increases wiring density in circuit layers below the via.

During the past few years, there has been increasing interest in using electrically conductive adhesives as interconnecting materials in the electronics industry [2]. Conductive adhesives are composites of polymer resin and conductive fillers. Metal-to-metal bonding between conductive fillers provides electrical conductivity [3-6], whereas a polymer resin provides better processability and mechanical robustness [7]. Excess filler loading to enhance conductivity tends to weaken the overall mechanical strength of a conductive adhesive. Therefore, reliability of the conductive joint formed between the conductive adhesive and the metal surface to which it is mated is of prime importance. Conductive adhesives can have broad particle size distributions. Larger particles can be a problem when filling smaller holes (e.g., diameter of 60 μm or less), resulting in voids. Several nano and micro-filled adhesives have been reported for advanced packaging applications. For example, Xiao et al [8] describes epoxy or silicone based conductive adhesive joints and their thermal and mechanical stabilities. Jeong et al [9] reported the effects of curing behavior, solvent evaporation, and shrinkage on conductivity of adhesives. They [10] also described conductivity of micro-filled adhesives upon addition of nanoparticles. Lee [11] reported the effect of nano-sized silver particles on the resistivity of micro-sized silver flakes, in mixed-sized silver particle-filled conductive adhesives. Goh et al [12] mentioned the effect of annealing on the morphologies and conductivities of sub-micrometer sized nickel particles used for electrically conductive adhesive. Inoue et al [13] investigated the variations in electrical properties caused by differences in the curing conditions of a typical isotropic conductive adhesive (ICA) made with an epoxy-based binder. Coughlan et al [14] described electrical and mechanical analysis of conductive adhesives where the main properties of joint resistance and adhesive strength were examined before and after different environmental treatments. Fu [15] describes cluster effects of nano fillers in conductive adhesives. Sancakter et al. [16] reported pressure-dependent conduction behavior with particles of different sizes, shapes, and types. The effects of

external pressure on the filler resistance were measured. Jiang et al [17] reported surface functionalized nano silver-filled conductive adhesives. Li [18] reported that self-assembled monolayers (SAMs) protected silver nano-particle-based conductive adhesives. These studies have described material properties and reliability assessment at a macroscopic level, but have not described fabrication, integration, and reliability issues. Although several composites have been available, the authors believe that there is potential for improvement of the existing materials, so that flexible and reliable material that can be processed at low temperatures can be developed for z-axis interconnections.

The first objective of this study is to investigate the effect of nanoparticle addition to microcomposites. Nanoparticles of silver were chosen because of their higher electrical conductivity and chemical stability. Nanoparticles were mixed with microparticles to improve the sintering behavior of the adhesives. A second objective is to use a conducting polymer and low melting point (LMP) fillers. Addition of a conducting polymer will increase the overall mechanical strength without compromising electrical conductivity. LMP and LMP-coated particles melt during processing and produce a continuous metallic network. A variety of metals including Cu, Ag, LMP and LMP-coated Cu have been used to make the conductive adhesives. The adhesive was applied onto Cu substrates by printing or coating. This work also deals with adhesion issues between the adhesives and the substrates to which they are mated. The paper presents a reliability assessment of adhesive joints conducted by testing samples exposed to pressure cooker tests (PCT), IR-reflow, and solder shock. The work was extended to the development of a z-axis interconnect construction for a laminate chip carrier and printed wiring board (PWB). The structure employs an electrically conductive medium to interconnect thin cores (subcomposites). The cores are processed in parallel, aligned, and laminated to form a composite. The net effect is a composite laminate having vertical interconnections with small diameter holes that can terminate arbitrarily at any layer within the cross section of the package. There is no requirement for PTHs to be formed at the composite level. Some of the technical challenges associated with this z-interconnect technology are addressed. This effort is an integrated approach centering on three interrelated fronts: (1) materials development and characterization; (2) fabrication, and (3) reliability of the electronic package.

2. Experimental Procedure

A variety of silver, copper, and low melting point (LMP)-based nano and micro particles and their dispersion into epoxy resin were investigated in order to achieve uniform mixing in the adhesive. In a typical procedure, epoxy-based conductive adhesives were prepared by mixing appropriate amounts of the conducting filler powders and epoxy resin in an organic solvent to form a paste like composition. For conductivity measurements, a thin film of this paste was deposited on a non conducting substrate and cured at different temperatures ranging from 150 $^{\circ}\text{C}$ to 265 $^{\circ}\text{C}$. For reliability assessments, two paste films were laminated together.

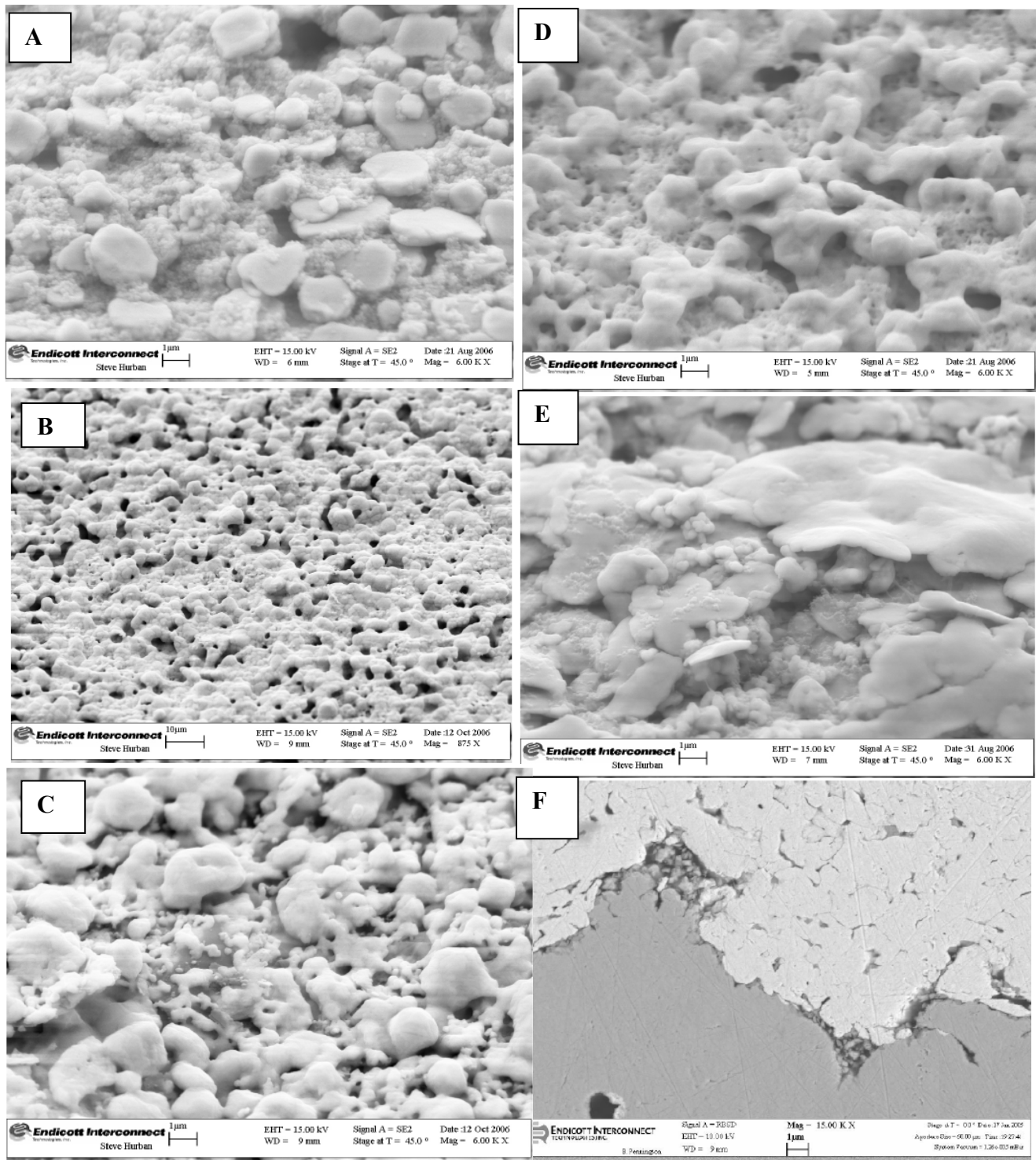


Figure 2: SEM micrographs for the nano-micro filled silver based conducting adhesives; (A) un-sintered at 200 °C, (B)-(D) sintered at (275 ±10) °C, (E) un-sintered at 300 °C, and (F) sintered at 365 °C.

In the fabrication of a high-density laminate chip carrier, a joining core consisting of a single metal reference plane and no circuit traces for signal transmission (0S/1P) was constructed using a copper power plane, 35 μm thick, sandwiched between layers of a dielectric material composed of silica-filled allylated polyphenylene ether (APPE) polymer. Through holes in the joining cores, formed by laser drilling, and having diameters ranging from 50 to 75 μm , were filled with an optimized electrically conductive adhesive. The adhesive-filled joining cores were cured and cross sectioned to evaluate hole fill quality.

Adhesives were characterized by Scanning Electron Microscopy (SEM) and optical microscopy to ascertain particle dispersion and interconnection mechanism. A Keithley micro-ohmmeter was used for electrical measurements. Tensile strength of simulated interconnects was measured using a MTS tensile tester.

3. Results and Discussion

It is well known that change in grain size has a direct impact on the electronic properties of a system. In view of this, a systematic investigation of electrical resistance behavior of silver nanocomposites has been carried out, and the results of such an investigation are presented here. **Figure 2** shows SEM images of the specimens collected from nanocomposites with different sintering temperature, from lower temperature (**Figure 2A**) to higher (**Figure 2F**). As can be seen, the main components are a mixture of nanoparticles and microparticles. The nanoparticles may contact with the adjacent ones, but the nano aggregation lengths are short, less than 10-fold of the microparticle diameter on average (**Figure 2A**). As the sintering temperature increases, particle diffusion becomes more and more obvious. The aggregation length becomes much longer, resulting in the formation of one-dimensional jointed particle assemblies developing into a smooth continuous network (**Figures 2B-D**). Conductivity measurements show that the resistance drops 30-50% from 200C to 265C. In contrast, the nanocomposites synthesized with a nano-micro mixture show a much different morphology as can be seen in **Figures 2E-F**. The nanoparticles are less (low concentration). They are not following the same sintering mechanism as observed for the nanocomposite shown in **Figures 2B-D**. Instead, most of the particles maintain their identity, as if they didn't sinter with temperature. **Figure 2** shows nanocomposites sintered at lower temperature and higher temperature. The observation suggests that the sintering mechanisms are different for the nanocomposites synthesized in the two different mixtures. Based upon the morphologies observed above, we suggest a sintering mechanism for the nanocomposites at low temperature as follows.

In the high-concentration region, nanoparticles are highly reactive due to immediate particle to particle contact. Moreover, the diffusion (sintering) of nanoparticles should be lower than that of the corresponding bulk solid. With the increase of size, the particles need higher temperature for diffusion to make a uniform metallic network. However, in the low-concentration region, the polymer plays an important role. In this region, the amount of polymer is sufficient to prevent metallic diffusion/sintering.

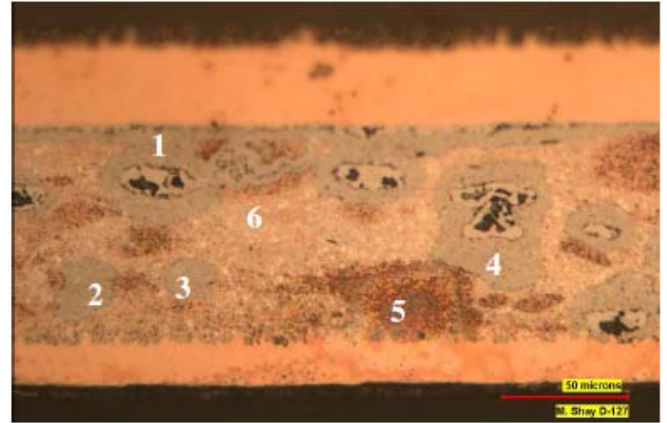


Figure 3: Micrographs for the cross-sectional view of adhesives containing low melting point (LMP) fillers, silver and Cu particles.

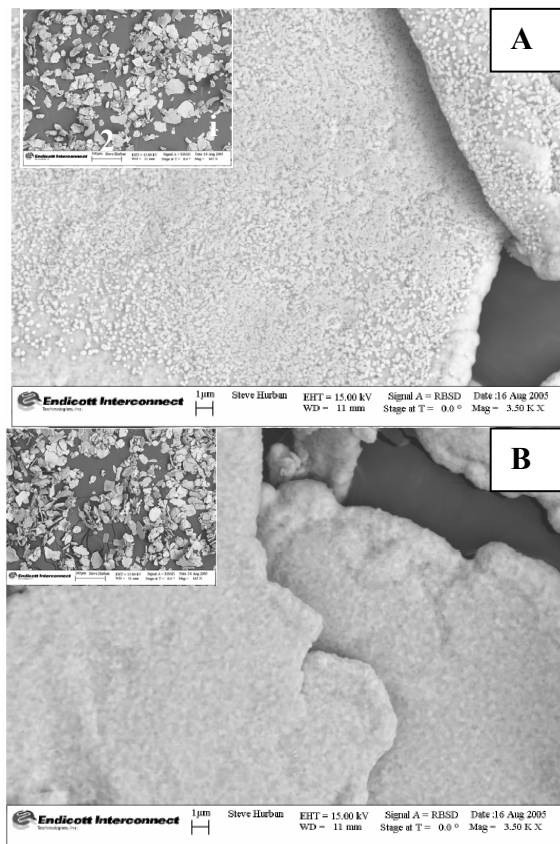


Figure 4 : LMP coated particles (A) partially LMP coated particles obtained from incomplete reaction and (B) complete reactions results fully LMP coated particles.

A combinatorial approach was applied to fabricate LMP-based, highly conductive adhesives. A library of different composition gradients was generated in conducting adhesives using various materials such as Ag, Cu, LMP etc. The intent in this investigation is to obtain a composition gradient in order to optimize a set of desired localized properties. **Figure 3** shows an optical photograph of conductive adhesives with variable composition zones. Zones 1, 2, 3, and 4 have excess

LMP that could melt and cause X-Y shorts during curing processes used in the fabrication of electronic circuitry. On the other hand, Zone 5 has excess metal. In a typical LMP system, the LMP metal melts and reduces interparticle resistance among the metallic particles. Less LMP was not sufficient to cover all the metal particles. Zone 6 (center part) shows minimum LMP content, but spread uniformly throughout the metallic network. This would probably be the best LMP-based conductive adhesive for z-axis interactions. Based on this experimental evidence, nano LMP-coated (~100 nm) particles were designed and synthesized. **Figure 4B** shows SEM micrographs of nano LMP-coated particles. **Figure 4A** shows particles with an incomplete reaction. Incomplete reaction results in partially coated particles.

Conducting polymers such as polyaniline are generally doped with protonic acids such as aqueous hydrochloric acid (HCl) to give a conductivity on the order of 1 S/cm². Polyanilines are generally soluble [19-21], environmentally stable polymers that are fabricated by a one-step synthesis involving inexpensive raw materials [22]. Other conducting polymers typically used in organic electronics are poly-3,4-ethylenedioxythiophene doped with polystyrene sulfonic acid PEDOT/PSS, dodecyl benzene sulfonic acid doped polyaniline ~DBSA-PANI and camphor sulfonic acid doped polyaniline, DNNSA-PANI, a polyaniline doped with dinonyl naphthalene sulfonic acid ~DNNSA. A variety of conducting polymers, blended with appropriate polymers and cured at ~190°C for 2 hours, showed low volume resistivity, in the range of 10⁵ ohm-cm, which is similar to that of micro-filled adhesives. Volume resistivity decreases with increasing curing temperature due to sintering of metal particles. Adhesion between the adhesive and the substrate to which it is mated is critical to the reliability of the semiconductor package. Bond strength of conducting-polymer-modified adhesive joints was evaluated using tensile strength measurements. Tensile strength was measured using an MTS tensile testing machine at a pulling rate of 0.025 inch per minute, and measuring until the joint ruptured. Micro-filled adhesives show high tensile strength with Gould JTC-type Cu foils and show cohesive failure. Conducting polymer doped samples did not show any failure. Here, adhesive (glue) used to attach laminates to test fixtures ruptured prior to the test structures. This indicates conducting polymer modified samples result in highly conducting adhesives having good mechanical strength. Conducting-polymer-based LMP samples showed high mechanical strength. Typically, LMP-based samples show mechanical strength in the range of 600 PSI. Addition of conducting polymer enhances the mechanical strength to 1800-2000 PSI. **Table 1** summarizes the tensile strength measurements of conductive adhesives. Conducting polymer silver-filled paste yielded the maximum mechanical strength. There is a significant resistivity drop with increasing curing temperature from 150 °C to 190 °C. **Figure 5** shows volume resistivity of silver adhesive with aging at room temperature as a function of curing temperature. Resistivity of conducting-polymer-based adhesives after 72 hours aging and cured at 190°C was not changed significantly. All conducting-polymer-based adhesives show less than 5% resistance change, even cured after 100 hours of aging at room temperature.

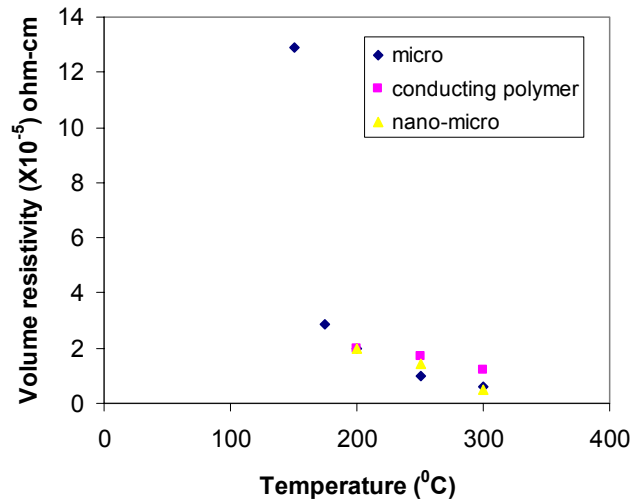


Figure 5: Volume resistivity of silver adhesive as a function of curing temperatures

Table 1. Tensile strength and modes of failure

Adhesive	Tensile Strength (PSI)	Failure Mode
Low melting point (LMP) Alloy	600	Cohesive
Conducting polymer + LMP	1800-2000	Cohesive
Conducting polymer	>3800	No adhesive fail (glue ruptured)
Silver (Ag)	3370	Cohesive

Core Fabrication

A few optimized metal-epoxy adhesives were used for hole fill applications to fabricate z-axis interconnections in laminates. Conductive joints were formed during composite lamination using an electrically conductive adhesive. Z-axis interconnection was achieved using joining cores. Through holes in the joining cores, formed by laser or mechanical drilling and having diameters ranging from 50 μm to about 300 μm, were filled with an optimized electrically conductive adhesive. The adhesive-filled joining cores were laminated with circuitized subcomposites to produce a composite structure. High temperature/pressure lamination was used to cure the adhesive in the composite and provide Z-interconnection between the circuitized subcomposites. A variety of joining core structures such as 0S/1P, 0S/2P, etc. were used for hole fill applications. The cores can be structured to contain a variety of arrangements of signal, voltage, and ground planes. In addition, signal, voltage, and ground features can reside on the same plane.

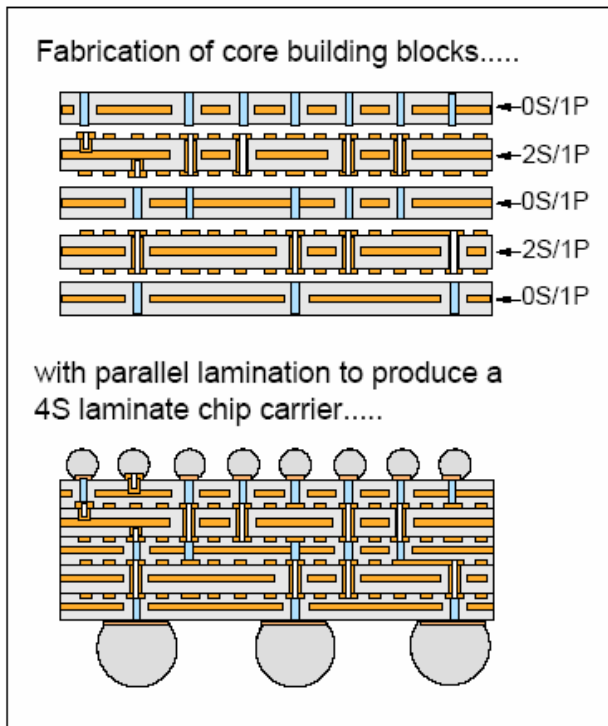


Figure 6: Parallel lamination of subcomposites (cores) to form laminate chip carrier having four signal wiring planes with a stripline transmission line structure.

By alternating 2S/1P and 0S/1P cores in the lay-up prior to lamination, the conductive paste electrically connects copper pads on the 2S/1P cores that reside on either side of the 0S/1P core. Two signal layers are added to the composite structure each time one adds an additional 2S/1P core and an additional 0S/1P core. A structure with four signal layers composed of five subcomposites (two 2S/1P cores and three 0S/1P cores) is shown schematically in **Figure 6**. Although this particular construction comprises alternating 2S/1P and 0S/1P cores, it is possible to place multiple 0S/1P cores adjacent to each other in the stack.

Figures 7A, 7B and **7C** show SEM micrographs and optical photographs of a joining core having paste-filled holes with a diameter of 75, 55 and 300 μm respectively. A photograph of a composite laminate structure is shown in cross section in **Figure 8**. Proper preparation of the subcomposites is crucial to obtaining robust, reliable joining between dielectric layers and between the conductive paste and the opposing copper pad. Sufficient flow of the dielectric materials must be achieved during lamination to allow for complete encapsulation of circuitized features and achieve good dielectric-to-dielectric bonding. Package level and sub-composite level reliability of conductive joints in the test vehicle were further examined by IR-reflow (3X, 225°C), PCT and solder shock. No intrinsic failure mechanisms were observed. There was no cracking or delamination at the paste joints. Conductive joints are stable even after multiple IR-reflow (3X), and PCT followed by a 15 second solder dip.

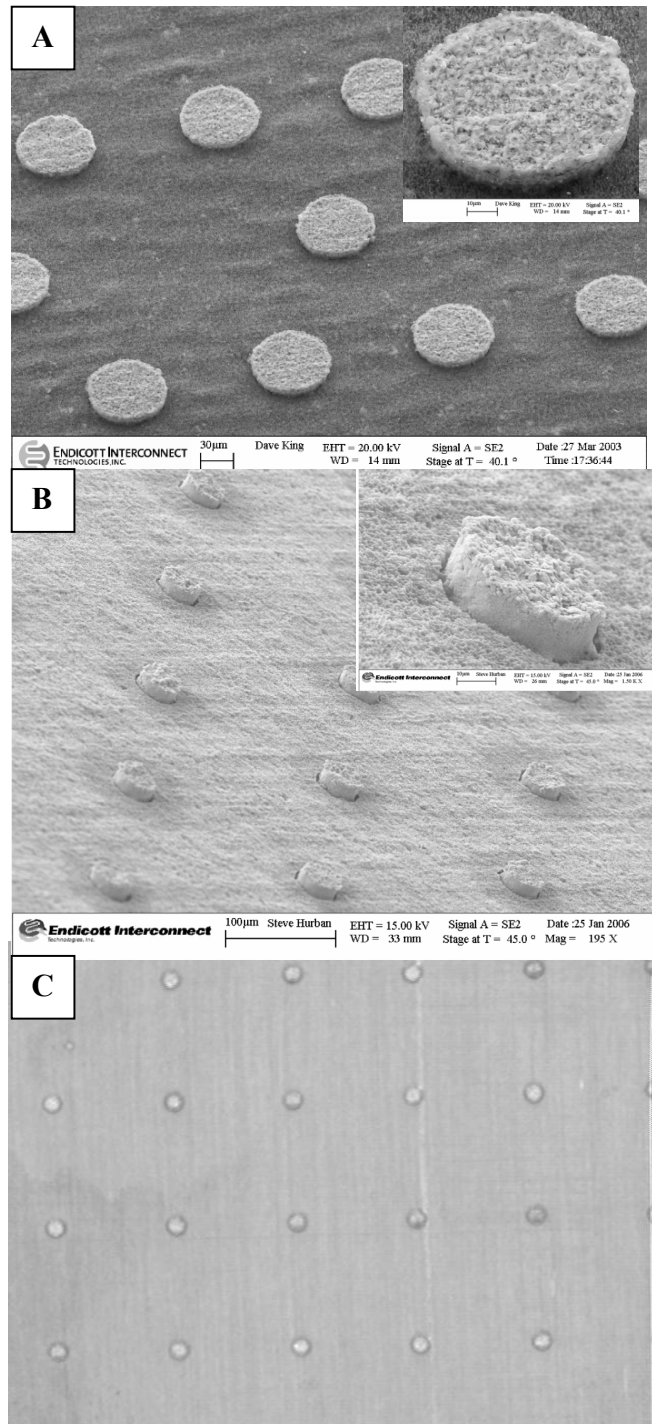


Figure 7: SEM micrographs of adhesive-filled joining core; (A) 75 micron hole diameter, (B) 55 micron hole diameter, and (C) 300 micron hole diameter.

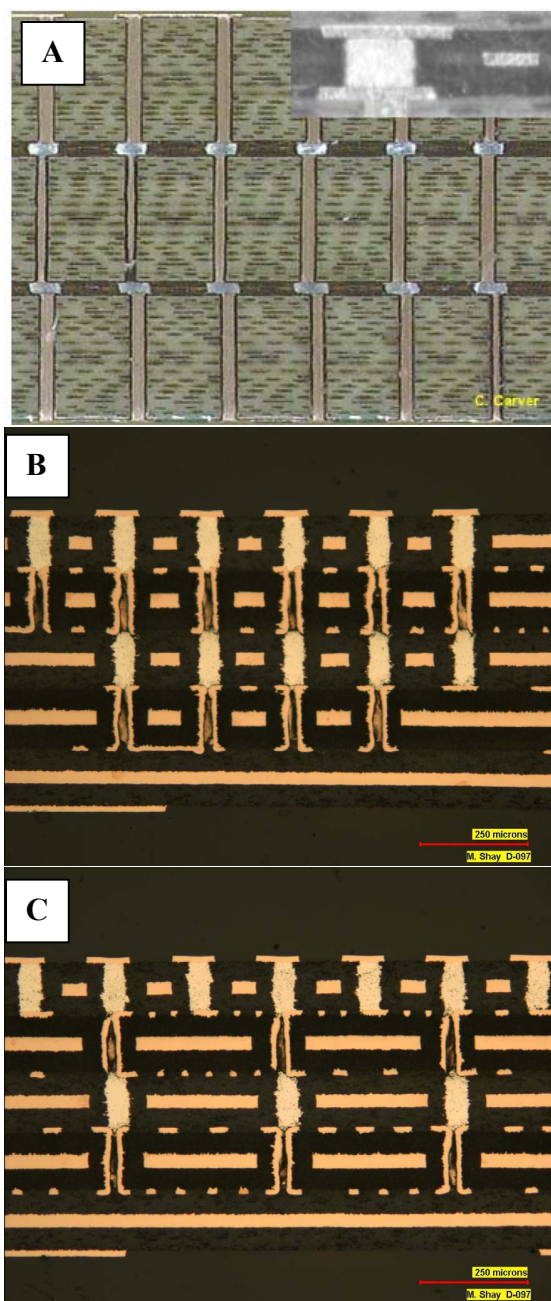


Figure 8: Photograph of z-interconnect laminates shown in cross section: (A) board with vias having 300 microns diameter and (B) chip carriers with vias having 55 micron diameter, and (C) chip carriers with vias having 55 micron diameter after IR-reflow (3X), and PCT followed by a 15 second solder dip.

Conclusions

A variety of micro-filled conducting adhesives modified with nano particles, conducting polymer, and LMP were used for a z-axis interconnection applications. High aspect ratio, small diameter holes anywhere in the range of 55 to 75 microns were successfully filled. Addition of nanoparticles reduces sintering temperatures of micro-filled conducting adhesives. Conducting-polymer-based adhesives were mechanically better than micro- and LMP-filled adhesives.

All adhesives maintained high electrical conductivity and tensile strengths. A combinatorial approach was used to optimize LMP-based systems. LMP-coated particles were synthesized and used as an alternate approach for conducting adhesives. Conductive joints were stable after 3x IR-reflow, pressure cooker test (PCT), and solder shock. The adhesive-filled joining cores were laminated with circuitized subcomposites to produce a composite structure. High temperature/pressure lamination was used to cure the adhesive in the composite and provide stable, reliable z-interconnections among the circuitized subcomposites

Acknowledgments

The authors acknowledge the valuable contributions of V. Markovich, K. Blackwell, S. Hurban, M. Shay, G. Kohut, and D. Thorne.

References

1. F.D. Egitto, S.R. Krasniak, K.J. Blackwell, and S.G. Rosser, "Z-Axis Interconnection for Enhanced Wiring in Organic Laminate Electronic Packages," Proceedings Fifty-Fifth Electronic Components and Technology Conference, May 31 to June 3, 2005, Lake Buena Vista, FL (IEEE, Piscataway, NJ, USA), p. 1132.]
2. Liu, J., 1999, *Conductive Adhesives for Electronics Packaging*, (British Isles: Electrochemical Publications Ltd, 1999), pp. 317-320.
3. Ye, L., Lai, Z., Liu, J., and Tholen, A., 1999, "Effect of Ag Particle Size on Electrical Conductivity of Isotropically Conductive Adhesives," *IEEE Trans. Electron. Packag., Manuf.*, Vol. 22,(1999), pp. 299–302.
4. Yasuda, K., Kim, J. M., Rito, M., and Fujimoto, K., "Joining Mechanism and Joint Property by Polymer Adhesive with Low Melting Alloy Filler," *Int. Conf. on Electron. Packag.*, (2003),pp. 149–154.
5. Yasuda, K., Kim, J. M., Yasuda, M., and Fujimoto, K., "New Process of Self-Organized Interconnection in Packaging by Conductive Adhesive with Low Melting Point Filler," *Int. Conf. on Solid State Devices and Materials*,(2003), pp. 390–391.
6. Yasuda, K., Kim, J. M., and Fujimoto, K., "Adhesive Joining Process and Joint Property with Low Melting Point Filler," *3rd Int. IEEE Conf. on Polymer and Adhesives in Microelec. and Photon.*, (2003), pp. 5–10.
7. Yao, Q., and Qu, J., 2002, "Interfacial versus Cohesive Failure on Polymer- Metal Interfaces in Electronic Packaging—Effects of Interface Roughness," *ASME J. Electron. Packag.*, Vol.124 (2002), pp. 127–134.
8. Xiao J, Chung DDL, "Thermal and mechanical stability of electrically conductive adhesive joints" *J. Electronic Mater.* 34 (5): 625-629 MAY 2005
9. Jeong WJ, Nishikawa H, Gotoh H, Takemoto T , "Effect of solvent evaporation and shrink on conductivity of conductive adhesive" *Mater. Trans.* 46 (3): 704-708 MAR 2005
10. Jeong WJ, Nishikawa H, Ito D, Takemoto T , "Electrical characteristics of a new class of conductive adhesive" *Mater. Trans.* 46 (10): 2276-2281 OCT 2005
11. Lee HH, Chou KS, Shih ZW, "Effect of nano-sized silver particles on the resistivity of polymeric conductive

- adhesives" *International J. Adhesion & Adhesives* 25 (5): 437-441 OCT 2005
12. Goh CF, Yu H, Yong SS, Mhaisalkar SG, Boey FY, Teo PS, "The effect of annealing on the morphologies and conductivities of sub-micrometer sized nickel particles used for electrically conductive adhesive" *Thin Solid Films* 504 (1-2): 416-420 MAY 10 2006
 13. Inoue M, Sukanuma K, "Effect of curing conditions on the electrical properties of isotropic conductive adhesives composed of an epoxy-based binder" *Soldering & Surface Mount Technology* 18 (2): 40-45 2006
 14. Coughlan FM, Lewis HJ, "A study of electrically conductive adhesives as a manufacturing solder alternative" *J. Electronic Mater.* 35 (5): 912-921 MAY 2006
 15. Fu Y, Willander M, Liu J, "Spatial distribution of metal fillers in isotropically conductive adhesives" *J. Electronic Mater.* 30 (7): 866-871 JUL 2001
 16. Sancaktar E, Dilsiz N, "Pressure-dependent conduction behavior of various particles for conductive adhesive applications" *J. Adhesion Science and Technology* 13 (6): 679-693 1999
 17. Jiang HJ, Moon KS, Lu JX, Wong CP, "Conductivity enhancement of nano silver-filled conductive adhesives by particle surface functionalization" *J. Electronic Mater.* 34 (11): 1432-1439 NOV 2005
 18. Li Y, Moon KS, Wong CP, "Monolayer-protected silver nano-particle-based anisotropic conductive adhesives: Enhancement of electrical and thermal properties" *J. Electronic Mater.* 34 (12): 1573-1578 DEC 2005
 19. M. Angelopoulos, A. Ray, A. G. MacDiarmid, and A. J. Epstein, *Synth. Met.* **21**, 21 (1987).
 20. M. Angelopoulos, G. E. Asturias, S. P. Ermer, A. Ray, E. M Scherr, and A. G. MacDiarmid, *Mol. Cryst. Liq. Cryst.* **160**, 151 (1988).
 21. K. T. Tzou and R. V. Gregory, *Synth. Met.* **69**, 109 (1995).
 22. A. G. MacDiarmid, J. C. Chiang, A. F. Richter, N. L. D. Somasiri, and A. J. Epstein, in *Conducting Polymers*, L. Alcaer, Ed., Reidel, Dordrecht, 1985, pp. 105-120.