

## Effects of Package Warpage on Head-in-Pillow Defect

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Head-in-pillow (HiP) is a BGA defect which happens when solder balls and paste can't contact well during reflow soldering. Package warpage was one of the major reasons for HiP formation. In this paper, package warpage was measured and simulated. It was found that the package warpage was sensitive to the thickness of inside chips. A FEM method considering viscoelastic property of mold compound was introduced to simulate package warpage. The CTE mismatch was found contributes to more than 90% of the package warpage value when reflowing at the peak temperature. A method was introduced to measure the warpage threshold, which is the smallest warpage value that may lead to HiP. The results in different atmospheres showed that the warpage threshold was 50  $\mu\text{m}$  larger in  $\text{N}_2$  than that in air, suggesting that under  $\text{N}_2$  atmosphere the process window for HiP defects was larger than that under air, which agreed with the experiments.

[doi:10.2320/matertrans.MI201404]

(Received January 14, 2015; Accepted April 6, 2015; Published May 29, 2015)

**Keywords:** head-in-pillow, ball grid array package, warpage

### 1. Introduction

Down to the road of speed, complexity, and miniaturization, ball grid array (BGA) design has been introduced into electronic industry due to its higher I/O density. However, the disadvantages of BGA, such as possibility of low joint reliability and difficulty of inspection, may lead to defects influencing the performance of components.<sup>1,2)</sup> HiP (head-in-pillow) is one of such defects. For a normal joint, the solder ball sitting on solder paste forms a metallurgic joint after reflow process. But for an HiP joint, though mechanical and electric contact can be established, there is neither metallurgic bond nor an appropriate joint shape.<sup>1-6)</sup> And when HiP occurs during Surface Mount Technology (SMT) process, it is hard to detect this defect using standard nondestructive testing methods since electrical connection may still work, and failures always happen at customer side after a short-term usage.<sup>7)</sup>

Thus, it is essential to understand the HiP formation mechanism, and find out effective control factors to reduce the risks of HiP formation.<sup>8)</sup> Among the factors may lead to HiP during reflow soldering, package warpage is a main cause of it.<sup>5,9,10)</sup> The packages warp is mainly induced by the CTE (coefficient of thermal expansion) mismatch between metallic and polymeric materials.<sup>11,12)</sup> Sidhu<sup>9)</sup> *et al.* measured the warpage of package at a reflow temperature  $\sim 240^\circ\text{C}$  with shadow moiré method and found the package area warping  $> 100 \mu\text{m}$  was at a high risk of HiP. Ken<sup>13)</sup> *et al.* suggested a full-field method to evaluate influence of component warpage: dual-surface warpage of components were measured and analyzed to help to predict defects such as HiP. Chiu<sup>14)</sup> *et al.* simulated warpage of packages with consideration of the constitutive relationship of an epoxy molding compound (EMC). And Kim<sup>15)</sup> *et al.* simulated PCB warpage

after patterning process by separately meshing all subparts and proposing a linear thermo elasticity analysis. However, it is noticed that few researches quantitatively investigated the influence of warpage on HiP. This paper mainly focused on package warpage effect on the formation of HiP. The simulation of package warpage and analysis of the warpage threshold were also introduced and the results allowed design engineers to predict HiP severity before actual fabrication.

### 2. Materials and Experimental Procedure

Sn-3.0Ag-0.5Cu solder paste used in experiment is produced by KOKI Inc. Figure 1(a) shows the double-sided PCB (printed circuit boards) used in the experiment. The PCB consists of 6 same units which were connected by

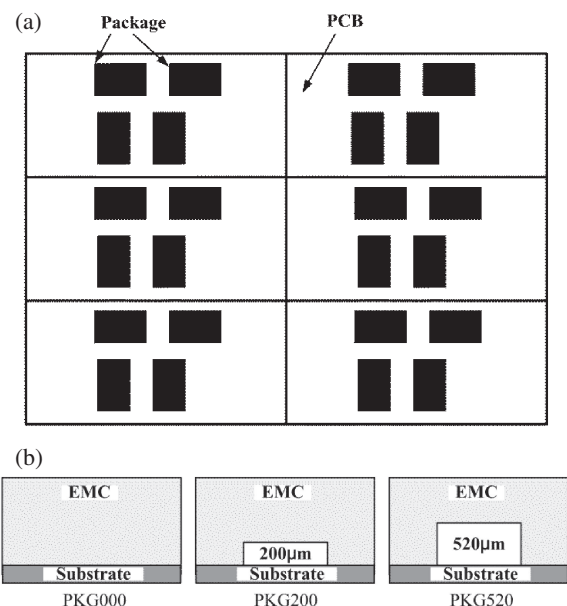


Fig. 1 Schematic diagram of (a) PCB and (b) package structures.

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Table 1 Dimension and material properties of package.

Material	Size (mm)	Thickness ( $\mu\text{m}$ )	Young modulus (GPa)	Poisson's ratio	CTE ( $10^{-6}/^{\circ}\text{C}$ )	Thermal conductivity ( $\text{W}/(\text{m}\cdot^{\circ}\text{C})$ )
Chip	12*8.4	40–45	170	0.3	3.0	98.4
EMC	—	—	17	0.3	$T_g = 125^{\circ}\text{C}$ $\frac{10(T < T_g)}{40(T > T_g)}$	0.6
Substrate	18*14	20	22	0.28	14	0.25
Package size	18*14	1400	—	—	—	—

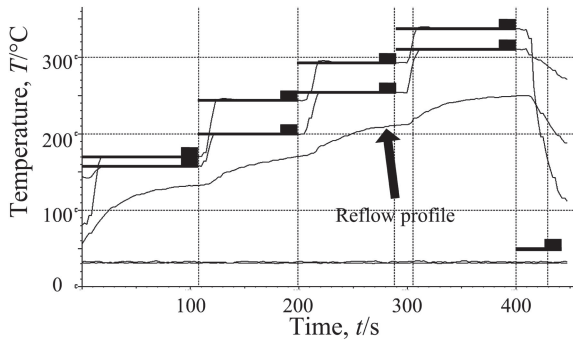


Fig. 2 Reflow profile.

break-away. There were 24 packages on each side of the PCB. The structures of dummy packages ( $18\text{ mm} \times 14\text{ mm} \times 1.4\text{ mm}$ ) are showed in Fig. 1(b). 3 kinds of packages were designed with different chip thickness inside and named by PKG000 (no chip inside), PKG200 ( $200\text{ }\mu\text{m}$  chip thickness) and PKG520 ( $520\text{ }\mu\text{m}$  chip thickness).

Generally, the reflow soldering technology includes 3 processes: print, mount assembly and reflow. To accelerate the experiment and get more defects, an aging process was applied between mount assembly and reflow process. The aging condition was heating samples at  $190^{\circ}\text{C}$  for 3~5 min to induce degradation of solder paste and aggravate oxidation of solder balls. Then the samples were sent into reflow oven and reflowed with the profile shows in Fig. 2. Dye and pry methods were introduced to evaluate the solder joint, especially the HiP propensity.

After reflow, the package warpage were measured with shadow moiré method. The package warpage is defined as follow: the + (smile) or - (cry) represents the shape of warpage<sup>16)</sup> and the value represents the magnitude of warpage.<sup>16)</sup> The BGA solder balls were removed before measurement to produce a flat surface. Shadow moiré measurements were conducted by placing a grating (low CTE glass with transparent and opaque stripes) parallel to the samples. A light beam in an angle of approximately  $45^{\circ}$  was projected through the grating and produces the stripe pattern on the sample.<sup>16)</sup> The moiré fringe pattern (geometric interference pattern) can be observed through the grating.<sup>16)</sup> Finally, the package warpage from planarity over the substrate surface can be provided by the analysis of the patterns.

Numerical simulation of package warpage was also carried out. The dimensions and material properties of 3 kinds of dummy packages used in this paper are listed in Table 1.

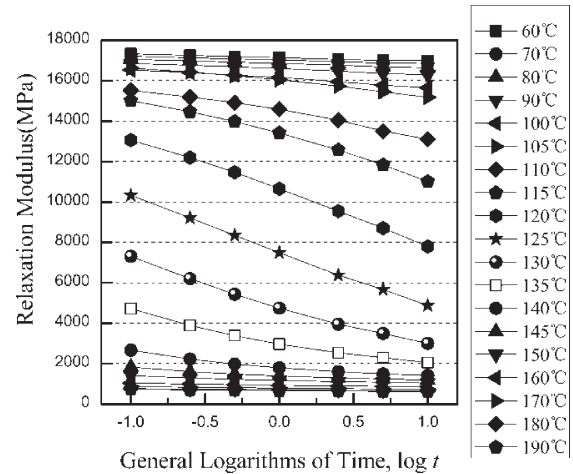


Fig. 3 Viscoelastic data of EMC.

Quarter finite element models for the dummy packages were built in ANSYS software to take advantages of symmetry.<sup>15,17)</sup> In the model, mechanical properties of materials except EMC were assumed to be linearly elastic. The viscoelastic property of EMC was introduced into the simulation and the EMC viscoelastic data measured with Dynamic Mechanical Analysis is revealed in Fig. 3.

It is noted that before reflowing, the as-received package normally had an initial package warpage, which is introduced by model compound reaction shrinkage and post-mold curing (PMC) after EMC injection in package production process.<sup>14,18–20)</sup> So this process before reflow should be also included in the simulation. It is common to assume that the model is stress free at  $175^{\circ}\text{C}$  before EMC injection.<sup>14)</sup> The total linear shrinkage of the EMC is 0.15%. The following PMC process consists of 4 stages: (1) cooling from molding temperature ( $175^{\circ}\text{C}$ ) to room temperature ( $25^{\circ}\text{C}$ ) in 30 min, (2) heating from  $25^{\circ}\text{C}$  to PMC temperature in 30 min, (3) curing at  $175^{\circ}\text{C}$  for 6 h, (4) cooling down to  $25^{\circ}\text{C}$  in 1 h. Details of the implementation of PMC simulation could refer to.<sup>14)</sup> Based on the simulation results (initial warpage) of package production process, the simulation of reflow was continued.

### 3. Results and Discussion

#### 3.1 Package warpage and its effects on HiP

Shadow moiré measured the warpages of different packages and the results are presented in Fig. 4. Each data point in figure represents an average of three samples. It is observed

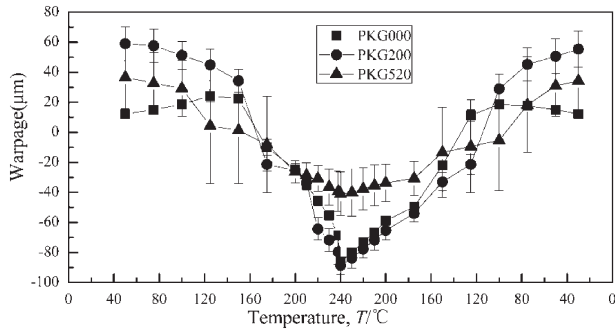


Fig. 4 Warpage of PKG000, PKG200 and PKG520 under different temperature.

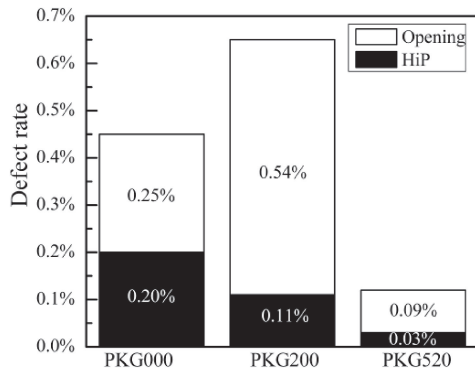


Fig. 5 Defect rate versus different package.

that at room temperature PKG200 has the largest initial package warpage of 60  $\mu\text{m}$  while PKG000 has the smallest of 11  $\mu\text{m}$ . As temperature increases, the warpage of all packages changed from concave (smile, +) to convex (cry, -) and peaked at the highest temperature. When the temperature cooled down, the package warpage fell back to the initial warpage level. The maximum warpage is the key factor for HiP occurrence because formation of HiP occurs during the melting of solder at high temperature. Results demonstrated that the PKG520 had the smallest max warpage around 40  $\mu\text{m}$  (at peak temperature) while PKG000 and PKG200 had a similar max warpage above 80  $\mu\text{m}$  (at peak temperature).

The dye and pry method showed that the HiP and opening were the major defects. The opening defect is a kind of defect where no mechanical contact of solder ball and paste is formed in a solder joint. Figure 5 shows the defects rate (including HiP and opening) of PKG000, PKG200 and PKG520 after the same reflow profile. The defect rate =  $N_d/N$ , where  $N_d$  means the amount of solder points with HiP or opening defect and  $N$  means the total amount of solder points ( $N = 10560$  in this paper). Apparently the defect rate = opening rate + HiP rate. According to the results, the HiP occurrence rate of PKG200 and PKG000 was 0.2% and 0.11%, respectively, whereas that of PKG520 was only 0.03%. It demonstrated that package with larger maximum warpage induced more HiP defects. That is because larger warpage separates the solder balls and paste and there is little contact at melting state. Furthermore, solder ball needs the flux of solder paste to remove the oxides on ball surface, but the separation reduces the amount of flux on solder ball and lowers the wettability of solder ball.

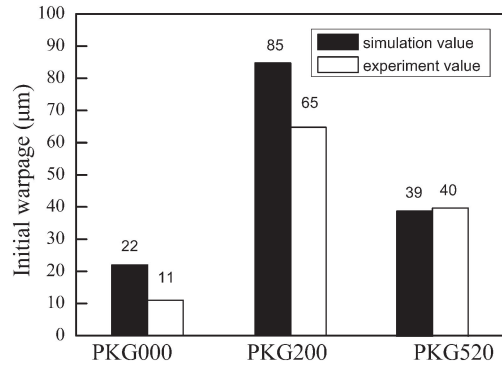


Fig. 6 Comparison of simulated and measured initial warpage value.

It is noticed that PKG200 had the largest warpage but its HiP defect rate was not the largest. It was because when the warpage was too large and opening defects was easier to occur compared with HiP. HiP and opening can be considered as two stages of defect both induced by package warpage. When the gap between solder ball and solder paste was small, a mechanical contact would occur when warpage decreased during cooling. However, when gap between them was too large, no mechanical contact occurred before the solidification of solder and the joint changed to an opening defect. Therefore, opening defect rather than HiP dominated in PKG200 which had the largest warpage.

### 3.2 Package warpage simulation

Numerical simulation was employed to help to analyze and predict the package warpages. As the initial package warpage was not zero, the package production process was taken into consideration in the numerical model. Both simulated and measured values consistently showed that PKG200 had the highest initial warpage, PKG000 had the lowest and PKG520 was in between (as shown in Fig. 6). The simulated and the measured initial warpages had a 10~20  $\mu\text{m}$  discrepancy. The discrepancy was mainly caused by two reasons: the simplifying of the actual package structure and homogeneity assumption of materials. Since the possible inclusion of minor inaccuracies or uncertain cannot overturn the trends and relative magnitudes of warpage,<sup>15)</sup> the simulation results were acceptable.

Based on the above results, warpages during reflow process were simulated. The simulated warpages were compared with experimental results, as shown in Fig. 7. The simulated warpage agrees well with shadow moiré experimental results. The discrepancy was within 10  $\mu\text{m}$  and statistically admissible considering the uncertainties presented in the simulation and experiment. It was noted that the simulated warpage reduced faster than the measured results in cooling process. This may be attributed to a faster profile cooling rate in finite element model compared with the experiment.<sup>21)</sup> However, it is noteworthy that the package warpage during its cooling down was not concerned in this paper since it has little influence on formation of HiP. The package warpage mainly resulted from CTE mismatch. Comparing with PKG000, PKG200 contained silicon chip in the package which enlarges CTE mismatch. Therefore, the warpage of PKG200 was larger than that of PKG000. In the

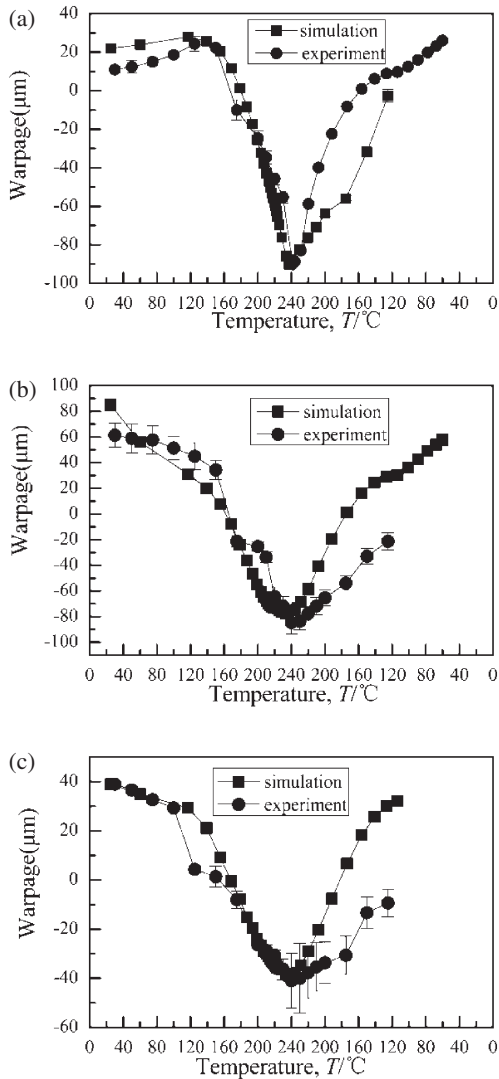


Fig. 7 Comparison of the simulation warpage and actual measured warpage of (a) PKG000, (b) PKG200, (c) PKG520.

other hand, thicker silicon chip was stiffer and difficult to warp, resulting in smallest warpage of the PKG520.

Besides predicting warpage, the simulation can be further used to analyze the cause of warpage. Both the CTE mismatch and the thermal gradient in the package can cause the warpage. It is difficult to separate the effects of CTE mismatch and thermal gradient in physical experiment, but in simulation it turns easy. The thermal gradients of PKG000, PKG200 and PKG520 at the peak temperature (~240°C) are less than 0.8°C/mm as shown in Fig. 8 and never exceeded this value during the whole reflow soldering process. To avoid the effect of thermal gradient, models of PKG000, PKG200 and PKG520 were built and simulated with every element set as the same peak temperature of 240°C. The warpage result is shown in Fig. 9. The warpage of PKG000 in Fig. 9(a) was -85 μm while that in Fig. 7(a) was -87 μm (at peak temperature), which means the effect of CTE mismatch contributed to 97.7% warpage and the effect of thermal gradient offered 2.3% warpage. But for PKG200 and PKG520, the warpages were -95 μm (108% of warpage in Fig. 7(b)) and -45 μm (110% of warpage in Fig. 7(c)), respectively. The silicon chip inside had a lower thermal

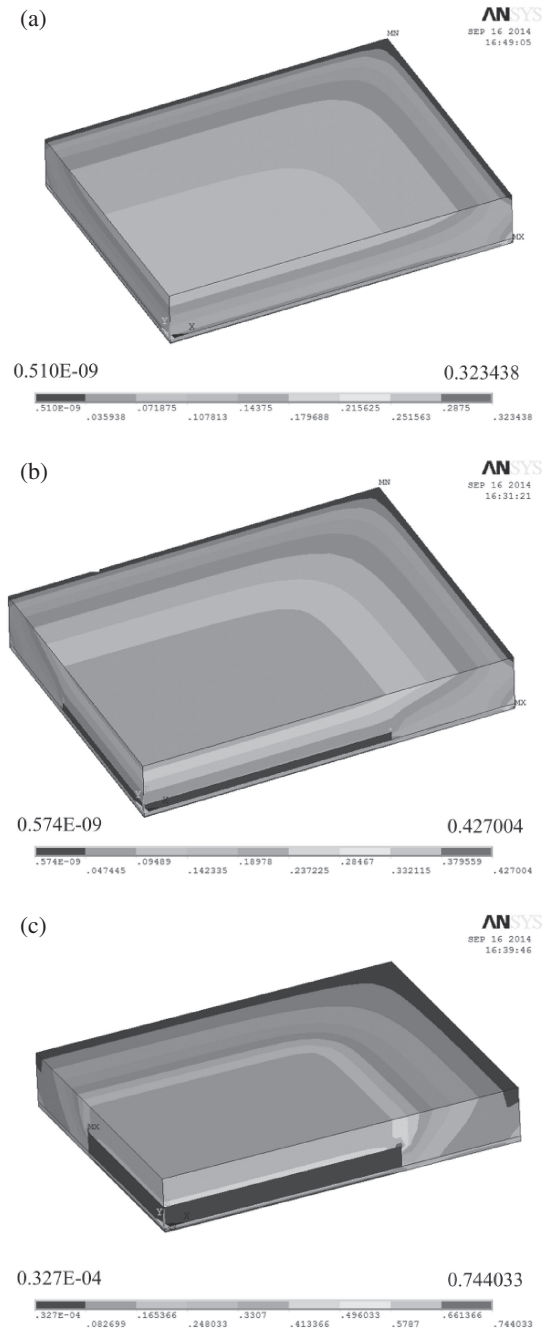


Fig. 8 Thermal gradients of (a) PKG000, (b) PKG200, (c) PKG520 (quarter model) at peak temperature (240°C).

gradient as shown in Fig. 8, which meant the thermal conduct was faster and temperature in it was under 240°C. Therefore the thermal gradient resulted in a decrease of warpage in PKG200 and PKG520 at peak temperature. Even so, the effect of thermal gradient on warpage was within 10%, and CTE mismatch was still the main cause of warpage in this paper. It should be noticed that the package in this experiment was simple and small. If the package grew larger or the structure was more complex, the thermal dissipation will be difficult and the thermal gradient may also influence warpage greatly.

### 3.3 Warpage thresholds for HiP

Based on warpage simulation and measurement, a warpage

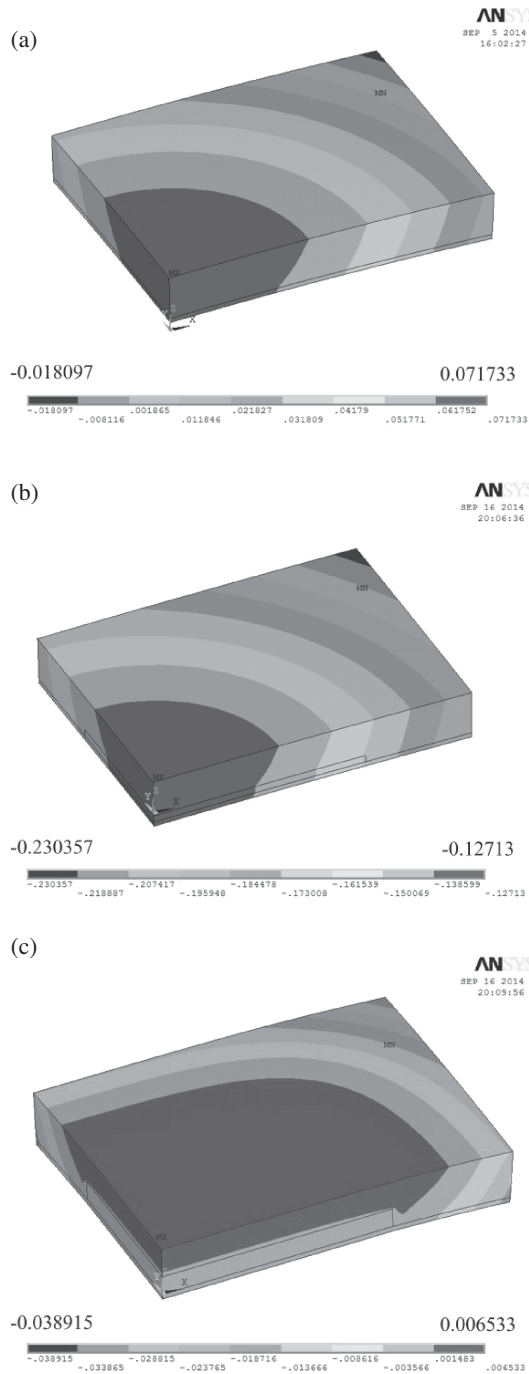


Fig. 9 Warpages of (a) PKG000, (b) PKG200, (c) PKG520 (quarter model) with element temperature set as 240°C.

threshold for HiP should be defined and measured. As the HiP forms when the solder is melting, the smallest package warpage value at peak temperature in a joint that forms an HiP is defined as the warpage threshold for HiP. Joints with warpage above the threshold will be at a high risk of HiP or opening defect while below it is safe. It is obvious that the larger warpage threshold, the better process window. A BGA rework station and a high speed camera were used to measure the warpage threshold for HiP during reflow. In the measurement, the samples were put on the BGA rework station to go through a reflow process and the whole process was recorded by a high speed camera. After reflow, the joints were examined to find where HiP occurred. Then the video

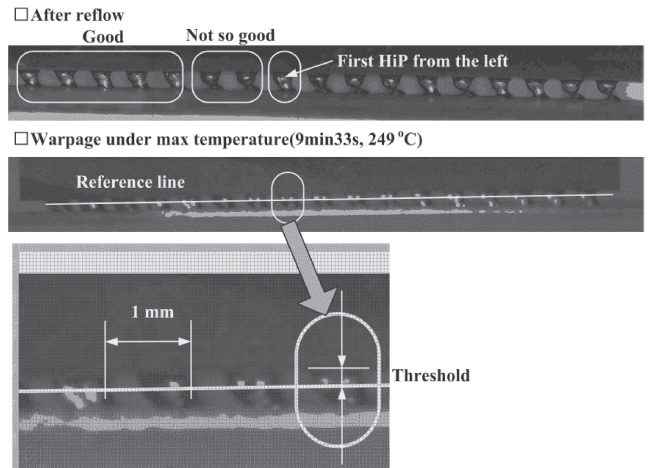


Fig. 10 Warpage threshold measuring method by using high speed video.

Table 2 Threshold measured results.

Package	Atmosphere oxygen content (ppm)	Position (number of solder joint counted from the left)	Threshold for HiP ( $\mu\text{m}$ )
PKG200	180	8	101
	air	4	54

was played back to observe the joint with HiP and work out the threshold of gap between solder ball and paste at peak temperature (as shown in Fig. 10).

For example, joints of PKG200 soldered in both air and  $\text{N}_2$  atmosphere were measured respectively and the result was listed in Table 2. The threshold for HiP was 54  $\mu\text{m}$  in air. Whereas, it was 101  $\mu\text{m}$  in  $\text{N}_2$ , 50  $\mu\text{m}$  larger than that in air. In  $\text{N}_2$  atmosphere, the solder oxidation is slight and flux activity can be kept for longer time, leading to a better contact condition compared with that in air.

#### 4. Conclusion

- (1) Package with a thick chip (PKG520) inside had the smallest max warpage (50  $\mu\text{m}$  at 240°C) while the package with no chip (PKG000) or thin chip (PKG200) had larger max warpage (above 90  $\mu\text{m}$  at 240°C). The probability of HiP increases by three times as warpage enlarges twice.
- (2) The package warpage was simulated with viscoelastic model of EMC. The discrepancy between simulation results and measured results were less than 20  $\mu\text{m}$ . And the CTE mismatch contributed more than 90% warpage at peak temperature according to the simulation.
- (3) A method was introduced to measure this threshold and according to the results, the threshold in  $\text{N}_2$  atmosphere was 50  $\mu\text{m}$  larger than that in air for PKG200.

#### Acknowledgments

This research was supported by Samsung Electronics Co., Ltd, by State Key Laboratory of Automotive Safety and Energy, Tsinghua University (Grant No. 2013XC-B-02),

National Natural Science Foundation of China (Grant No. 51375261), by The Natural Science Foundation of Beijing (Grant No. 3132020), by The Specialized Research Fund for Doctoral Program of Higher Education (Grant No. 20130002110009) and by Tsinghua University Initiative Scientific Research Program (Grant No. 2010THZ 02-1).

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