

Using Physics of Failure to Predict System Level Reliability for Avionic Electronics

IMAPS New England Conference

May 7, 2013

Agenda

- Introduction
- Avionic Applications
- Common Issues
- Failure Mechanisms
- Virtual Qualification Approach
- Automated Design Analysis Solution

Avionic Applications

ARINC 429-Mil-Std-1553 Module



Cobham-Carson Sikorsky Suite

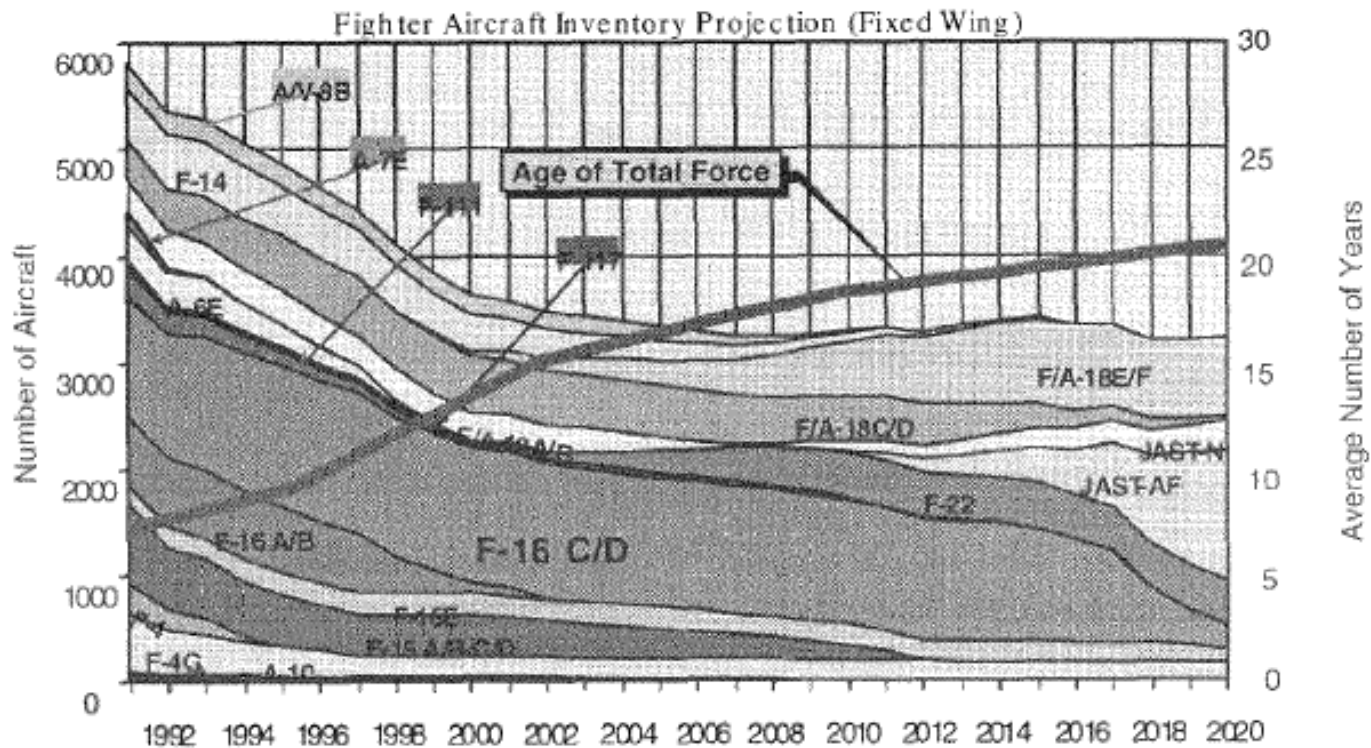


Gardner Aviation UniLink LRU



DfR Solutions

Aging Fleet



What Do they All Have in Common?

- High Temperature Environments
- Vibration (flight, gunfire) and Shock (Landing) Environments
- Temperature and Power Cycling Environments
- High Current Flows and Thermal Transfer Requirements
- A variety of materials forming the product

Stringent Environmental Conditions

- Being used at varying temperatures or temperature extremes
- Having a temperature range of -55°C to 125°C
- Being used in an application having a medium to high shock, pressure, vibration, or moisture environment
- Being stored for later usage (over 10 years)
- Having an application life span of greater than 30 years

Failure Mechanisms

- Thermo-mechanical fatigue induced failures
 - CTE mismatch
 - Temperature swings
- Bond Wire Fatigue
 - Shear Stresses between bond pad and wire
 - Repeated flexure of the wire
 - Lift off (fast temperature cycling effect)
 - Heel Cracking
- Die Attach Fatigue
- Solder Fatigue
 - Voids
- Device Burn Out

How Can We Resolve these Issues During the Design Phase of a Product?

- Utilize an Automated Design Analysis Approach Because:
 - Mil-HBK-217 actuarial in nature
 - Physics based algorithms are too time consuming
 - Need to shorten NPI cycles and reduce costs
 - Increased computing power
 - Better way to communicate

PoF: the Complexity Roadblock

$$\tau_{HCI} \propto \exp\left[\frac{b_{HCI}}{V_D}\right] \cdot \exp\left[\frac{E_{aHCI}}{kT}\right]$$

$$L = L_r \left(\frac{V_r}{V_0}\right) \times 2^{\left(\frac{T_r - T_A}{10}\right)}$$

$$T_f \propto \exp\left(\frac{\sim 0.51eV}{kT}\right) \times \exp(\sim -0.063\%RH)$$

$$\tau_{TDDB} \propto \exp[-b_{TDDB} \cdot V_G] \cdot \exp\left[\frac{E_{aTDDB}}{kT}\right]$$

$$N_f^{-0.6} D_f^{0.75} + 0.9 \frac{S_u}{E} \left[\frac{\exp(D_f)}{0.36} \right]^{0.1785 \log \frac{10^5}{N_f}} - \Delta \varepsilon = 0$$

$$\frac{t_1}{t_2} = \left(\frac{V_2}{V_1}\right)^n \exp\left[\frac{E_a}{K_B} \left(\frac{1}{T_1} - \frac{1}{T_2}\right)\right]$$

$$\tau_{EM} \propto (J)^{-n} \cdot \exp\left[\frac{E_{aEM}}{kT}\right]$$

$$\tau_{NBTI} \propto \exp[-b_{NBTI} \cdot V_G] \cdot \exp\left[\frac{E_{aNBTI}}{kT}\right]$$

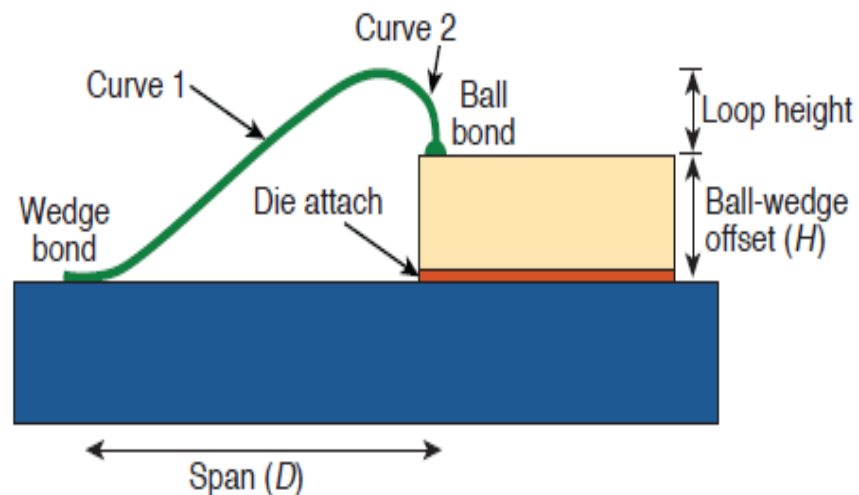
$$(\alpha_2 - \alpha_1) \cdot \Delta T \cdot L = F \cdot \left(\frac{L}{E_1 A_1} + \frac{L}{E_2 A_2} + \frac{h_s}{A_s G_s} + \frac{h_c}{A_c G_c} + \left(\frac{2 - \nu}{9 \cdot G_b a} \right) \right)$$

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Common Failure Modes

○ Wire Bonds

Wire bonding has been the most common interconnect for IC packages for over 50 years. The most common materials are gold, aluminum, and more recently copper. The most common bond pad material is aluminum.

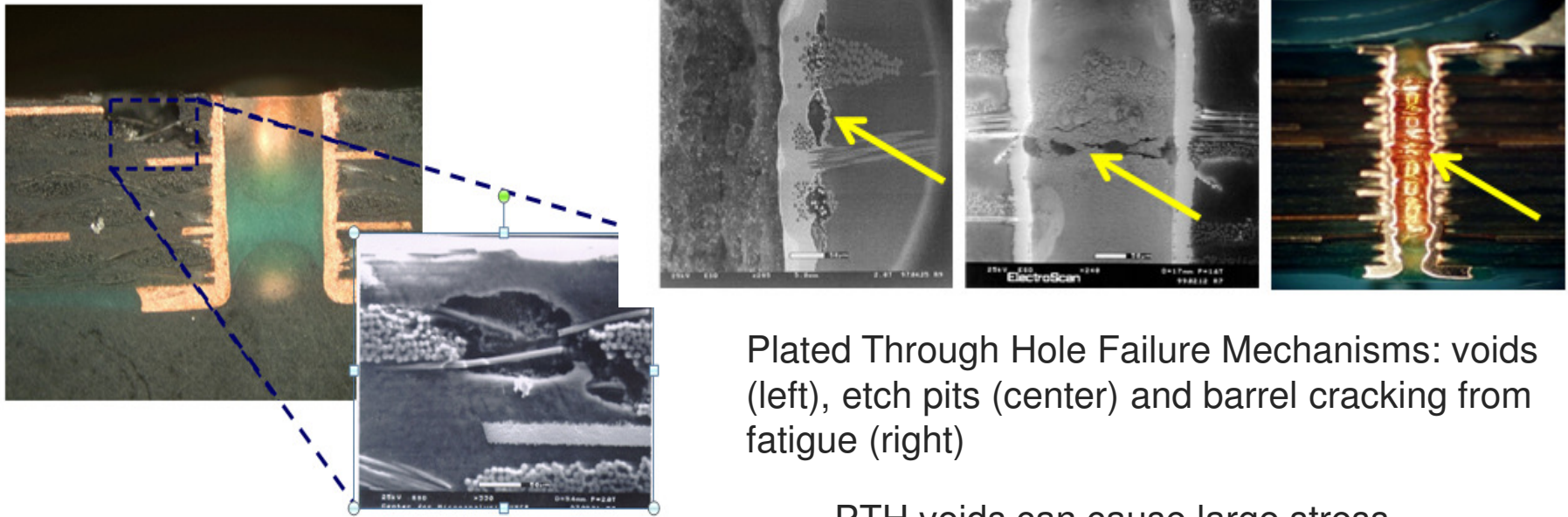


Wire bonds tend to fail if exposed to elevated temperatures (intermetallic formation), exposure to elevated temperature and humidity (corrosion) and exposure to temperature cycling (low cycle fatigue).

Common Failure Modes: PCBs

- Printed Wiring Boards have several failure modes that are detrimental to reliable operation. Failures in PCBs can be driven by:
- Size (larger boards tend to experience higher temperatures)
- Thickness (thicker boards experience more thermal stress)
- Material (lower T_g tends to be more susceptible)
- Design (higher density, higher aspect ratios)
- Number of reflow exposures

Common Failure Modes: PCBs



Plated Through Hole Failure Mechanisms: voids (left), etch pits (center) and barrel cracking from fatigue (right)

Conductive anodic filament (CAF), also referred to as metallic electromigration, is an electrochemical process which involves the transport (usually ionic) of a metal across a nonmetallic medium under the influence of an applied electric field. CAF can cause current leakage, intermittent electrical shorts and dielectric breakdown between conductors in printed wiring boards.

PTH voids can cause large stress concentrations, resulting in crack initiation.

Etch pits are due to either insufficient tin resist deposition or improper outer-layer etching process and rework.

Overstress cracking can occur in the PTH due to a Coefficient of Thermal Expansion (CTE) mismatch which places the PTH in compression.

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Common Failure Modes: Solder Fatigue

- Thermo-Mechanical Fatigue of solder joints is one of the primary wear-out mechanisms in electronic products. This is especially true in products used outside of commercial/ consumer environments where a longer lifetime is required and more severe operating conditions exist. The analysis assesses the fatigue of the solder joints as a function of the stresses applied during its lifetime and provides insight into whether joints are susceptible to failure.



Automated Design Analysis Attributes

- Easy to Utilize
- Easy to Locate commands
- Industry Terminology
 - Parts List
 - Stack-up
 - Pick and Place
 - ODB++
 - GERBER

Automated Design Analysis

- There are several high levels steps involved in performing an automated design analysis. They are:
 - Define Reliability Goals
 - Define Environments
 - Add Circuit Cards
 - Import Files
 - Generate Inputs
 - Perform Analysis
 - Interpret Results

Reliability Goals

The screenshot shows the Sherlock software interface with a project tree on the left and a 'Life Cycle Editor' dialog box in the foreground. The project tree includes folders like 'Antilock Braking System', 'Heart Pump', 'HVAC Controller', 'Keyfob', 'Network Switch', 'Satellite Communication', 'Solar Inverter', 'Thrust Reverser', 'Life Cycle', 'Project Results', and 'Annunciator'. The 'Life Cycle' folder is expanded, showing 'Phase 1' with sub-items: '1 - Mechanical Shock', '2 -Flight Thermal Cycle', '3 - Diurnal Profile', and '4 - In flight random Vibration'. The 'Life Cycle Editor' dialog box has a title bar and a close button. It contains the following text: 'Modify any of the following properties and press the Save button to update the current life cycle for this project. Press the Load Life Cycle button to load a different life cycle from the file system or the Save Life Cycle button save the current life cycle in a named file. Life cycle files can be used in other projects and/or shared with other Sherlock users.' Below this text are two sections: 'Identification' with 'Name: Life Cycle' and an empty 'Description' field; and 'Reliability Goals' with 'Reliability Metric: 30' and 'Service Life (years): 20'. A dropdown menu is open for the 'Reliability Metric' field, showing options: 'Prob. of Failure (%)', 'Reliability (%)', 'Prob. of Failure (%)', 'MTBF (years)', 'MTBF (hours)', 'FITs (1E6 hrs)', and 'FITs (1E9 hrs)'. At the bottom of the dialog box are 'Save' and 'Reset' buttons.

Ambient Environment

The screenshot displays the Sherlock software interface. On the left is a project tree with a tree view containing:

- Antilock Braking System
- Heart Pump
- HVAC Controller
- Keyfob
- Network Switch
- Satellite Communication
- Solar Inverter
- Thrust Reverser
 - Life Cycle
 - Phase 1
 - 1 - Mechanical Shock
 - 2 - Flight Thermal Cycle
 - 3 - Diurnal Profile
 - 4 - In flight Random Vibration
- Project Results
 - Annunciator
 - Files
 - Inputs
 - Analysis
 - Results
 - CONTROLLER

A green arrow points from the 'Annunciator' folder in the tree to the 'Thermal Event Editor' dialog box. The dialog box has the following sections:

- Identification:** Name: 2 - Flight Thermal Cycle; Description: (empty)
- Thermal Event Settings:** # of Cycles: 730; PER YEAR (dropdown)
- Thermal Profile:** Profile #1 graph showing Temperature (C) vs Time (min). The graph shows a step function where temperature is -25C until 125 minutes, then jumps to 75C and stays there until 250 minutes.

At the bottom of the dialog are buttons: Load Profile ..., Edit Profile ..., Save Profile ..., Save, Reset, Cancel.

On the right side of the interface, there are two graphs:

- Harmonic Sweep Profile:** titled 'gunfire_conditions'. The y-axis is Load (G) from 0.0 to 7.5. The x-axis is Frequency (HZ) from 0 to 2,000. The graph shows a step function with a peak of 7.5G between 750 and 1,500 Hz.
- Random Vibe Profile:** titled 'Flight Random Performance-gc'. The y-axis is Amplitude (G²/Hz) from 0.00 to 0.35. The x-axis is Frequency (HZ) from 0 to 2,000. The graph shows a multi-peaked profile with a maximum amplitude of approximately 0.28 G²/Hz between 1,000 and 1,250 Hz.

Handles Very Complex Environments



Input Design Files

The screenshot displays the Sherlock software interface. On the left, a project tree lists various systems: Antilock Braking System, Heart Pump, HVAC Controller, Keyfob, Network Switch, Satellite Communication, Solar Inverter, Thrust Reverser, Life Cycle (with Phase 1 sub-items: Mechanical Shock, Flight Thermal Cycle, Diurnal Profile, In flight Random Vibration), Project Results, Annunciator (with sub-items: Files, Inputs, Analysis, Results), and CONTROLLER. An arrow points from the 'Inputs' sub-item under 'Annunciator' to the 'Edit File Properties' dialog box.

The 'Edit File Properties' dialog box is open, showing options for File Type, Comment, Pick & Place, # of Heat, Reference ID, X Coordinate, Y Coordinate, Footprint, Rotation, Board Side, and Description. The File Type dropdown is set to 'Pick & Place (CSV)'. The 'Location Units' field is set to 'in'. Buttons for 'Guess' and 'Save' are visible at the bottom.

The main workspace shows a detailed PCB layout for the 'ANNUNCIATOR BOARD ASSY'. The board is populated with numerous components, including resistors (R1-R46), capacitors (C1-C8), integrated circuits (U1-U8), and other components (Q7, Q8, Q9, VR3). The layout is color-coded, with components highlighted in green and red. The board is labeled 'ANNUNCIATOR BOARD ASSY' and '05232'.

Input: Parts List

The screenshot displays a software interface for managing parts. The main window shows a 'Main Board Parts List' with a table of parts. The table has columns for 'Ref Des', 'Part Number', and 'Part Type'. The parts are color-coded: blue for confirmed, yellow for unconfirmed, and orange for guess. A 'Part Properties - U94' dialog box is open, showing properties for a selected part. The dialog has tabs for 'ID', 'Pkg', 'Thermal', 'Loc', 'Ball', 'Pad', 'Die', 'Flag', 'Lead', and 'Qual'. The 'Ball' tab is active, showing properties like 'Ball Pattern', 'Ball Count', 'Ball Units', 'Ball Pitch', 'Ball Diameter', 'Ball Height', and 'Ball Chan Width'. Two 'Package Chooser' dialog boxes are also open, showing a list of packages with columns for 'Package Type', 'Pin Count', 'Size (mm)', and 'Package Name'. The packages are color-coded: blue for confirmed, yellow for unconfirmed, and orange for guess. The 'Package Chooser' dialog boxes show a list of packages with columns for 'Package Type', 'Pin Count', 'Size (mm)', and 'Package Name'. The packages are color-coded: blue for confirmed, yellow for unconfirmed, and orange for guess. The 'Package Chooser' dialog boxes show a list of packages with columns for 'Package Type', 'Pin Count', 'Size (mm)', and 'Package Name'. The packages are color-coded: blue for confirmed, yellow for unconfirmed, and orange for guess.

Ref Des	Part Number	Part Type
U110	075-1313-5	IC
U700	075-0973-5	IC
U701	075-0973-5	IC
U702	075-0700-5	IC
U703	075-0700-5	IC
U704	075-0700-5	IC
U705	075-0700-5	IC
U707	075-0676-5	IC
U708	075-0676-5	IC
U709	075-0676-5	IC
U710	075-0676-5	IC
U720	075-0686-5	IC
U721	075-0686-5	IC
U722	075-0736-5	IC
U724	075-1154-5	IC
U727	075-0560-5	IC
U728	075-0700-5	IC
U730	075-0667-5	IC
U731	075-0667-5	IC
U732	075-1154-5	IC
U733	075-0667-5	IC
U734	075-1386-5	IC
U738	075-0853-5	IC
Y2	076-0050-5	IC
Y3	076-0050-5	IC
Y4	076-0050-5	IC

- Color coding of data origin
- Minimizes data entry through intelligent parsing and embedded package and materials database

Inputs: Stack-Up

Stackup Properties

The following board properties are based on the currently defined board outline and the individual layer properties shown below:

Board Size: 370 x 178 mm [14.6 x 7.0 in]	CTExy: 17.519 ppm/C
Board Thickness: 1.6 mm [62.0 mil]	CTEz: 58.646 ppm/C
Board Density: 2.8515 g/cc	E_{xy}: 35,743 MPa
Copper Layers: 10	E_z: 4,379 MPa

Stackup Layers

Double click any row to edit the properties for that layer or select one or more rows and press the **Edit Selected** button below to edit properties for a batch of layers. Press the **Generate Stackup Layers** button to replace all layers using a given PCB thickness and default layer properties.

Layer	Type	Material	Thickness	Density	CTExy	CTEz	E _{xy}	E _z
1	POWER	COPPER (33.7%)	1.0 oz	4.1927	21.180	21.180	45.838	45.838
2	Laminate	Generic FR-4					24.804	3,450
3	POWER	COPPER (92.2%)					105.099	105.099
4	Laminate	Generic FR-4					24.804	3,450
5	POWER	COPPER (50%)					62.350	62.350
6	Laminate	Generic FR-4					24.804	3,450
7	POWER	COPPER (92.2%)					105.099	105.099
8	Laminate	Generic FR-4					24.804	3,450
9	POWER	COPPER (91.1%)					103.984	103.984
10	Laminate	Generic FR-4					24.804	3,450
11	POWER	COPPER (19.9%)					31.859	31.859
12	Laminate	Generic FR-4					24.804	3,450
13	POWER	COPPER (92.2%)					105.099	105.099
14	Laminate	Generic FR-4					24.804	3,450
15	POWER	COPPER (23.2%)					35.202	35.202
16	Laminate	Generic FR-4					24.804	3,450
17	POWER	COPPER (92.2%)					105.099	105.099
18	Laminate	Generic FR-4					24.804	3,450
19	POWER	COPPER (20.9%)					32.872	32.872

Edit Selected Layers

Enter any fields to be updated in all selected layers. If a field is left blank, then the current field value will remain unchanged for each layer.

Laminate Layer Properties

Laminate Material: Generic FR-4

Laminate Thickness: Generic

Grace
Hitachi
ITEQ
Isola
Kingboard
LG Chemical
Mitsubishi

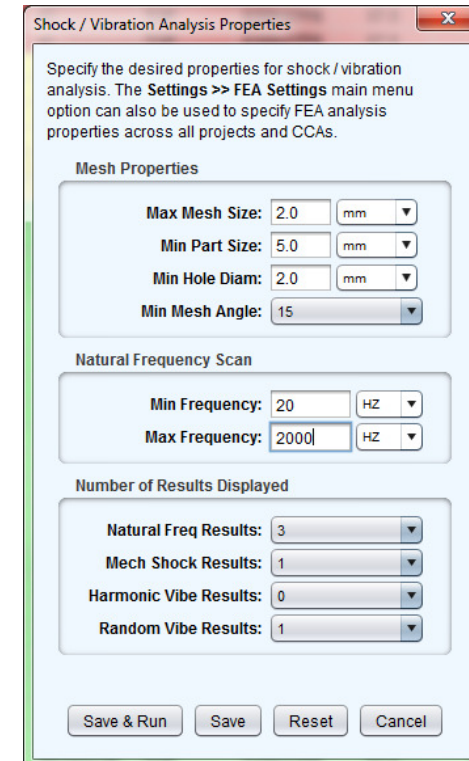
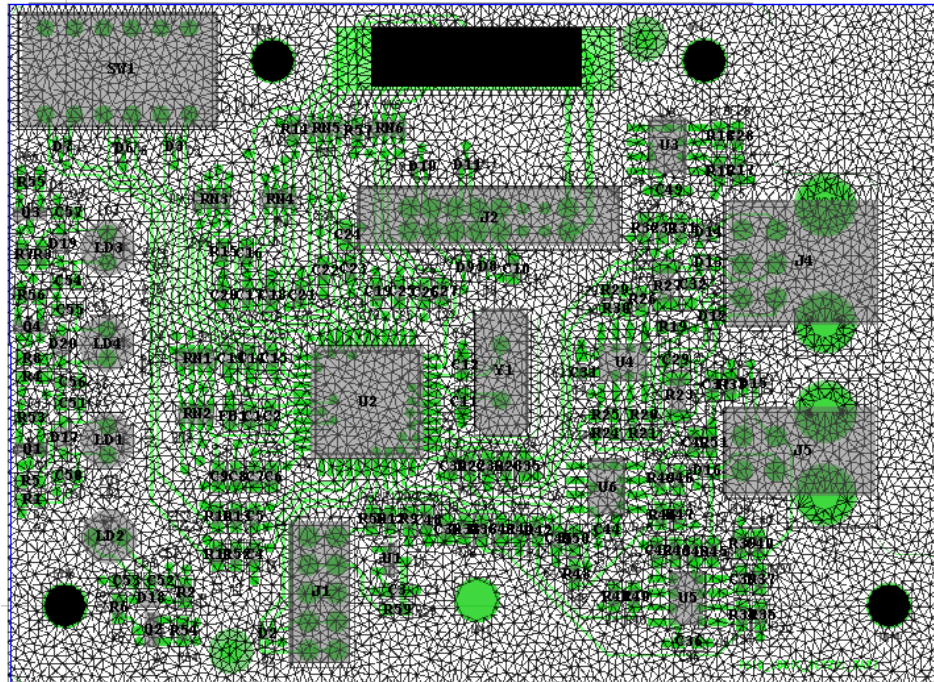
Cancel

- Automatically generates stackup and copper percent (%)
- Embedded database with almost 400 laminate materials with 48 different properties

Analyses

- Eight different analyses can be performed. They are:
 - CAF – Conductive Anodic Filament Formation
 - Plated Through Hole Fatigue
 - Solder Joint Fatigue
 - Finite Element Simulations
 - ICT Impact
 - DFMEA
 - Vibration Fatigue - Natural Frequencies
 - Mechanical Shock

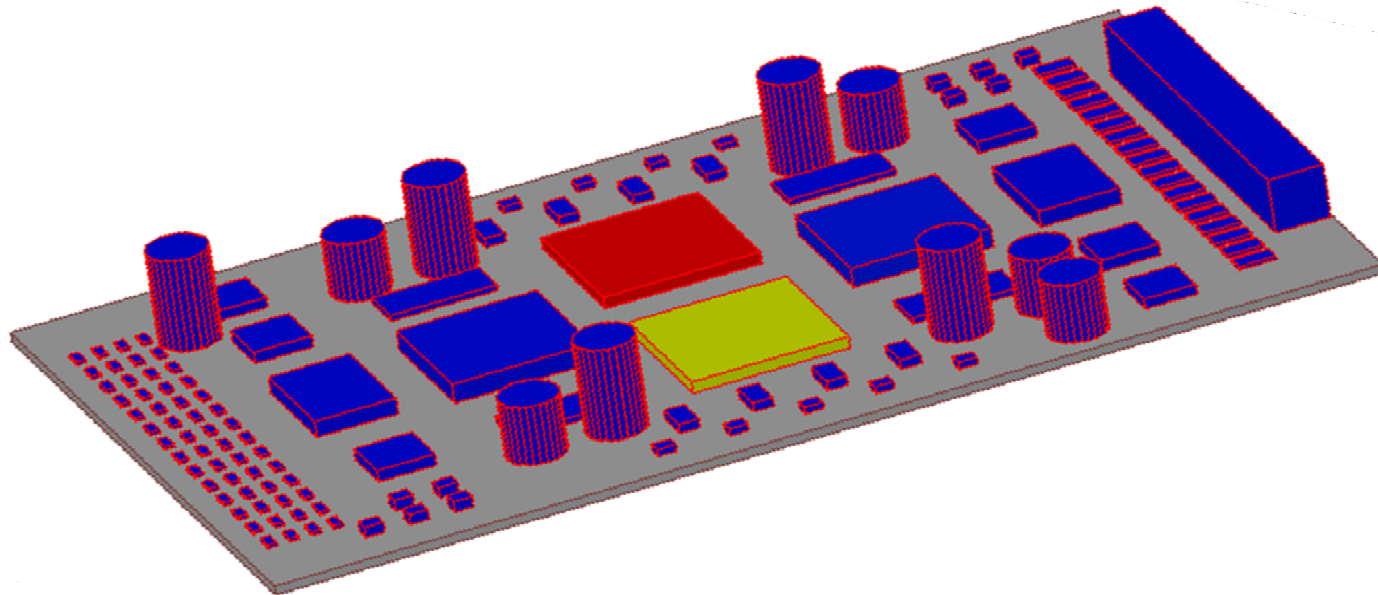
Results: Automated Mesh Generation



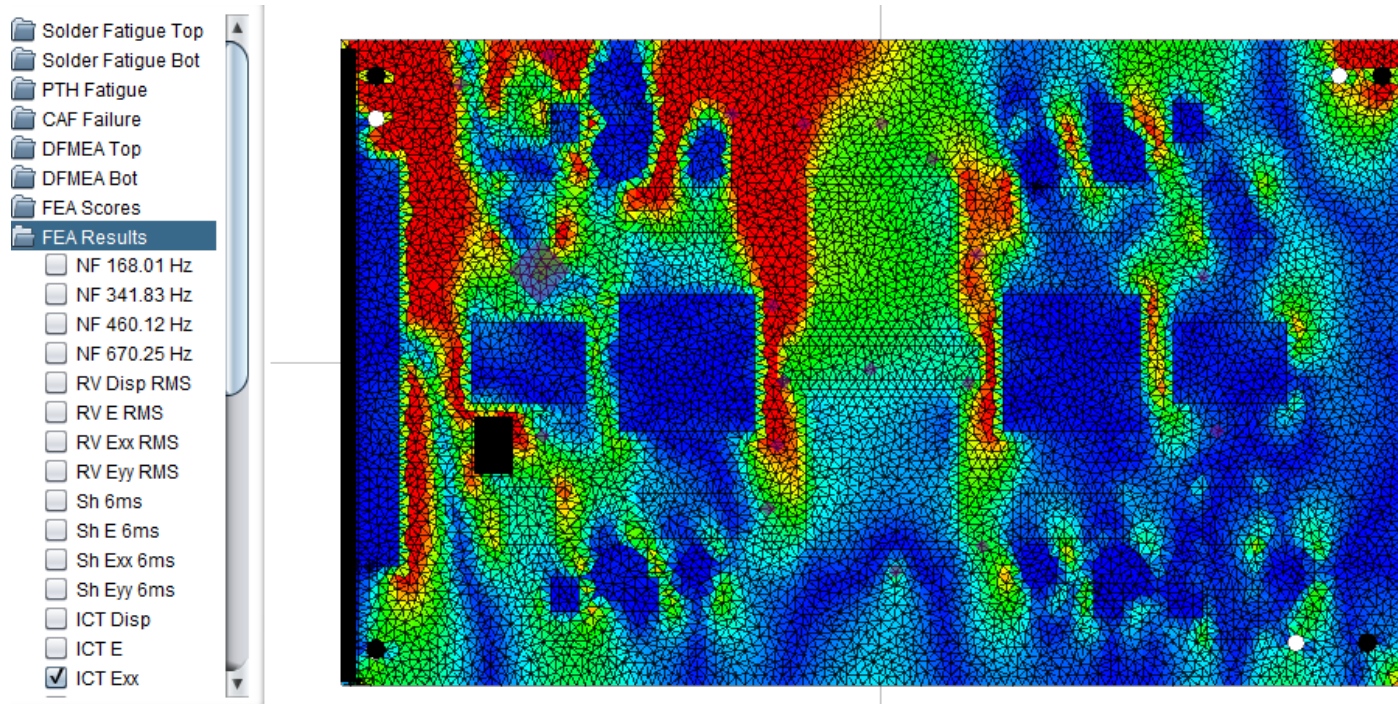
- Identifies optimum mesh density based on board size
- Expert user no longer required; model time reduced by 90%

3D Output

The analysis can also establish 3D models by creating a mesh structure and the model from the data input to the analysis.



In-Circuit Test Evaluation



- Uses embedded FEA engine to compute board deflection and strain cause by ICT fixture

DFMEA

Navigation

- Open - Pin 17 (N127243)
- Open - Pin 18 (N127703)
- Open - Pin 19 (N127703)
- Open - Pin 20 (GND)
- Short - Pins 1 (PLCC20-1) & 2
- Short - Pins 1 (PLCC20-1) & 20
- Short - Pins 5 (N124525) & 6 (N124525)
- Short - Pins 7 (N124972) & 8 (N124972)
- Short - Pins 9 (N125421) & 10 (N125421)
- Short - Pins 11 (N125875) & 12 (N125875)
- Short - Pins 15 (N126785) & 16 (N126785)
- Short - Pins 17 (N127243) & 18 (N127243)
- Short - Pins 19 (N127703) & 20 (N127703)
- U2
 - Logic Failure
 - Open - Pin 1 (PLCC20-2)
 - Open - Pin 2 (N131610)
 - Open - Pin 3 (N131610)
 - Open - Pin 4 (N131614)
 - Open - Pin 5 (N131614)
 - Open - Pin 6 (N131618)
 - Open - Pin 7 (N131618)
 - Open - Pin 8 (N131622)

Subcircuit Properties

Subcircuit Name: UNASSIGNED

Description:

Part Properties

Part Designator: U2

Description: IC ADV PWM MOTOR CTRL LCCC-20

Failure Mode Properties

Failure Mode: Logic Failure

Potential Cause: Device failure

Potential Effect:

SEV: 8

OCC: 2

DET: 2

RPN: 32

- Uses ODB++ data including net list to create board level DFMEA
- Includes customizable spreadsheets for export

Results: Five Different Outputs

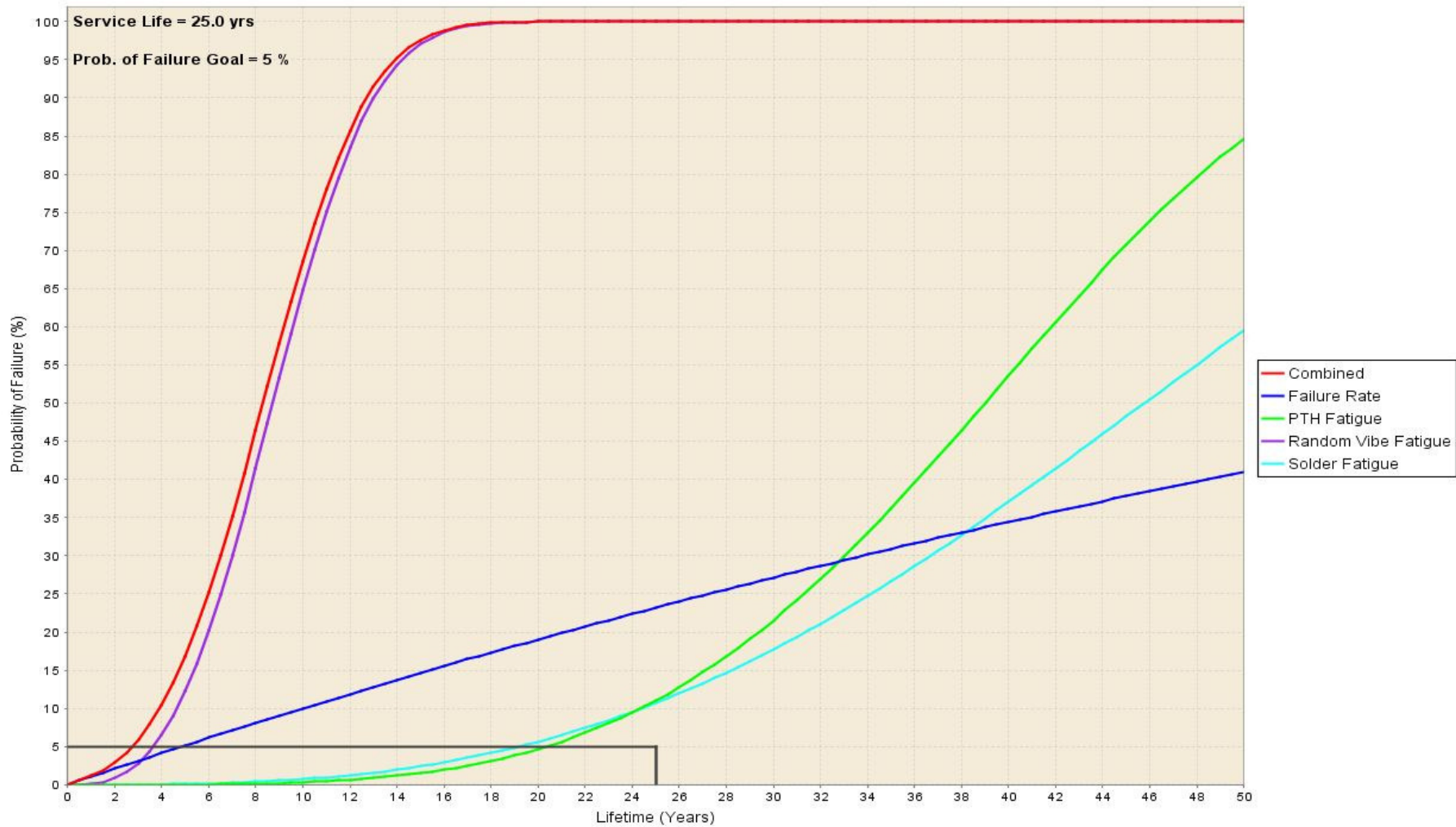
The image displays five screenshots from the Sherlock software interface, illustrating different types of analysis results for a PCB project named 'Antilock Braking System dfr-vibration-coupon4 Solder Fatigue'.

- Top Left:** 'Solder Fatigue' analysis results. It shows a 'Module Score' of 0.0 and an 'Analysis Type' of 'Deterministic'. A bar chart indicates the distribution of components: 7 or more (192, 96.0%), 3 to 7 (6, 3.0%), and less than 3 (2, 1.0%).
- Top Right:** A table of component failure data. The table lists components like U11 (LCCC-44 IC) and U9 (BGA676 IC) with their respective failure rates and scores.
- Middle Left:** 'Analysis Statistics' and 'Board Prop'. It shows 'Parts Analyzed: 200' and 'Reliability Goals' such as 'Service Life: 10 yrs' and 'Failure Prob Goal: 10.0%'.
- Middle Right:** 'Antilock Braking System dfr-vibration-coupon4 - Solder Joint Fatigue Life Prediction'. A graph showing 'Probability of Failure (%)' vs 'Lifetime (Years)'. It includes a 'Service Life = 10.0 yrs' and a 'Prob. of Failure Goal = 10%'.
- Bottom Left:** 'Antilock Braking System dfr-vibration-coupon4 - Distribution'. A histogram showing the distribution of 'Time To Failure (years)' for all components.
- Bottom Right:** A PCB layout view showing 'Solder Fatigue Top'. It includes a 'Filters' panel with settings for Part (0.0), Hole (0.0), and Label.

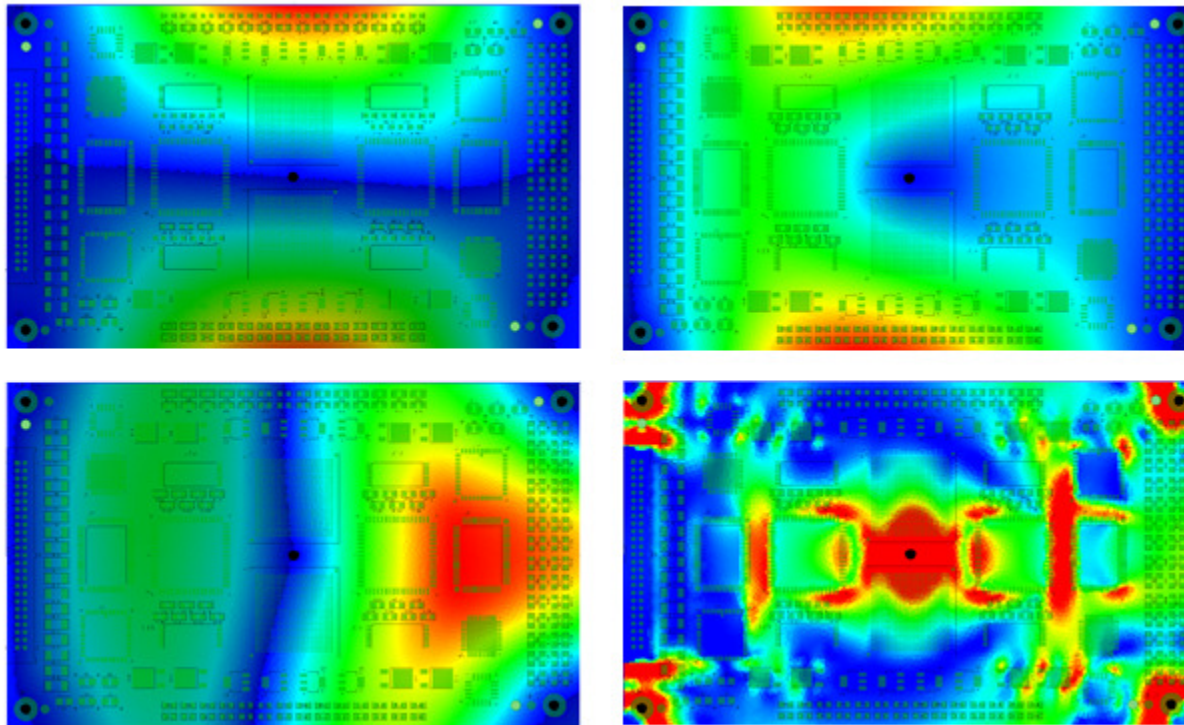


Unreliability Curves

Tom's Demo ODB++ Tutorial - Life Prediction



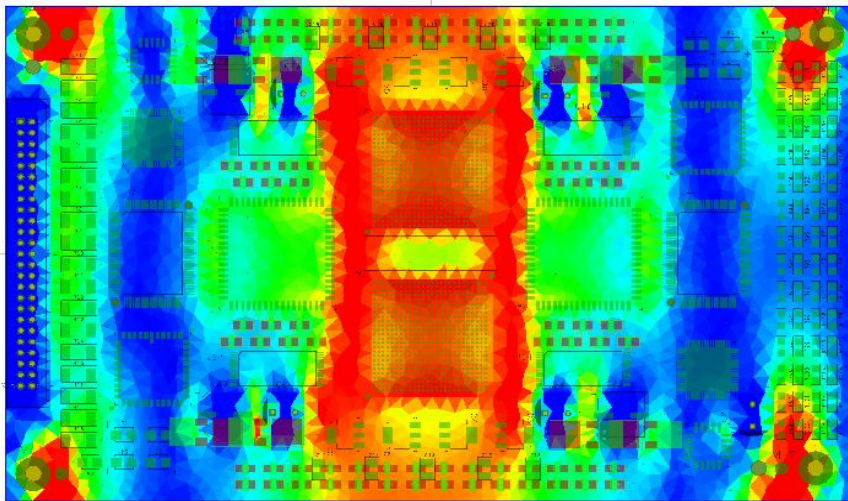
Natural Frequencies



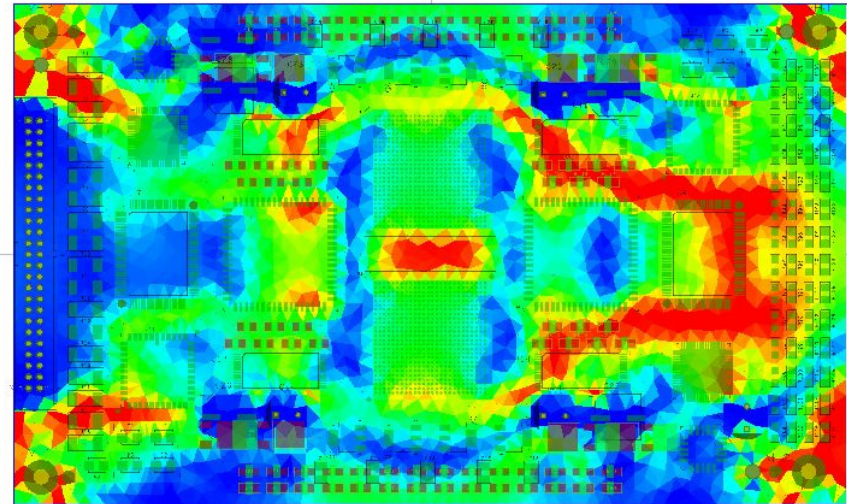
Natural Frequencies Identified (1st-upper left), (2nd-upper right), (3rd -lower left) and 4th – lower right)

Vibration Strain Levels

Solder Fatigue Bottom / PTH Fatigue / Random Vibration RMS XX Strain / Failure Rate...



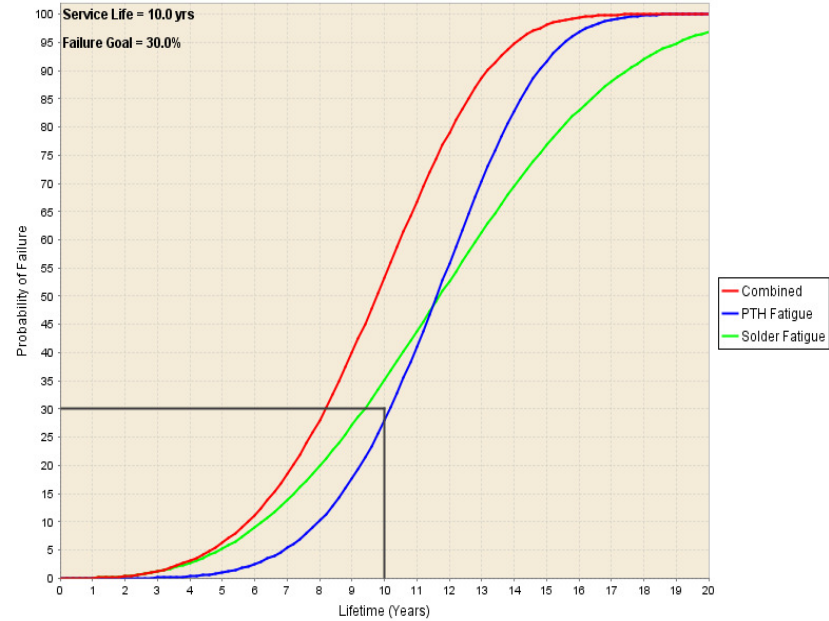
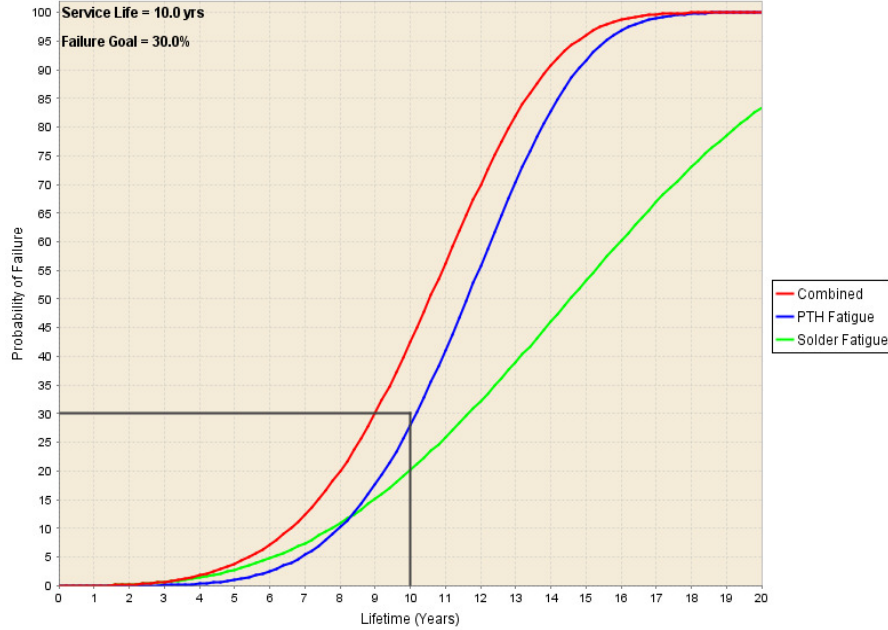
Solder Fatigue Bottom / PTH Fatigue / Random Vibration RMS YY Strain / Failure Rate ...



In addition, the analysis can provide data regarding the strains applied to the circuit board as a function of the vibration stress levels. The left illustrates this data in the XX direction and YY in the right image.

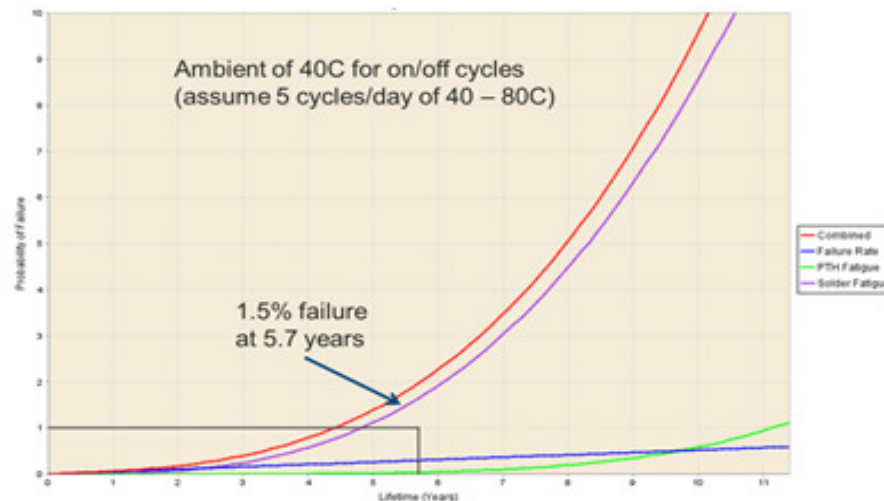
What If?

Comparison of Sn/Pb (left) and SAC305 (right) with respect to solder fatigue



Product Test Plans

- Product test plans, also known as design verification, product qualification, and accelerated life testing (though, these are not the same thing), are critical to the successful launch of a new product or new technology into the marketplace.
- These test plans require sufficient stresses to bring out real design deficiencies or defects, but not excessive levels that induce non-representative product failure.
- Tests must be rapid enough to meet tight schedules, but not so accelerated as to produce excessive stresses.
- Every test must provide value and must demonstrate correlation to the eventual use environment (which includes screening, storage, transportation/shipping, installation, and operation).





Thank You!

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