The Long-term Shaping of the JTAG/Boundary-scan Standards

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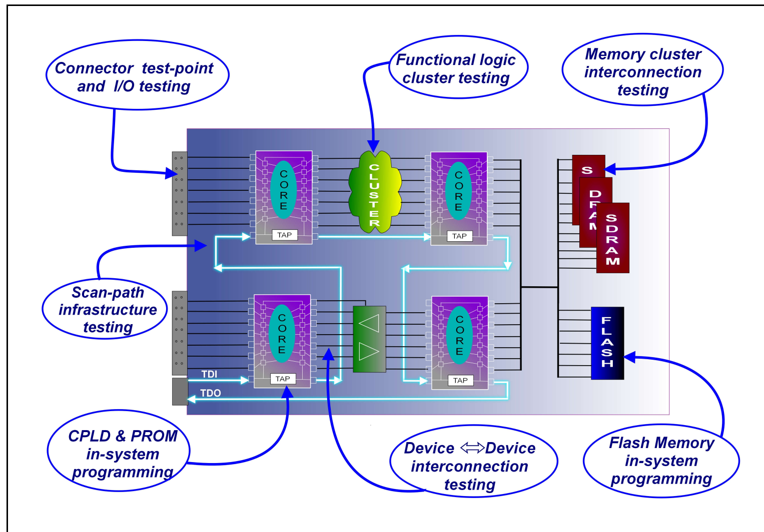
Originating from the last millenium, almost three decades ago, the introduction of surface mount packaging triggered a wave of changes throughout many aspects of electronics production. A small number of talented, innovative test engineers from various big players of the industry started to attend meetings to discuss the impact of that change of technology on their future test concepts for modern assemblies. The Joint Test Action Group was born.

In most cases PCB testing at that time (mid 1980s) had been accomplished using ICT (In-Circuit Testers) for individual component and PCB testing, or functional testers that could mimic the environment of the UUT (Unit Under Test) to send/receive stimulus and response signals. The work of the JTAG committee however would change the test landscape dramatically.

The fruits of their labor was the now familiar 'Test Access Port and Boundary-scan Architecture' (aka IEEE 1149.1), and it describes how an embedded serial scan register can access digital signal pins of its host device to either capture an input signal or propagate an output signal through the pin of the device while isolating its regular function. By applying test patterns across interconnections between devices, assemblies could be tested for open circuits and shorts. Soon after tests were being developed that could stimulate and check the interconnects to RAMs, Flash and other logic parts. A few years after that the JTAG TAP was being used access for configuring/programming PLDs FPGAs and microcontrollers.



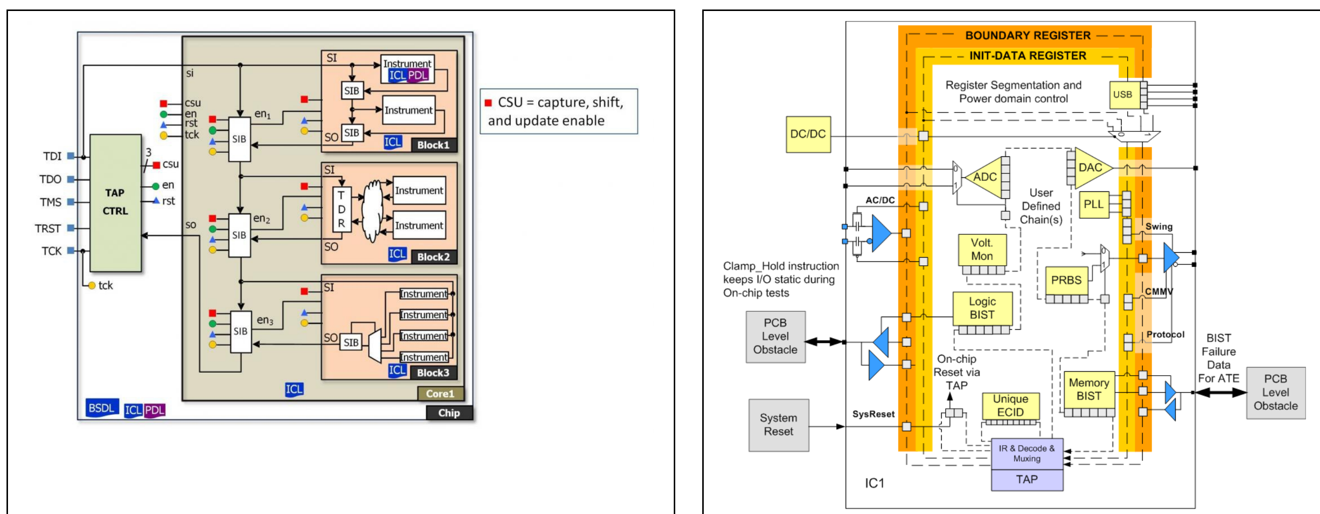
Fast forward 30 years and you can see that JTAG/IEEE 1149.1 usage for both testing and programming has become mainstream, being used extensively in testing of PCB assemblies within Defense, Aerospace, Telecoms Automotive, and Industrial sectors. Yet the need to pre-empt future test issues remains a constant and current wisdom suggests more 'at-speed' testing through use of [device] embedded instruments is to be encouraged

The most recent major update to standard 1149.1 came in 2013 with a sizable addendum to the original work which came about following a period of intense activity around 2010, with two separate groups proposing similar updates to the existing 1149.1 standard, which was by then 20 years old. As well as 1149.1 2013 there also existed a group working on IEEE 1687. Both groups had identified deficiencies in the existing standard and both groups have addressed these through the introduction of more 'dynamic' IC infrastructures. In the case of 1149.1 2013 the driver for the changes was to standardise some of the design practices that IC vendors had introduced on a unilateral basis, such as initialisation protocols, individual device id codes and power management scenarios. While in the case of 1687 the main driver was to improve board-level 'testability' through the greater use of embedded test cores (BIST IP) accessed via an extended standardised infrastructure.

The now-ratified extension to 1149.1 has more than doubled the size of the descriptive document to 444 pages and includes the syntax of a new procedural description language (PDL) that is used to define the usage of the dynamic

register segmentation and device IP hierarchy for a given application. IEEE 1687 meanwhile also features PDL, however there is only a basic level of compatibility between the two PDLs – apparently due to the *vastly* different focus of each new standard ! PDL is designed to document the procedures for stimulating and observing test data register fields for 1149.1-2013 and in P1687, the procedures for stimulating and observing data to an instrument. Not much of a difference except that in P1687 a second language is required to describe the [embedded instrument] access networks – ICL (Instrument Control Language) while in 1149.1-2003 the access network descriptions are embedded in an extended BSDL model. For complex networks that make extensive use of embedded instruments P1687s ICL is claimed to be better suited.

Below you can see redrawn block diagrams of the two 'competing' standards so the differences can be made clear.



The argument for the continued development of standards are clear. Chiefly these are a) to keep the technology relevant to today's designs and b) to ease the task of tool vendors who rely on standard techniques to achieve maximum levels of automation in application generation. c) expand the market potential of a given methodology.

What else is in store for the future ? Well I think we can expect expansion of the features for enabling JTAG to go in two, more or less opposite, directions. 1)

More embedded testing at device level (as per IEEE 1687 and IEEE 1149.7) and 2) extended infrastructures for system-level access and test as espoused by the SJTAG committee (see www.sjtag.org) who's purpose is stated on the web-site as follows – '..*to provide an extension of the IEEE 1149.1 standard specifically aimed at enabling the configuration, control, management, and representation of the communications required at the hierarchical system and board levels to perform operations on the IEEE 1149.1 Test Access Port (TAP) of one or more devices or device cores, in a uniform and transportable way across all system modules.*

However, it is a slow process and only time will tell if the 'standard makers' can offer a needed system that is both timely and profitable for the silicon vendors to implement. In the world of test standards much good work has now been put into everyday use while other developments have withered on the vine. There has always been a difficult balancing act in developing viable test methods that can be standardised and used profitably.

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