ASSEMBLY AND RELIABILITY ISSUES ASSOCIATED WITH LEADLESS CHIP SCALE PACKAGES

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ABSTRACT
This paper addresses the assembly and reliability of 0.5 mm pitch leadless Chip Scale Packages (CSP) on .062" immersion Ag plated printed circuit boards (PCB) using Pb-free solder paste. Four different leadless CSP designs were studied and each was evaluated using multiple PCB attachment pad designs.

Assembly was performed by stencil printing solder paste over the PCB pads, placing components with a high-speed placement machine, and reflowing in a forced convection oven. Vision issues were encountered during the placement process and a "video model" was required to place certain leadless packages.

Post assembly characterization included electrical measurements, visual inspection, X-ray inspection, and representative cross-sectioning to examine the 2nd level solder interconnects. Assemblies were subjected to 20-minute 0-100°C air-to-air thermal cycles. Cycle to failure (CTF) data was found to be quite sensitive to optimization of the solder paste printing process and, possibly, to the board pad dimensions.

INTRODUCTION
Leadless CSPs are leadframe packages characterized by their low assembly profile (see Figure 1), which may be 50% lower than traditional CSPs. Leadless packages are also lighter and fairly inexpensive. These packages are ideal for consumer electronic products, personal telecom, and datacom devices. Leadframe packages are also the preferred choice for RF applications due to their short lead length that results in low inductance and capacitance [8,9].

Phenomenal growth is predicted for leadless package usage, with estimates of more than 1.8 billion in 2004 [8, 9], and the devices are expected to replace QFP, SOIC, and SOT style packages in the near future [8, 9].

Leadless CSPs require the creation of second level interconnections by deposition of either a solder paste or conductive adhesive. While they usually contain SnPb finishes, this is not a critical feature and replacement with either an Organic Solder Protect (OSP) coating or Ni/Au structure would readily facilitate a transition to Pb-free assembly. Notably, the industry is justifiably concerned about the unavoidable transition period during which some components will only be available with SnPb balls and others only with no-Pb. Any component offered without solder obviously leaves the choice of paste alloy up to the assembler. Three of the present packages discussed were supplied with a SnPb finish, while one package utilized a resin bump.

Leadless CSPs tend to be small and, because of their construction, are resistant to moisture and warpage. Most utilize a perimeter land array pattern with an exposed die paddle located beneath the silicon die (see Figure 1). The die paddle may be soldered directly to the PCB to enhance heat dissipation and electrical grounding (see Figure 2). The actual heat transfer efficiency can be further improved by the use of thermal vias from the PCB heat land to the ground planes.

A significant concern is, of course, assembly reliability. Because of the much lower standoff, thermal mismatch induced strains in the solder joints are generally much larger than for bumped or leaded devices. While individual companies and industry consortia have been researching the issues [13] there is currently little published data on the reliability of leadless CSP assemblies.

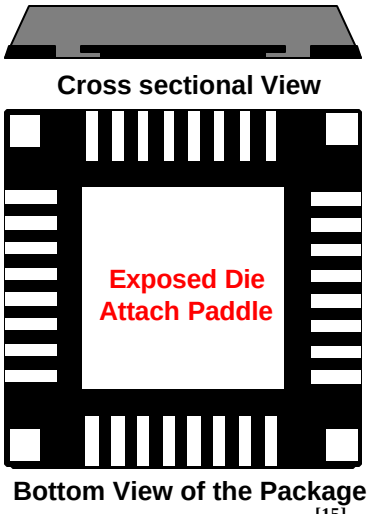

Figure 1: Leadless Chip Scale Package [15]

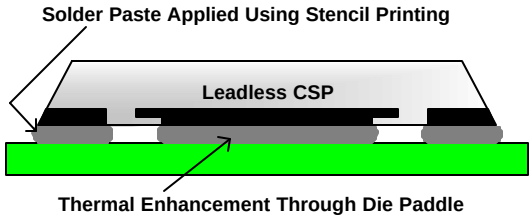

Figure 2: Thermal Enhancement through Die Paddle [15]

The present work addresses Pb-free assembly and the resulting reliability of four representative leadless CSPs.

ASSEMBLY MATERIALS

Four different packages were considered in the present study, all square or nearly square with 40-48 I/O on 0.5 mm pitch. Three of the devices (A, B, C) were ¼" packages with terminations on all four sides, whereas the fourth device (D) was 0.43" long with terminations along two sides.

The four packages evaluated were similar in construction. However, the packages varied in die dimensions and die paddle usage as summarized in Table 1.

Table 1: Package Description

Pkg	Die Dimensions	Die Paddle
A	148 x 148	Yes
B	No Die	Yes
C	166 x 166	No
D	138.2 x 138.2	No

All dimensions in mils

The components were all soldered to immersion Ag plated copper pads on a 62 mil thick, high-T_g FR-4 printed circuit board using a type 3 no-clean 95.5Sn/3.8Ag/0.7Cu solder paste.

ASSEMBLY

Stencil Printing

Solder paste was deposited by printing through a 5 mil thick laser cut stencil using a 250 mm metal squeegee angled at 60°. The quality of the print deposits was assessed by visual inspection using an optical microscope after every print. Four different aperture designs were considered for each package. Not surprisingly, the transfer efficiency varied with the ratio between the exposed PCB surface area and that of the aperture sidewalls in the usual fashion. Extensive clogging was observed in a number of cases, notably for three out of the four designs tried for package A which lead to insufficient paste deposition. As we shall see later, this had significant consequences, not only in terms of the risk of opens but also for the assembly reliability.

Two different designs were considered for the thermal pads on the PCB under packages A and B (see Figure 4): one with 25 thermal vias and one with four separated heat lands, respectively. Ideally, the die paddles should be soldered to these pads without significant voiding, but it may not be possible to eliminate voids completely because of the presence of the thermal vias and/or the large size of the thermal pad [14]. In addition, outgassing during reflow may cause solder balling especially if the solder paste coverage is large. Amkor recommends the use of multiple smaller stencil apertures instead of one big opening for printing on the thermal pads [14]. In the present work, however, we employed the simpler patterns showed in Figure 3. This did indeed lead to imperfect filling of the thermal vias as indicated by the X-ray images in Figure 5 and the cross section in Figure 6, but such details should have little or no effect on thermal cycling results.

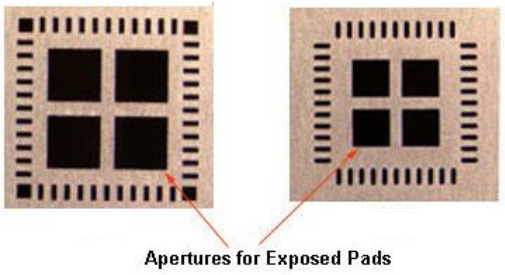

Figure 3: Stencil Aperture For Exposed Die Paddle [4]

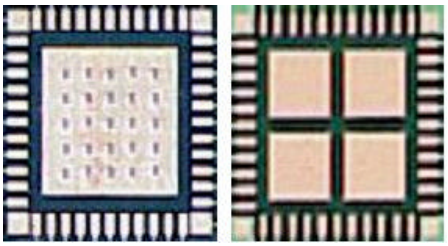

Figure 4: Heat Land Designs on PCB (Left – Heat Lands with Thermal Vias, Right – Four Heat Land Design) [2, 4]

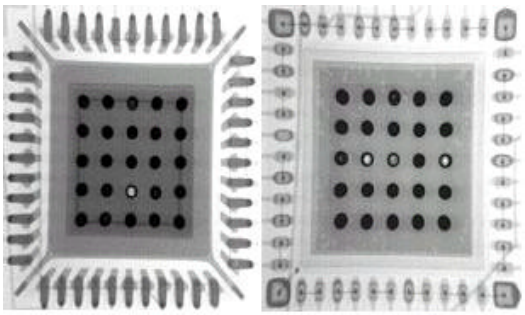

Figure 5: X-ray Image of Unfilled Thermal Vias on Package B (left) and Package A (right) [5]

Figure 6: Cross-section of Unfilled Thermal Vias [5]

Component Placement

A four spindle flex head General Surface Mount (GSM) placement machine was used for component placement. Components were supplied to the GSM in matrix trays and a placement force of 150 grams was used for placement.

Vision problems were encountered during component placement. This is because many leadless packages have poor contrast between the pad features and package background [11]. This reduces the ability of the vision system to distinguish between the features that have been assigned for the component recognition. Moreover, some of the leadless packages use a non-functional corner pad at 45° orientation [10]. These non-functional pads can be mistaken by the vision systems to be "pin 1" [10]. Leadless packages may also utilize unusually shaped corner pads whose geometry may not be recognized by the placement machines (see Figure 7) [10, 11].

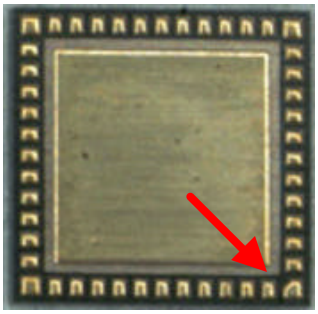

Figure 7: Leadless CSP with Odd Shaped Corner Pad

Reflow soldering

A previous study [6, 12] using a different no-Pb solder paste revealed higher assembly standoffs after reflow in air than after reflow in a nitrogen atmosphere, reflecting an incomplete collapse of the solder in the former. Also, reflow in air caused significant solder balling, an effect that was eliminated by reflow in nitrogen (see Figure 8).

In the present study assemblies were reflown in a nitrogen atmosphere with less than 50 ppm oxygen in a 10 zone forced convection oven. The peak reflow temperature was relatively high at 250°C reflecting likely temperatures for the present components in a mass reflow with other, heavier ones. Time above liquidus was 54 seconds.

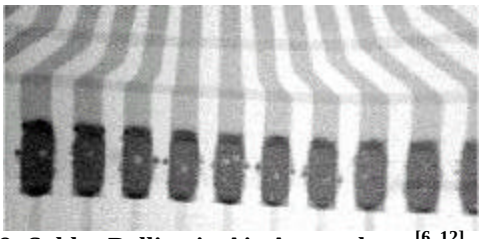

Figure 8: Solder Balling in Air Atmosphere [6, 12]

POST ASSEMBLY INSPECTION

Solder voiding

Voiding is not always critical in area array assembly, but in the present case it appeared to be. Leadless packages are generally susceptible to solder voiding, and significant voiding was indeed observed for all the packages. However, particularly extensive voiding was observed in package D assemblies. Figure 9 shows front and side cross-sectional views of typical joints, and Figure 10 shows an X-ray image of joints in a package D assembly.

In general, the solder voiding in a leadless package assembly is the result of a combination of factors [1, 2, 4, 5, 6, 12]:

- The low standoff height which does not allow the voids to escape from open surfaces, instead entrapping them in the solder joint;
- The coating on the lead finish which may contribute to the outgassing leading to void formation; and
- The shape of the terminations.

Figure 9: Solder Voiding in Package D Assembly – Left: Front Cross-sectional View, Right: Side Cross-sectional View [5]

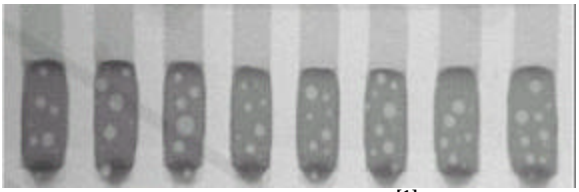

Figure 10: X-ray Image of Package D [1]

Various numbers of solder joints were cross-sectioned for the different packages, and the solder joint and solder void areas were measured. Table 2 lists the average solder joint areas, the largest void areas and the average void areas for each.

Table 2: Solder Voiding in Different Packages [5]

Pkg Code	Total Joint Area	Max Void Area	Avg. Void Area	Standoff
A	49.0	28.1	3.0	< 1.0
B	47.0	9.8	3.0	2.0
C	90.7	1.2	1.0	2.5
D	51.4	22.4	9.6	1.5

All dimensions in mils

Three of the packages have essentially the same joint area, while package C has considerably larger joints, as well as the largest standoff. The largest void area is seen to increase systematically with decreasing standoff across the four packages. As far as the average size of a void is concerned the effect is perhaps less obvious, but the largest standoff (package C) clearly leads to much smaller voids. Not surprising, there was also a clear effect of solder volume on the shapes and percentage of voids. Figure 11 shows a cross-sectional image of a joint resulting from insufficient solder deposition on a package A site.

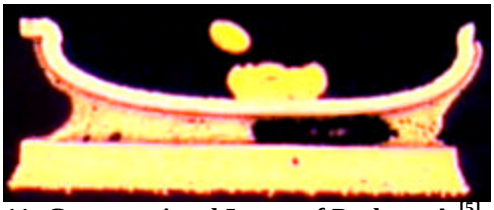

Figure 11: Cross-sectional Image of Package A [5]

Standoff Measurements & Cross-sectional Analysis

Figure 12 shows a cross-sectional view of package B. All cross-sectioned assemblies showed good wetting and the typical standoff height was assessed at 2.0 – 2.5 mil. Moreover, good toe fillets were also found in these assemblies (refer Figure 13)

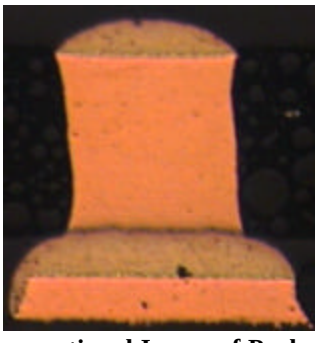

Figure 12: Cross-sectional Image of Package B [5]

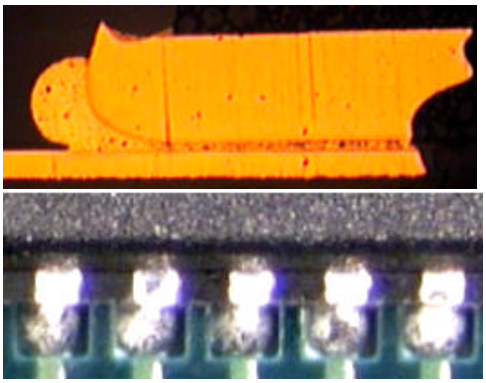

Figure 13: Toe Fillets on Package B Assemblies

Figure 14 shows a cross-sectional view of package A. Again, good wetting was observed. This was the only package with a metallized resin bump, rather than just a flat pad on the bottom. Together with a gap size essentially fixed by the solder between die paddle and PCB pad this lead to a minimum solder height of less than 1 mil. While this is not inherently a problem for reliability, (the resin presumably offers compliance and reduces thermal cycling stresses on the solder), it had a clear effect on voiding (see Table 2).

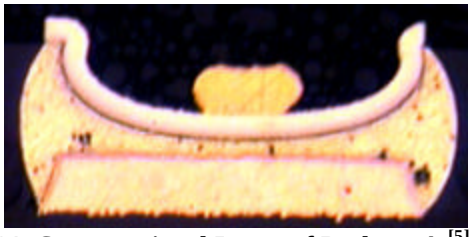

Figure 14: Cross-sectional Image of Package A [5]

Figure 15 shows a cross-sectional view of package C. Good wetting was again observed and the standoff was slightly larger (2.5 mil) than with package B.

Finally, Figure 9 shows a cross-sectional view of package D, for which smaller stencil apertures relative to the corresponding pad areas led to a smaller standoff height of about 1.5 mil.

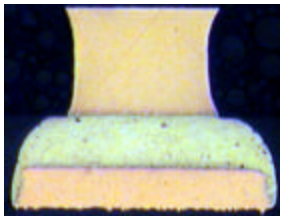

Figure 15: Cross-sectional Image of Package C [5]

In general, there were no significant differences between the standoffs for the same packages assembled to different PCB pad sizes [6. 12] because the stencil design always incorporated larger apertures for larger PCB pads.

RELIABILITY RESULTS

Each combination of package, substrate pad and solder mask design, and stencil aperture design was subjected to 0-100°C air-to-air thermal cycling with 5 minute ramps and 5 minute holds. Afterwards dye penetration tests were performed on 6 samples of each of the failed component types. Figure 16 indicates the frequency of completely cracked joints versus location within the solder joint arrays for packages D, B, and C. Packages B and D are seen to behave as expected, with the joints furthest from the package center (neutral point) being most susceptible to failure during thermal cycling. In the case of package C, however, failures appeared to be randomly located within the package footprint (see Figure 16) [7, 13]. Figure 17 shows three adjacent solder joints of package C subjected to dye penetration test. Solder fatigue is represented by red dye. Although the joints are located next to each other, the degree of fatigue is seen to vary considerably. The reasons for this are still under investigation.

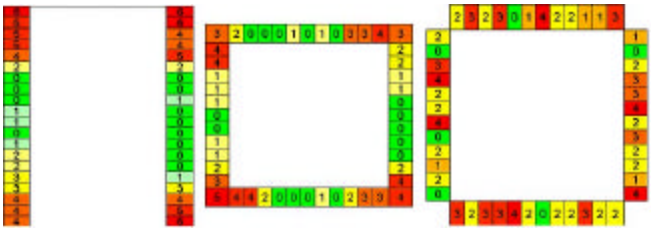

Figure 16: Dye Penetration Results for packages D, B and C [7, 13]

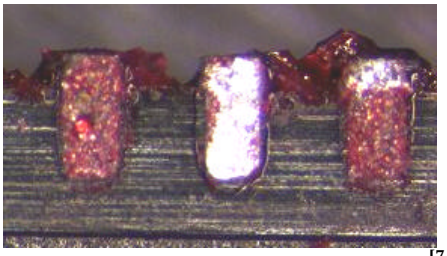

Figure 17: Dye Penetration Test on Package C [7, 13]

Once a significant number of failures were recorded, a Weibull distribution was produced and the slopes and characteristic lifetimes, N_{63}, of the assemblies were determined.

None of the package B assemblies failed through 5000 thermal cycles, presumably because of the lack of a Si die in the package. Soldering of the die paddle to the PCB is also expected to provide some stress relief for the solder joints along the edge, but the other package with a die paddle, package A, experienced many failures. In fact, package A failed earlier than the similarly sized package C which did not have an exposed die paddle.

The overall package performance indicates that the reliability of package C is superior to that of packages D and A. Package D demonstrated the lowest characteristic life. This is not surprising given that package D was the largest device, contained solder joints with the lowest standoff and with numerous voids.

The effects of pad and stencil size were evaluated for the three devices with failures. As expected, larger stencil apertures (greater transfer efficiencies) were shown to improve reliability. The results also indicate that an optimization of pad area and pad dimensions exists. In other words a long, thin pad may not produce the same reliability as a shorter, wider pad with an identical surface area. However, the pad variations studied were limited and prevent us from further comment. Overall, there seems to be little doubt that the reliability of the present leadless packages may be strongly affected by stencil design.

Packages A and C showed a systematic effect of stencil aperture and pad design. Larger apertures (greater transfer efficiency) combined with larger PCB pads clearly improved reliability. Sensitivity to aperture clogging and paste deposit insufficiency for package A has been previously discussed, and optimizing the aperture design (increasing the area ratio) and increasing the pad size resulted in an N_{63} increase from 1280 to 1962 cycles. The reliability improvement was attributed to slightly larger solder volumes, and more importantly, to the significant reduction in joint volume *scatter* invariably achieved by such optimization. In other words, there was a preferential elimination of the smallest joints with the most/largest voids. Further evidence of such is apparent when comparing the failure distributions provided by the Weibull slope. The Weibull slope indicates that the pad and stencil optimization was accompanied by a tightening of the failure distribution by a factor of about two, i.e. a preferential elimination (or delay) of the earliest failures (which are most often of practical concern).

A similar optimization had less effect for package C, which had a much larger standoff and thus fewer, smaller voids (Table 2). However, among the variables considered, an increase in N_{63} from 2063 to 2498 cycles appeared to be related to an increase in minimum pad width (and thus solder joint width and the crack length needed for failure) and/or stencil aperture transfer efficiency. Once again we emphasize that a moderate increase in the area ratio is generally known to affect the scatter in solder paste volume more than the average. As the increase in N_{63} was again accompanied by a systematic tightening of the failure distribution (70% increase in Weibull slope), it again seems most likely that the improvement is related to the preferential elimination of relatively small solder joint volumes with relatively large voids. This might also account for the apparent randomness of failure location observed for this component.

The results for Package D indicate a systematic dependence on pad size. The Package D N_{63} increased linearly (from 803 to 1193 cycles) with increasing pad area and thus solder joint cross section. However, in this case there is no indication of a dependence on minimum pad width (and

package C showed no correlation between N_{63} and pad area). On the other hand, the largest N_{63} again corresponded also to the tightest failure distribution and stencil apertures optimized to minimize the scatter in solder deposit volume.

CONCLUSIONS

Commercially available leadless CSPs were readily assembled onto high-T_g boards with Pb-free solder paste. Assembly reliability appeared quite sensitive to the proper optimization of the PCB pad and stencil aperture design, presumably through a minimization of the scatter in solder joint volume and voiding. It follows that further reduction in voiding through materials selection and process optimization may offer additional benefits.

In general, lifetimes in excess of 1000 cycles between 0^oC and 100^oC seem achievable with these packages on 62 mil thick boards. However, we caution that two assemblies involved low-level Pb contamination of the no-Pb solder joints. The effects of this are expected to depend on the relative volumes, reflow profile parameters and subsequent thermal history, as well as assembly mechanics and detailed accelerated test parameters. We are currently researching the mechanisms behind such dependencies, but at this point we would consider it very risky to extrapolate our results to very different test conditions or 'life in service'.

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