Low ESL / 7343 Package

In the quest for lower ESL devices, having the ESL reduced in the package is only half of the battle; connecting that device to the circuit determines how much of that low ESL appears to the circuit. For this low ESL part type, it would be a shame to take a part of 200 pH and add 2000 pH to its ESL because of via patterns on the PCB.

There are several proposed methods that might be employed to secure a low ESL to the circuit. The first proposal would allow for the vias to be covered by the solder mask, and located as close to the perimeter of the pad attach areas as possible.

The solder pads were created to mirror the initial Sanyo TPL[1] termination pads. This is a three-terminal presentation for a two-terminal, 7343 component. The proposed solder pads in Figure 1, show three pads with the pad on the left connected to the anode elements of the device. The middle and right pad are both cathode contacts, connecting a singular leadframe element in the package. The key to the low inductance is the small gap between the anode and cathode plates (in Figure 1, the middle and far right solder pads are both cathode contacts, while the far left pad is the anode contact).

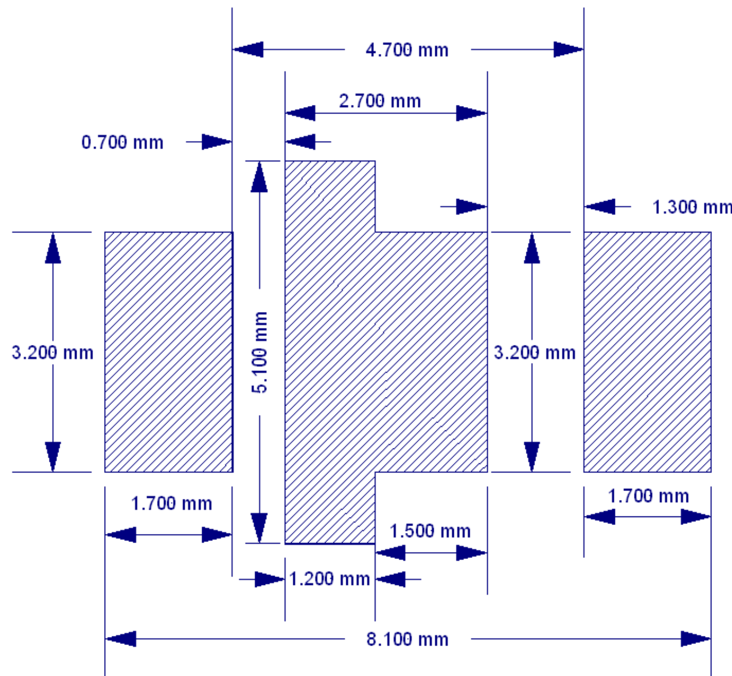

Figure 1. Initial solder pads proposed for facedown 7343.

Splitting the cathode contact into two smaller pads eliminates a huge disparity in pad areas creating a configuration which could lead to solder lifting the chip beneath the cathode and breaking the anode contact.) The Sanyo TPL device uses three termination pads and the subsequent mirrored solder pads that guides the cathode solder pads to be similarly split, but this three-terminal design was patented by Sanyo. Since the primary consideration for this three-pad termination was to break the solder pad area of the cathode, the KEMET T528 7343 design uses only two termina-

tion pads with a very large cathode plate which spans both cathode solder pads. This allows this design to work with the Sanyo pad layout, but we need to emphasize that the recommended solder pad recommendation is the same – preventing a very large singular cathode solder pad which could lead to lift.

Initial 16 Via Layout

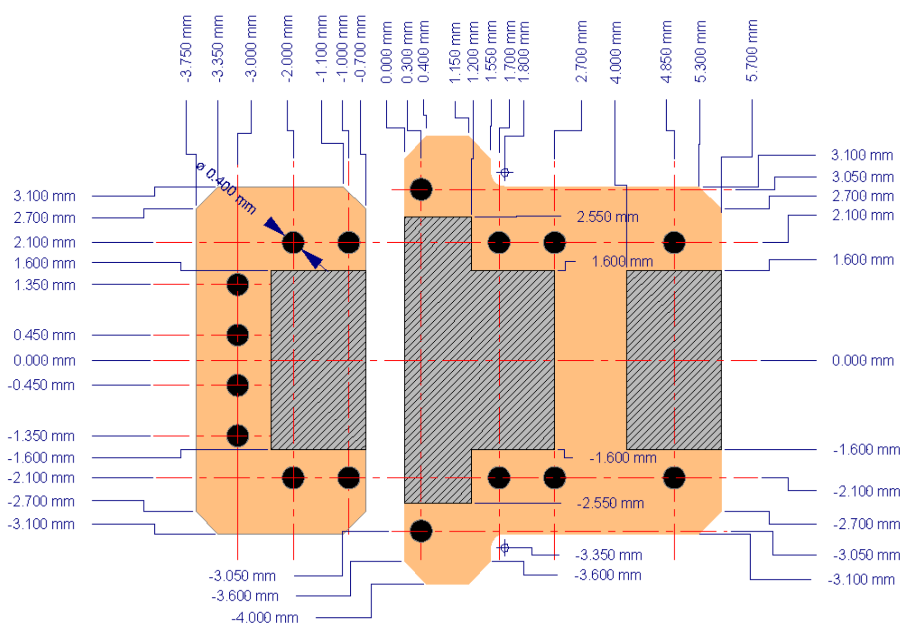

Figure 2. Initial copper, soldered pad, and via structure.

In Figure 2, the copper, solder pads and vias are located to create the acceptable solder pads as in Figure 1. The copper is shown without a solder mask, but this region would be covered with a solder mask. The solder mask was left off to show once again that the two cathode plates are really one contact for the capacitor. These capacitors are two-terminal devices, and the two cathode plates and pads are of the same polarity and voltage levels. The total via count is 16, evenly split with 8 vias for the anode and 8 vias for the cathode. The high frequency current path will concentrate to the smallest loop path or those opposite polarity vias closest to each other. As the vias move away from the anode-cathode separation, they lessen their impact on ESL and ESR, but remain as contributors to the thermal conduction and therefore the power or ripple capability for the device.

The problem is that this layout does not bring multiple positive and negative vias close to each other to create some inductive cancellation. There are no vias in the gap between the anode and cathode plates, eliminating the shortest (lowest inductance) path possible. This created a significant improvement from the standard two-terminal 7343 tantalum chips, but it was short-sighted in optimizing the best possible layout.

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Shortening the path loop – 1st Iteration

Initial attempts to improve the pad geometry were to concentrate the vias along the anode-cathode separation. This was accomplished by creating the 18 vias in the solder pad areas, along the separations edge for the anode and cathode pads. Another row of 9 vias were created in the “secondary” cathode contact to assist in the heat dissipation or ripple current capability of this device (over 90% of thermal dissipation is conducted and the heat source is the tantalum pellet). These secondary cathode vias are duplicated in some manner in all subsequent proposals.

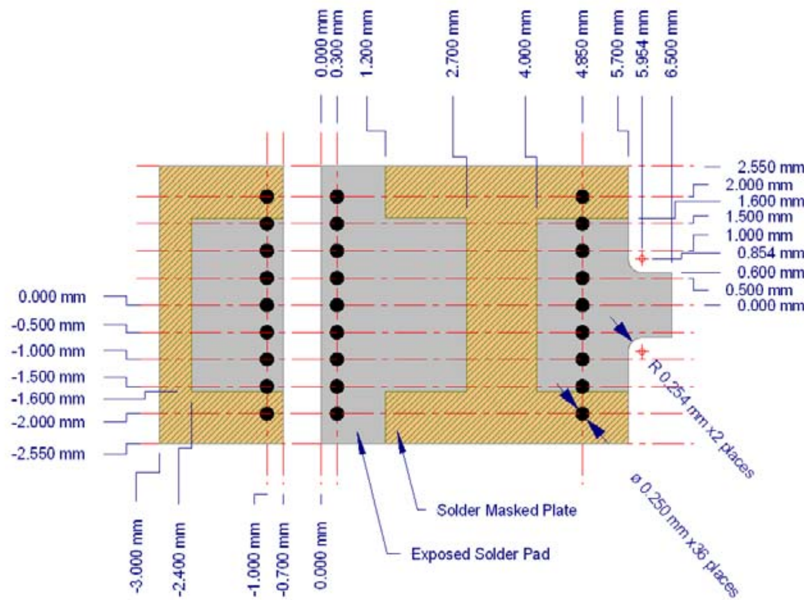

Figure 3. Crowding vias along anode-cathode interface region.

Most designers objected to using vias in the solder pad regions as these vias could draw in excessive amounts of solder, and they requested that we move these structures to the masked copper areas.

This design does increase the total via count to 27, with the 18 located nearest the anode-cathode separation sharing the optimum current path affecting ESL and ESR, although their absence from the open barrier between the anode-cathode separation adds to the current loop-path. Utilizing this area for the vias could shorten the path and reduce ESL/ESR. The 9 vias in the cathode solder pad furthest from the separation add to the thermal conduction for the device.

Interdigitated Vias – 1st Proposal

The vias in Figure 3 are crowded along the separation region, but by keeping them out of this region they are too far apart to maximize inductive cancellation effects. By moving these vias into the separation region, they can be placed close enough to create some cancellation effects, and since they are in the separation region, the vias are covered with solder mask, protecting them from pulling in excessive solder from the pad regions. Because considerations for via diameter, conductive flair from the hole outward, and isolative separation between opposite polarity vias, the tight grouping from Figure 3 could not be used. The rule used by most designers is the "10-20-30" mil rule, or the diameter must be at least 10 mils in diameter, the conductive ring outside the via must extend to a diameter of at least 20 mils from the via's center (establishing a radius or minimum of 5 mils copper along the edge of the via), and the separation between this contact and any other contact must extend to at least 30 mils from the via's center (5 mils radius or minimum separation between adjacent, non-common electrical connections).

Rectangular tabs alternatively extending from the anode and cathode solder pad copper into this separation would be the simplest method, but this would create a dramatically reduce number of vias in this region. Optimum placement required a serpentine separation pattern as shown in Figure 4. The separation is actually 5.5 mils, and this creates 8 inductive cancelling pairs of opposite polarity vias within this region or 9 vias. There are a total of 35 vias in this layout with 12 connected to the anode and 23 connected to the cathode.

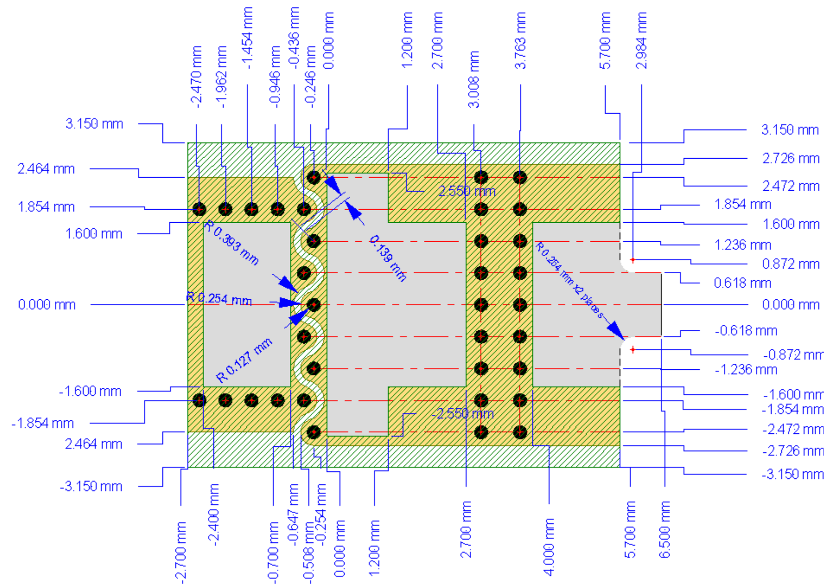

Figure 4. Vias interdigitated in separation region, mask covered – 5.5 mil isolation in anode-cathode separation.

We were requested to increase the separation to about 0.180 mm and this leads us to our 1st proposal as in Figure 5.

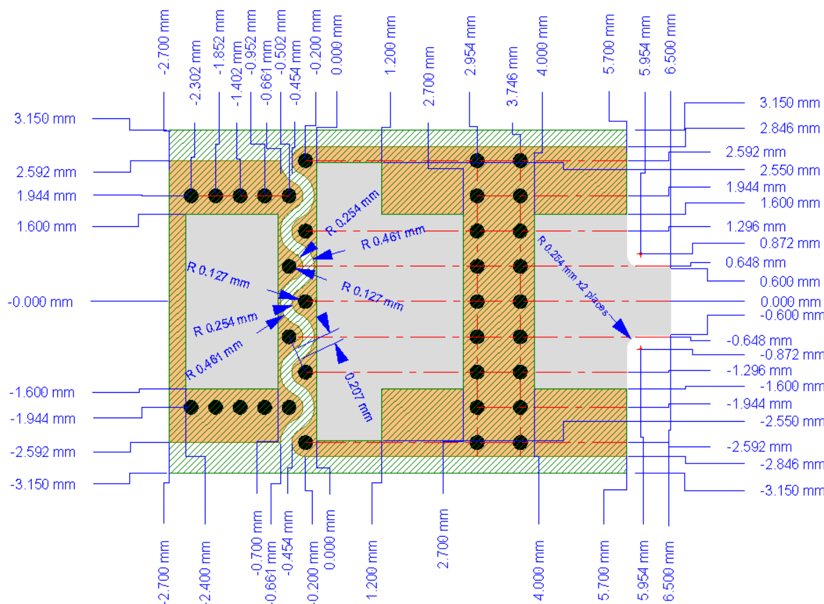

Figure 5. Vias interdigitated with 10-20-36 mil applied – 8 mil gap.

Here we applied a 10-20-36 mil rule and were able to achieve a 0.207 mm separation. The via count and anode-cathode distribution remains the same although the distance between opposite polarity vias in the anode-cathode region was increased to allow a greater isolation gap.

Interdigitated Vias – 2nd Proposal

Some engineers wanted simplification. They believe that a few vias connected in an interdigitated fashion will be sufficient to optimize the performance of these devices for their applications and they used the rectangular tab extensions as a center point for the vias..

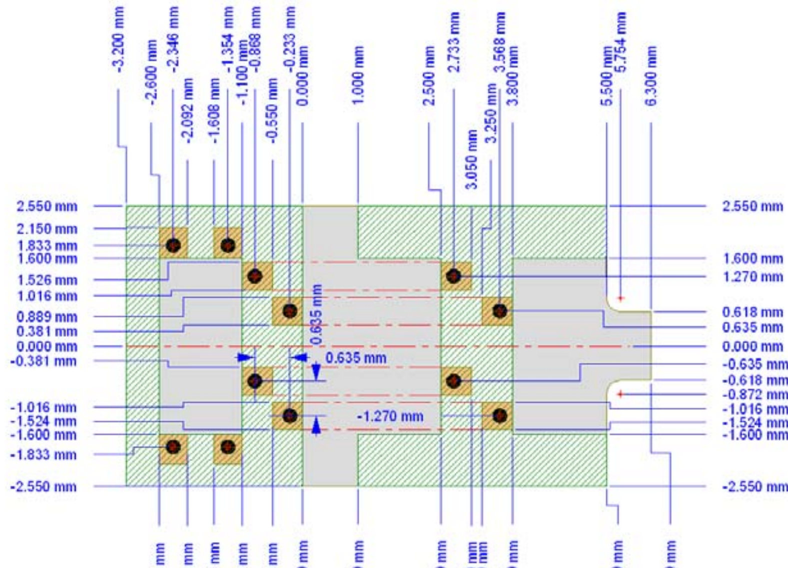

Figure 6. Simpler interdigitated with 12 vias, mask covered.

In Figure 6, there are only 12 vias created with only two pairs creating some inductive cancellation in the separation region between the anode and cathode plates. The solderable plates in this design are the different from the initial layout shown in Figure 1. The separation was increased in this layout from 0.70 mm as shown in all previous layouts, to 1.10 mm. This conforms to the termination areas beneath the chip as that separation between the anode and cathode on the chip are 1.1 mm. In this design, it was required by the engineer that the vias' centers be separated by 25 mil (0.635 mm) in both horizontal and vertical axis (or 35 mil., 0.898 mm, center-to-center). Even with this change we could not maintain the 5 mil unencumbered copper radius entirely around the vias as the gap between the via's edge and the solderable surface is reduced to 4 mils. If the separation was maintained at 0.70 mm, this would have required part of the vias to exist within the solderable area.

Conclusions

The best method of reducing the inductive impact of the vias connection the low ESL device to the board is with as many interdigitated vias in the separation region (between the anode and middle cathode solder pads) as possible. This does introduce complexity to the design and the openings in the plates in layers beneath this may impact the high current feeds around these multiple vias.

The purpose in creating this document was to offer some direction for the designers to optimize the layouts, especially via locations to allow their circuit to utilize the low ESL of the package without adding excessive ESL in the circuit connection to that device. Variations of these layouts are welcome as they are intended as suggested methods to optimize the performance of the low ESL component.

References

[1] Sanyo Poscap Capacitors, SANYO Electric Co., Ltd., Oct. 2004, p. 13.

John Prymak – Director Advanced Applications
Erik Reed – Director Advanced Testing
Allen Mayar – Director Strategic Marketing