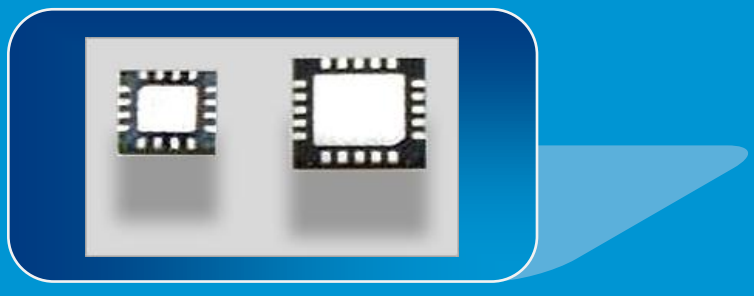
PRINTING AND ASSEMBLY CHALLENGES FOR QUAD FLAT NO-LEAD (QFN) PACKAGES

With proper stencil design, stencil technology selection, and PCB solder mask layout the challenges that QFNs present to the assembly process can be overcome.



By William E. Coleman Ph.D.,

Vice President Technology

PHOTO STENCIL

PHOTO STENCIL

Colorado Springs, CO 80919
Phone: (719) 599-4305
Fax: (719) 599-4334
www.photostencil.com

Printing and Assembly Challenges for Quad Flat No-Lead (QFN) Packages

By William E. Coleman Ph.D.,

Photo Stencil, Vice President Technology

Benefits and Challenges

QFN (quad flatpack, no leads) and DFN (dual flatpack, no lead) are becoming more popular in new component releases. Their very small form factor allows smaller packages, better grounding, and better heat sink thermal properties compared to other SMT packages.

Most QFNs have a metal pad on the underside of the part for grounding and heat conduction. DFNs have a similar center metal pad but have leads on only two sides. Typical thickness of the QFN devices is .85mm and the body range from 3mm up to 12mm, so the packages are very small and very light. The QFN leads and ground plane conductor are flat and in the same plane on the bottom of the package. Printing solder paste 1-1 with the ground plane can cause the QFN to float during reflow, thus miss-registering the leads on the QFN and the pads on the PCB. QFN float can be controlled by reducing the amount of solder paste printed on the ground plane. Typically a 50 to 60% reduction will solve the QFN float problem. However the aperture reduction must be done judicially. A Window Pane aperture is recommended for most cases. This allows the solder paste volatiles to easily escape during reflow without moving the QFN device. Figure 1 shows the benefits of window pane apertures for the ground plane.

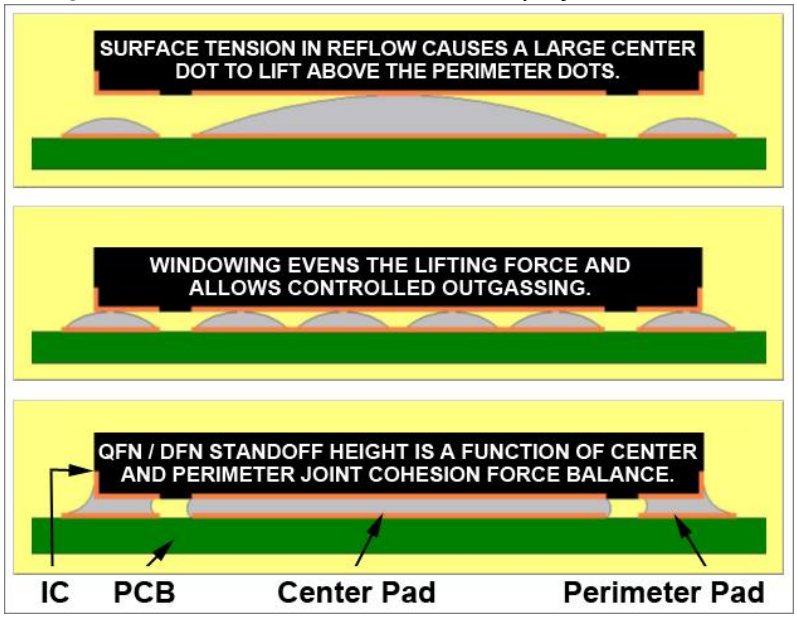


Figure 1. Benefit of Window Pane Ground Plane Apertures

The next challenge is the actual aperture size in the stencil. **Figure 2 shows a 3mm QFN and a 4mm QFN device.** Typical aperture widths as low as .175mm and aperture lengths as low as .4mm present a challenge to the printing process as far as percent paste transfer. The other challenge is the solder mask employed on the PCB.

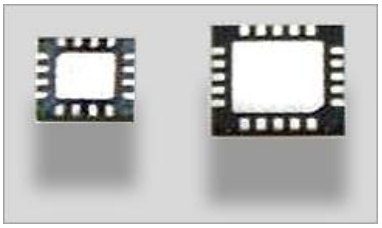


PHOTO STENCIL
Colorado Springs, CO 80919
Phone: (719) 599-4305
Fax: (719) 599-4334
www.photostencil.com

There are three types of solder mask designs which are shown in Figure 3: a) SMD where the pad opening on the board is defined by the solder mask, b) NSMD where the pad itself defines the boundary of the pad and the solder mask is pulled back off the pad (typically .05 to .075mm per side), and c) NSMD – Window. In the last case there is no solder mask between pads so bridging between pads is more likely than with solder mask between pads.

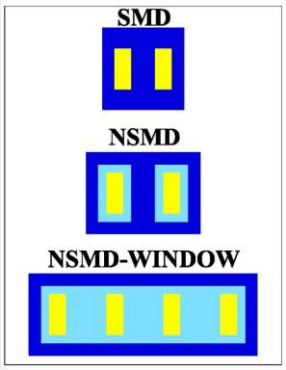


Figure 3. Solder Mask Designs

It should be noted that the recommended length of the pad on the PCB compared to the length of the lead on the QFN is .2mm larger. As seen the Area Ratio for a .125mm thick stencil is >.66 for all the examples listed. Aperture size for the SMD is .05mm smaller than the PCB pad. There are typically two reasons for this reduction. If the stencil is slightly misaligned to the PCB, paste could be printed on the solder mask. Also there might be high stress points if solder contacts the mask. The reduction in aperture size has reduced the Area Ratio making paste transfer more difficult. For Area Ratios below .66 Electroform stencils or Nano-Coated stencils are normally recommended. The final example in Table 1 is the NSMD–Window. The pitch is .4mm leaving little room to put solder mask between pads on the PCB. Aperture size is also small giving a challenging Area Ratio for .125mm thick stencils; therefore .100mm thick stencils are normally recommended to provide a more robust stencil printing process window.

Stencil and PCB Design Considerations

Table 1 shows stencil design guidelines for the three solder mask cases. This table shows the package size, the lead pitch, the number of I/O, the package lead dimensions, the recommended PCB pad dimensions, the recommended stencil aperture dimension, recommended stencil thickness, and resulting Area Ratio. For NSMD the stencil aperture is 1-1 with the PCB pad dimension.

Stencil Design for Typical QFN Apertures (NSMD)

Package	Pitch	I/O	Package Lead Width	Package Lead Length	PCB	PCB	Aperture NSMD	Aperture NSMD	Stencil Thickness	Area Ratio
3mm	.5mm	12	.23mm	.55mm	.23mm	.75mm	.23mm	.75mm	.125mm	0.70
4mm	.5mm	20	.25mm	.40mm	.25mm	.60mm	.25mm	.60mm	.125mm	0.71
7mm	.5mm	44	.25mm	.55mm	.25mm	.75mm	.25mm	.75mm	.125mm	0.75
10mm	.5mm	72	.23mm	.40mm	.25mm	.60mm	.25mm	.60mm	.125mm	0.71
12mm	.5mm	80	.25mm	.55mm	.25mm	.75mm	.25mm	.75mm	.125mm	0.75

Stencil Design for Typical QFN Apertures (SMD)

Package	Pitch	I/O	Package Lead Width	Package Lead Length	PCB	PCB	Aperture SMD	Aperture SMD	Stencil Thickness	Area Ratio
3mm	.5mm	12	.23mm	.55mm	.23mm	.75mm	.18mm	.70mm	.125mm	0.57
4mm	.5mm	20	.25mm	.40mm	.25mm	.60mm	.20mm	.55mm	.125mm	0.59
7mm	.5mm	44	.25mm	.55mm	.25mm	.75mm	.20mm	.70mm	.125mm	0.62
10mm	.5mm	72	.23mm	.40mm	.25mm	.60mm	.18mm	.55mm	.125mm	0.54
12mm	.5mm	80	.25mm	.55mm	.25mm	.75mm	.20mm	.70mm	.125mm	0.62

Stencil Design for Typical QFN Apertures (NSMD window)

Package	Pitch	I/O	Package Lead Width	Package Lead Length	PCB	PCB	Aperture SMD	Aperture SMD	Stencil Thickness	Area Ratio
4mm	.4mm	32	.175mm	.45mm	.175mm	.610mm	.175mm	.560mm	.125mm	0.53
4mm	.4mm	32	.175mm	.45mm	.175mm	.610mm	.175mm	.560mm	.100mm	0.67

Table 1. QFN, PCB, Stencil Design Guidelines

Colorado Springs, CO 80919
Phone: (719) 599-4305
Fax: (719) 599-4334
www.photostencil.com

Another problem arises when using a NSMD window when the solder mask is higher than the pad on the PCB. In this case the solder paste is extruded through the stencil since the stencil is not in contact with the PCB pads during printing. This extruded paste will make contact with the bottom side of the stencil causing potential bridging during successive prints since there is no solder mask between neighboring pads. Stencil wiping after every print may help reduce this problem. An Example of a NSMD – Window PCB with solder mask above the height of the PCB pads is shown in Figure 4.

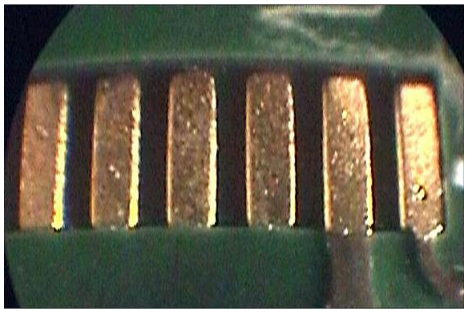


Figure 4. NSMD-Window with Mask to pad gap of .03mm

One possible solution suggested by a customer[1] is a PCB side step stencil as shown in Figure 5. This is an Electroform stencil which is .08mm thick everywhere except in the QFN area inside the solder mask where it is .01mm thick. In this case the mask opening was of the order of .125mm per side except on the ends of the pad rows where it was less. There are several limitations to this approach. Namely the spacing between the step and the solder mask is extremely small allowing for little miss-registration. Also the stencil is thinner for all other components except the QFNs which may yield insufficient paste. The first limitation could be addressed at the PCB design level by making the mask to pad clearance much larger; of the order of .25mm per side as well as leaving the ground plane without any solder mask surrounding.

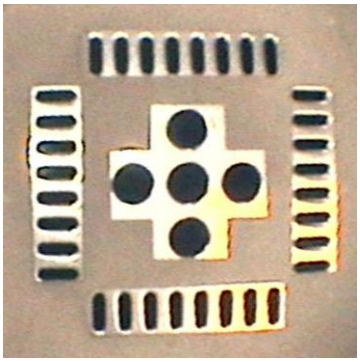


Figure 5. Step Electroform Stencil on PCB side - .1mm thick around QFN apertures and .08mm elsewhere for all other apertures.

Another possible solution is a single level stencil without step but with Nano-Coating on the aperture walls as well as on the bottom side (PCB side) of the stencil. Nano-Coatings have a property called fluxophobicity. Quite simply it is the stencils ability to resist the spread of flux on its surface. It is measured in the form of the 'Flux Contact Angle'. This is the angle that the flux will form when a drop is placed on the surface of the stencil. Nano coating not only increases the paste ability to release form the apertures but also to resist spreading on the bottom side of the stencil when the paste is extruded into a cavity created by the NSMD- Window. This property not only eliminates the need for frequent under board wiping but also reduces the occurrence for pad to pad bridging.

QFN Repair

The first step to repair a defective QFN device is to remove the defective device from the PCB and clean the excess solder from the PCB pads. Solder paste is then

Colorado Springs, CO 80919
Phone: (719) 599-4305
Fax: (719) 599-4334
www.photostencil.com

printed either on the PCB or on the bottom of the QFN prior to placing the QFN on the PCB and locally heating to reflow the solder paste and solder the device in place. Mini stencils are normally used to print paste on the PCB. This can be a difficult and tedious task for very small QFN devices ranging in size from 3mm up to 12mm. Printing solder paste directly onto the QFN device is a more popular approach[2].

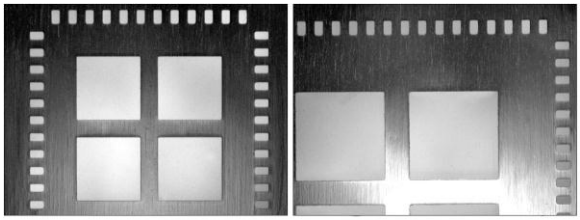


Figure 6 QFN Repair stencil with window pane ground plane apertures

Figure 6 shows a repair stencil that fits into a holding tool which also holds the QFN in registration to this stencil. The top portion of a 7mm / 48 I/O .5mm pitch repair stencil and the top portion of a 10 mm / 72 I/O .5mm pitch repair stencil are shown. Note that the aperture area for the ground plane is reduced by approximately 50% by the window pane technique. Figure 7 shows paste printed on QFN pads using the tool that holds both the stencil and the QFN device. Figure 8 shows paste on the same QFN. After paste is applied the QFN is placed on the PCB and locally reflowed.

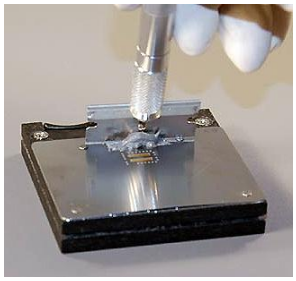


Fig 7. Printing Solder Paste on QFN device while in holding tool

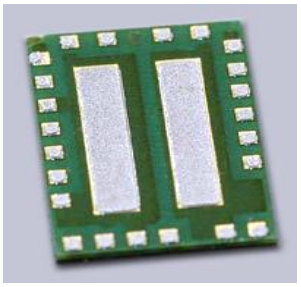


Figure 8 Solder paste printed on QFN before placement on PCB for rework

Conclusion

Although QFN devices present a challenge to the SMT assembly process with proper stencil design, proper stencil technology selection (Laser stencils, Electroform stencils, Nano-Coat stencils), and proper PCB solder mask layout these challenges can be overcome. The most popular QFN repair seems to be to print solder paste directly onto the QFN leads and ground plane.

References:

1. Private communication with Greg Kloiber, Manufacturing Engineer Plexus Corp.
2. "BGA and QFN Repair Process" William E. Coleman, APEX 2008

General QFN References:

1. "Rule of thumb guide for Practical DFN/QFN Printed Circuit Board and stencil Design" James R. Staley, Linear Technology application note
2. "PCB Land Pattern Design and Surface Mount guidelines for QFN Packages", Intersil Technical Brief TB389.6
3. "QFN Layout Guideline", Texas Instruments Application Report SLOA122
4. "Quad-flat no-leads package (QFN)" Wikipedia for other variants and manufacturer names.

Colorado Springs, CO 80919
Phone: (719) 599-4305
Fax: (719) 599-4334
www.photostencil.com

About the Author:

For nearly 30 years, Dr. Coleman has been providing his experience and knowledge to the electronic interconnect industry. Among his contributions, he was instrumental in establishing the standard IPC 7525 Stencil Design Guidelines. He is a 2-time winner of IPC's Committee Service Award and received the prestigious IPC President's Award for 2012. Coleman has numerous patents under his name and serves on university and industry boards of directors. He received a PhD in physics from West Virginia University. Some of the technical papers written by Coleman can be found on the Photo Stencil website at www.photostencil.com.