

## Assembly and Rework of Lead Free Package on Package Technology

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### Abstract:

Miniaturization continues to be a driving force in both integrated circuit packaging and printed circuit board laminate technology. In addition to decreasing component pitch (lead to lead spacing), utilization of the vertical space by stacking packages has found wide acceptance by both designers and manufactures of electronics alike. Lead free Package on Package (PoP) technology represents one of the latest advancements in vertical electronics packaging integration and has become the preferred technology for mobile hand held electronics applications. TT Electronics in Perry, Ohio has developed the capability to assemble and rework numerous “state of the art” packaging technologies. This paper will focus on the essential engineering development activities performed to demonstrate TT Electronics’ ability to both assemble and rework PoP components.

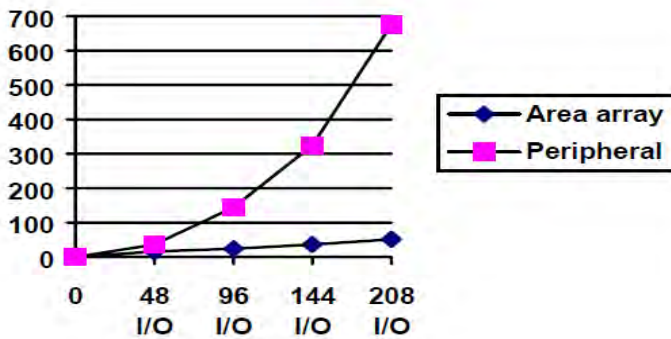
### Background:

For many years the peripherally leaded packages were at the forefront of electronic packaging technology. In those days the main purpose of integrated circuit (IC) packaging was to protect the device inside from environmentally induced corrosion, provide mechanical protection, and provide an electrical path to the printed circuit board. This strategy proved effective until ever increasing lead counts made the peripherally leaded package impractical. The introduction of area array packaging technology solved this problem. In today’s area array packaging the leads are distributed across the entire surface of the package in a rectangular array fashion (Figure 1). Thus, a larger I/O count can be accommodated in a smaller area package. In fact the area required for a peripherally leaded package increases exponentially with lead count while the area array package shows a linear dependence (Figure 2).

In recent years the stacked packaging structure has found acceptance in the mobile hand held electronic market. By combining logic and memory chips into the same stacked package, designers can fit more function into a smaller and lighter form. The two predominant forms of stacked packaging structures are: the stacked die structure and the Package on Package structure (Figure 3).<sup>1</sup>



**Figure 1.** Illustrates the difference between QFP and BGA packages, showing an ultra fine-pitch 160 lead QFP (pitch 0.3 mm) on a background consisting of the bottom side of a 1.5 mm pitch PBGA with 225 interconnection solder balls. From this picture it is easy to understand the popularity this BGA package has received among the people in the assembly business. Note that there are five QFP leads for every BGA solder sphere.

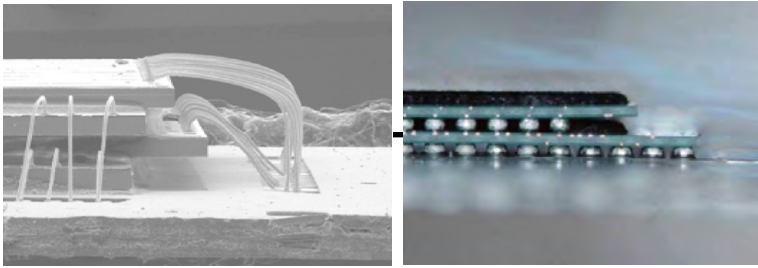


**Figure 2.** Peripherally led packages consume area at an exponential rate when compared to area array packages and the same pin count and lead pitch (0.5mm pitch shown).

The most obvious benefit of both PoP and the stacked-die structure is space savings; however, some other key differences make the PoP package the preferred embodiment. The main benefit of PoP structure is that the memory is decoupled from the logic device. Therefore:

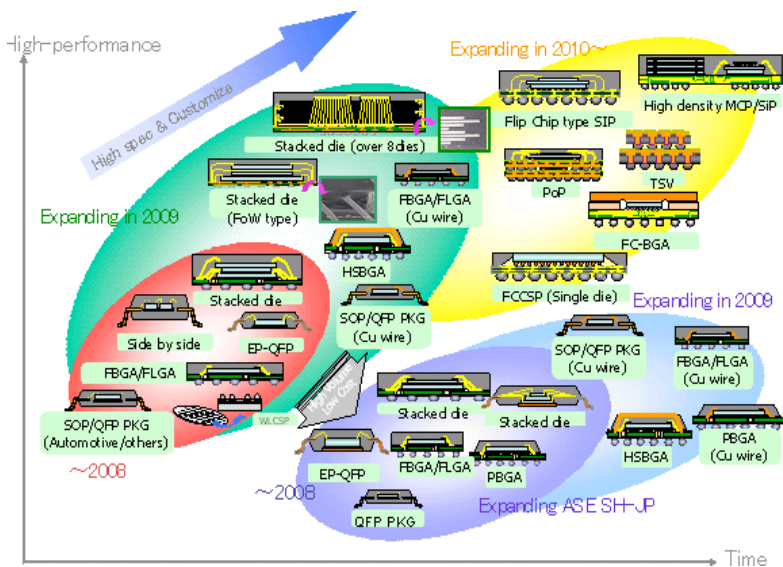
1. The memory package can be tested separately from the logic package.
2. Only "known good" packages are used in the final assembly. Compare this to the stacked-die package where the entire package is thrown away if either the memory or logic is defective.
3. The end user controls the logistics. This means that the memory can be treated as a commodity item and sourced from multiple suppliers.
4. Any mechanically mating top package can be used. Therefore for a low-end phone, a smaller memory package can be used on the top package. For a high-end phone, more memory could be used with the same package.
5. Because memory only comes into play during final assembly, there is no need for logic suppliers to source memory.

Electrically, PoP offers benefits by minimizing track length between logic components and memory. This results in better performance of the devices since the shorter routing of interconnections between circuit's results in faster signal propagation and reduction in "cross-talk" noise.



**Figure 3.** The Stacked-die structure (Left image) versus the Package on Package structure (Right image).

TT Electronics has invested significant financial as well as engineering resources into the development of "best in class" assembly capability thus, aligning our assembly platform with the latest integrated circuit packaging technologies as well as those to come in the foreseeable future (Figure 4). Package on Package technology represents one of the latest in trends in IC packaging. The use of PoP packaging technologies increases assembly complexity. To offset this added complexity printed circuit board (PCB) assemblers must employ improved techniques of assembly and rework.



**Figure 4.** Trends in Integrated Circuit packaging 2009 courtesy of The Advanced Semiconductor Engineering Group of Japan.

### Test Vehicle and Components:

The test vehicle used for this evaluation was a commercially available board with space for 15 PoP placements (Figure 5). The board size was 132mm x 77mm and 1.0mm thick. Two different surface finishes were selected for this evaluation. Two different PCB surface finishes were investigated: ENIG (Electro less Gold Immersion Nickel) and OSP (Organic Solder Preservative). 2, 3



Figure 5. Package-on-package test vehicle.

The pads on the test vehicles and the components are “daisy chained” together. There are a total of three networks for each populated location (Figure 6); one network for the entire bottom, one network for 3 leads located at each corner of the top package, and one network for the remainder of the leads on the top package.

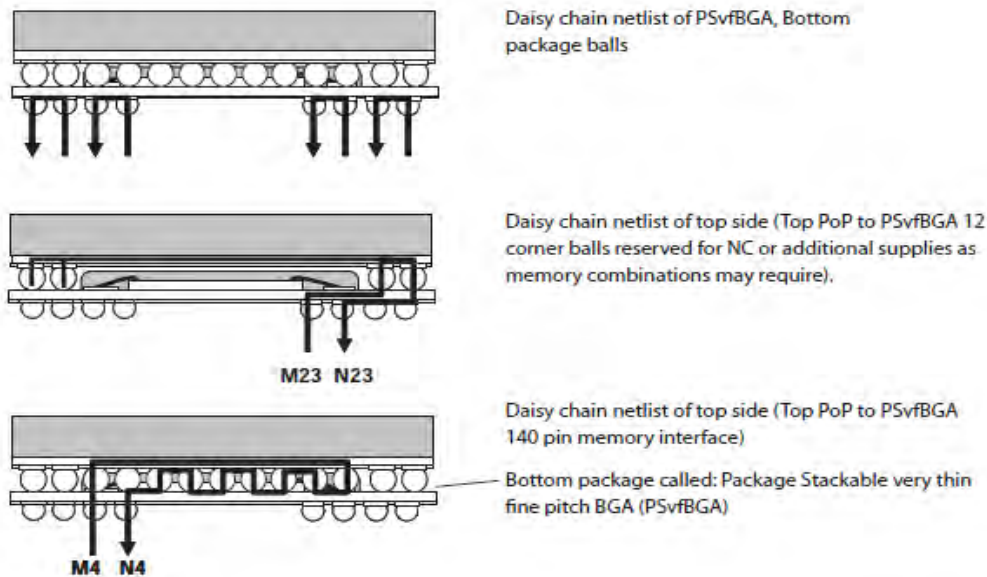
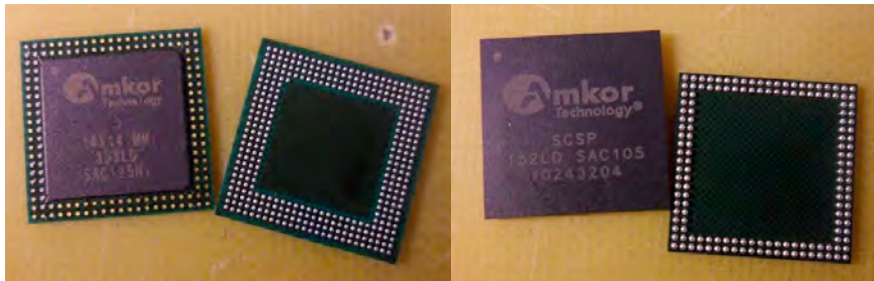


Figure 6. Electrical diagram of the three daisy chained network on each of the 15 sites of the Test Vehicle.



The Package on Package components selected for our initial experiments were 14mm x 14mm. The bottom package had a 4 row peripheral array of solder balls with 353 I/O on a 0.50mm pitch (Figure 7). The top package had a 2 row peripheral array with 152 I/O on a 0.65mm pitch (Figure 8). The solder ball alloy for the top package and bottom package were SAC105 (Sn98.5/Ag1.0/Cu0.5) and SAC125 (Sn98.3/Ag1.2/Cu0.5) respectively.



**Figure 7.** Bottom module.

**Figure 8.** Bottom module.

#### Package on Package Assembly Considerations:

The main goal of the PCB assembly test matrix was to determine the impact of several key assembly variables on final assembly yield. An extensive literature search as well as discussions with the manufactures of PoP components and assembly material suppliers led to the following PCB assembly matrix (Table 1):

- Evaluation of the impact of two PCB surface finish options ENIG versus OSP on final assembly yield.
- Evaluation of two fluxing options (mesh V paste versus tack flux) for the top PoP package and their effect on final assembly yield.
- Development of a cost effective method for transfer fluxing of the top PoP module.
- Development of a rework process for under-filled PoP components.

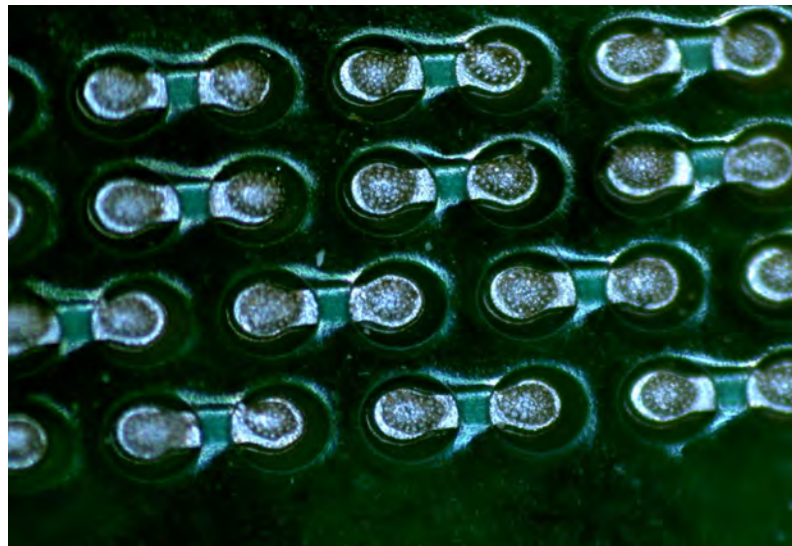
#### Test Vehicle Assembly:

All test vehicles were assembled on a conventional surface mount technology (SMT) line. The test vehicle PCB's were all screened with a No-Clean SAC 305 type III solder paste using a 5 mil thick stencil (Figure 9). The bottom packages were then placed directly on the test vehicle. The top packages were then dipped in either a flux or dippable solder paste prior to being placed on the lower package. A special fixture was developed for transfer fluxing of the top PoP package. An evaluation was conducted to determine the optimal method for transfer fluxing of the top PoP component (a transfer flux versus a "newly" developed ROLO SAC 305 transfer paste).

Once all PoP packages had been placed, the entire assembly was reflowed in a convection oven in an air environment. A reflow profile suitable for all ball metallurgies was used. The peak reflow temperature for the process ranged from 240C to 245C, with a time above 217C ranging from 60 seconds to 70 seconds (Figure 10).

The under-fill material was a reworkable epoxy based, heat cured material developed specifically for PoP applications. The under-fill was a black opaque color and had a glass transition temperature (Tg) of 69C. The coefficient of thermal expansion was 52 parts per million (ppm) below Tg and 188 ppm above Tg. The under-fill was dispensed using a conventional adhesive dispenser and allowed to flow under the packages via capillary flow. Curing was accomplished using the recommended curing profile in air of 8 minutes at a temperature of 130C.

PCB Surface Finish	Under-fill	Forced Rework
ENIG	No	No
OSP	No	No
ENIG	Yes	No
ENIG	No	Yes
OSP	No	Yes
OSP	Yes	Yes
ENIG	Yes	Yes
OSP	Yes	No



**Table 1.** Test vehicle assembly matrix.

**Figure 9.** Solder paste print using a Type III SAC305 solder paste.

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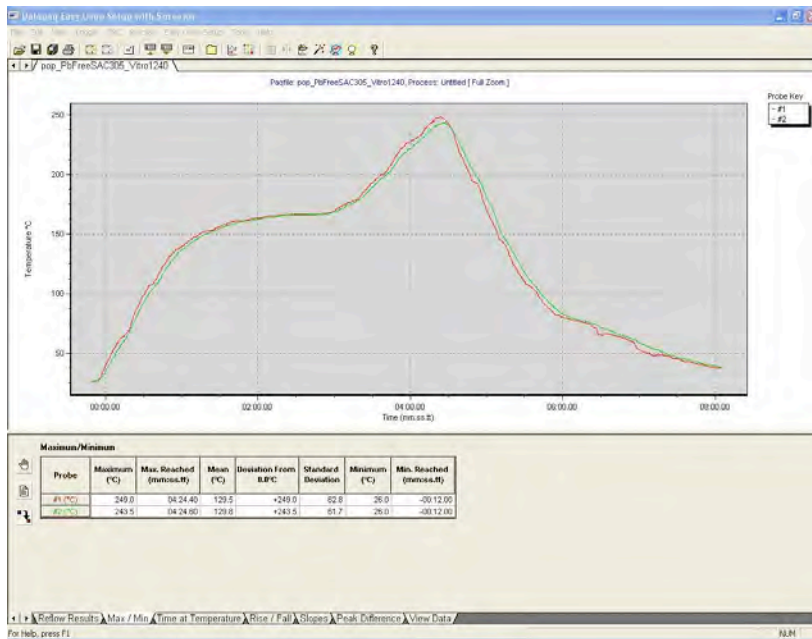


Figure 10. Reflow profile used for test vehicle assembly.

The under-fill material was a reworkable epoxy based, heat cured material developed specifically for PoP applications. The under-fill was a black opaque color and had a glass transition temperature ( $T_g$ ) of 69°C. The coefficient of thermal expansion was 52 parts per million (ppm) below  $T_g$  and 188 ppm above  $T_g$ . The under-fill was dispensed using a conventional adhesive dispenser and allowed to flow under the packages via capillary flow. Curing was accomplished using the recommended curing profile in air of 8 minutes at a temperature of 130°C.

### Forced Rework Process:

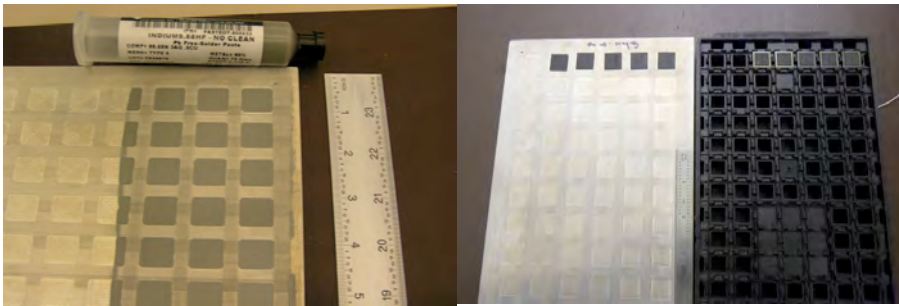
Four cells of the test matrix were reworked. Two of the rework cells consisted of under-filled PoP packages. Rework was accomplished using a combination of infrared and hot air heating. Considerable effort was spent in developing a rework process for the under-filled components since the addition of under-fill makes the rework process considerably more complex.

### Transfer Fluxing Process

TT Electronics engineers developed a semi-automated method for transfer fluxing the top module of the PoP package using a specially designed fluxing fixture (Figure 12a and Figure 12b). This fixture was developed for low volume, high mix assembly processes. This fixture has 84 pockets machined to a depth equal to 1/3 the ball height of top PoP module. Additionally, a locating mark was machined next to each pocket at a fixed distance. Using these locating marks each location can be programmed into the placement machine for automated placement of the top module into the pocket. Care was taken to ensure that the outline of the TT Fluxing fixture was the same as a JEDEC matrix tray. In doing this the tray can be utilized in the following manner:

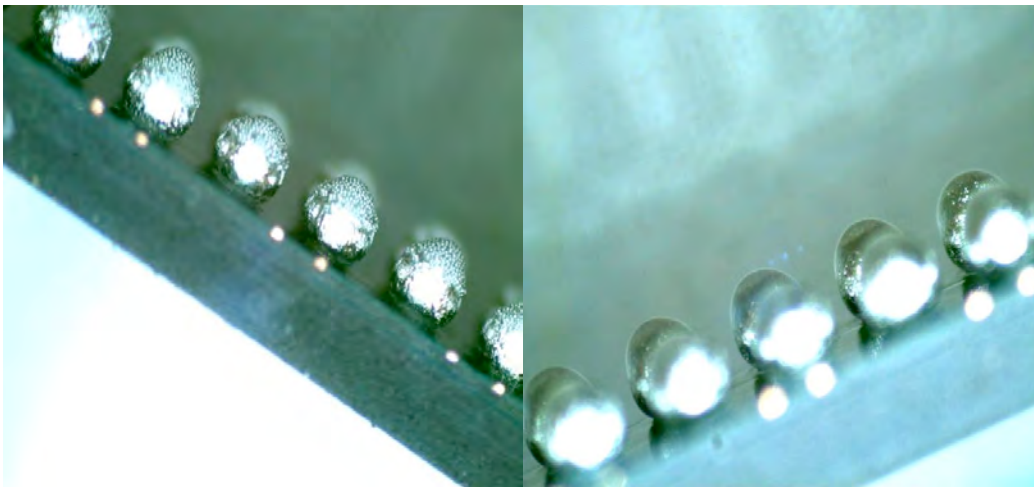
- Transfer flux (or paste) is screened into the pockets.
- The fixture is then inserted into the placement machine and the top module is inserted into the pre-fluxed pocket.

- After the top module has been placed into each of the pre-fluxed 84 pockets the tray is placed into the matrix tray handler of the placement platform.
- The pick and place tool is then used to place the bottom PoP module prior to placement of the pre-fluxed top module.



**Figure 12.** (Left) The PoP Transfer fluxing fixture developed by engineers at TT Electronics. (Right) regular JEDEC outline matrix tray for 14 mm PoP bottom and top modules.

The TT PoP Fluxing fixture provided successful soldering results on numerous trial runs (Figure 13a and 13b). A survey of recent publications on PoP assembly revealed that the preferred method of assembly is to use a paste type transfer flux for the top module. It was determined that more consistent soldering results were obtained using the Mesh V transfer paste for the assembly of the top PoP module therefore this material has been adopted as the process of record. <sup>4</sup>



**Figure 13a.** Transfer paste (Type IV) ROLO, No-Clean. **Figure 13b.** Transfer flux, No-Clean.

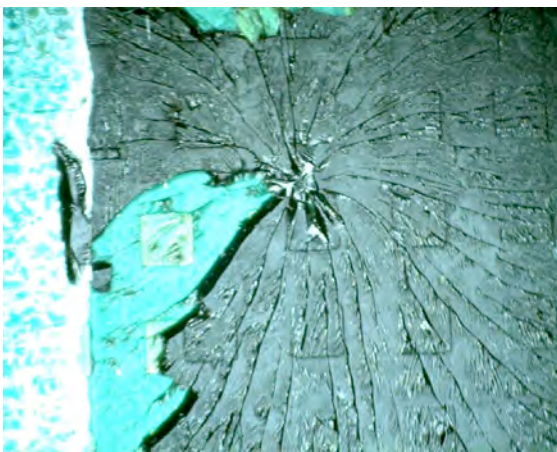


### Rework of Under-filled PoP Packages

Reworking under-filled PoP packages represents a significant challenge for development of an effective rework process. To clarify the effect of temperature on the under-fill shear strength it was determined that the shear strength of the under-fill as a function of temperature needed to be quantified. It was determined that the shear strength of the laminate could best be measured using test coupons consisting of under-fill sandwiched between two pieces of laminate. The test coupons were prepared using 1" square pieces of laminate with a thickness of 0.100". Thick pieces of laminate were used to ensure that no deformation of the sample occurred during shear testing. This allows for a more precise and consistent measurement of the under-fill shear strength. To prepare the samples the following process was used.

1. A controlled volume of under-fill was then dispensed onto one of the laminate pieces. With the under-fill acting as an adhesive and using temporary 0.005" shims to control the separation of the laminate pieces.
2. Two laminate were then joined together and temporally secured using clamps. The clamps ensured that there was no movement of the laminate / under-fill sandwich prior to curing.
3. The samples were then cured for 8 minutes at 130C.
4. Using this technique laminate / under-fill / laminate sandwiches were produced with a consistent under-fill bond line thickness of 0.005". After curing the test samples were then placed into fixture which measured the shear strength of each sample.

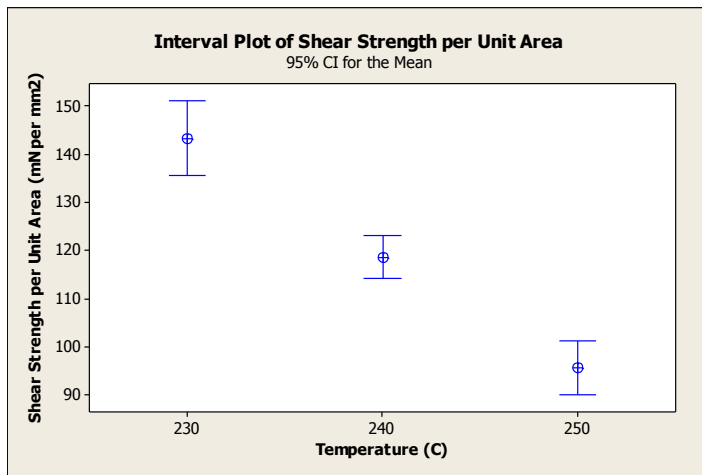
Using this technique laminate / under-fill / laminate sandwiches were produced with a consistent under-fill bond line thickness of 0.005". After curing the test samples were then placed into fixture which measured the shear strength of each sample.



**Figure 14.** The cohesive failure interface of the under-fill on the shear strength test coupons.

The fixture used to measure the under-fill shear strength was then heated to temperatures of 230C, 240C and 250C respectively. A thermocouple was used to ensure the under-fill shear test samples reached the desired temperature. The samples were then sheared to failure (Figure 14) and the maximum shear strength at cohesive failure of the under-fill was recorded. To ensure accurate shear strength measurements the area of the under-fill deposit at the failure interface was measured and then used to determine the shear strength per unit area (NOTE: all failures were cohesive in nature, no failures were observed at the under-fill laminate interface.) A total of 10 measurements were taken at each of the 3 temperatures. The

10 readings in milli-Newtons per square millimeter were recorded and the data has been plotted in Figure 14. The under-fill shear strength shows a consistent decrease in shear strength as a function of increasing temperature.

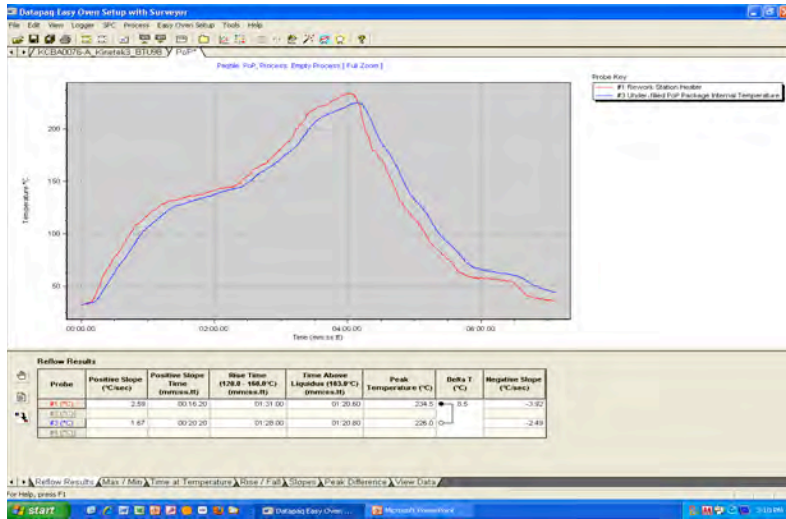


**Figure 15.** Plot of under-fill shear strength at various temperatures of interest for SAC 305 rework.

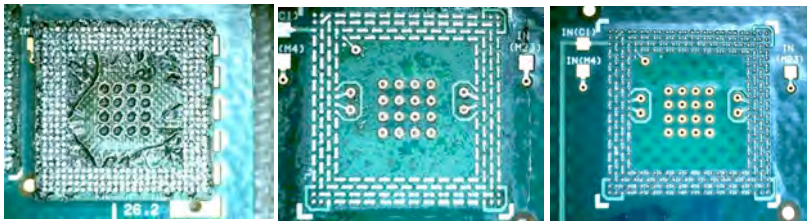
The essential elements of successful PoP package rework involve the following steps: 6, 7, 8

1. Heating of the PoP structure and removal of the Under-fill fillets from the perimeter of the package using a plastic scraping tool (taking care so as not to damage the laminate).
2. Heating of the Package on Package using an appropriate SAC305 profile (Figure 16).
3. Removal of the top and bottom PoP packages.
4. Removal of the residual under-fill using flux as a solvent and heat (Figure 17).
5. Re-dressing the site using SAC305 alloy and a soldering iron.
6. Replacements of the top and bottom package followed by reflow using an appropriate profile.
7. Reapplying under-fill and finally cure.

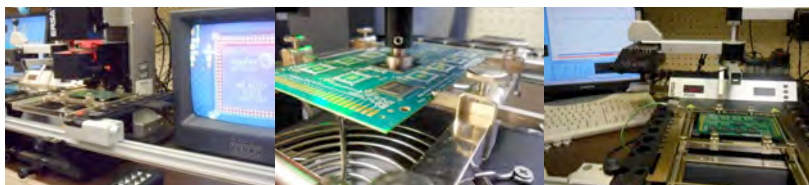
Successful rework of the PoP components requires an automated rework tool with a transfer fluxing station, vacuum component handling system, split-optics for accurate placement and a "real time" computer controlled closed loop heating system using hot air and / or infrared heating (Figure 18).



**Figure 16.** A profile developed for the removal of under-filled PoP components



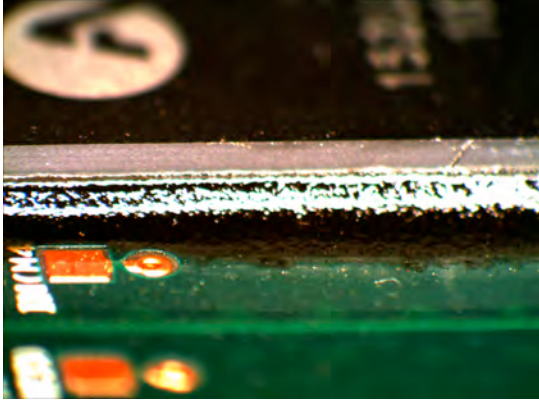
**Figure 17.** (Left) PoP rework site after removal of under-filled component. (Center) Site after complete under-fill removal. (Right) Site after complete under-fill removal and site redress.



**Figure 19.** An image of bottom PoP module only under-fill.

### Under-filled Options for PoP Packages

There are basically two options for the under-filling PoP packages. One involves under-fill of the bottom PoP module only and the second involves under-filling both the top as well as the bottom PoP modules (Figure 19 and Figure 20). A review of published literature reveals that the preferred method for optimal thermal cycle as well as drop test reliability involves applying under-filling of both top and bottom PoP modules. Thus, it was determined that all under-filling for the test matrix would be performed on both the top and bottom PoP modules. 9, 10

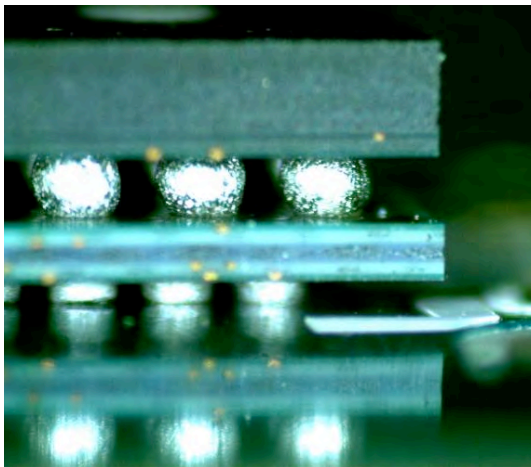


**Figure 20.** An image of complete under-fill of both the bottom and top PoP modules.

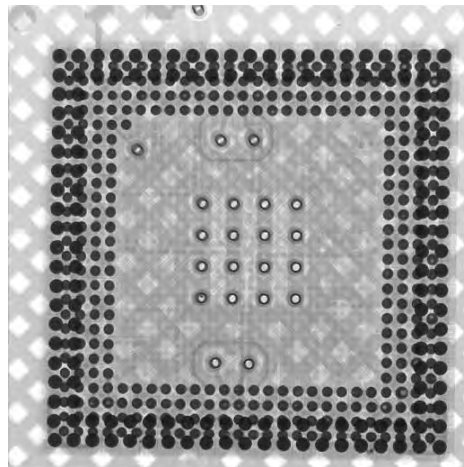
### Assembly Results

#### Assembly Yield & Cross Sections

Following assembly, all packages were inspected using Transmissive X-Ray, perimeter solder joints were inspected using an ERSA scope and all modules were electrically tested using a digital multimeter. No failures were observed after assembly. Figure 21 thru 26 show several images of the PoP packages after assembly and forced rework. Additionally no failures were observed in forced rework locations.

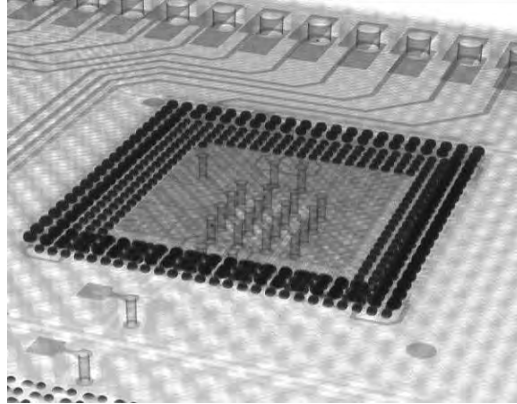
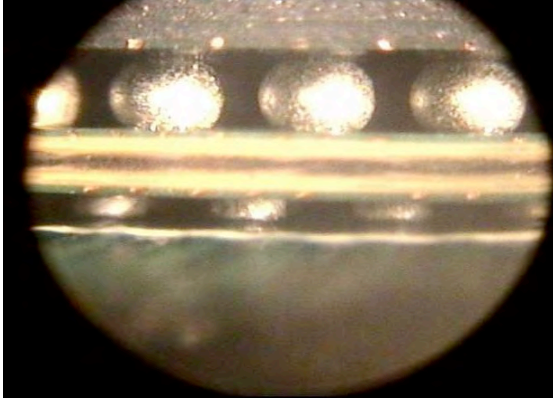


**Figure 21.** 45X Image of OSP Reworked site.

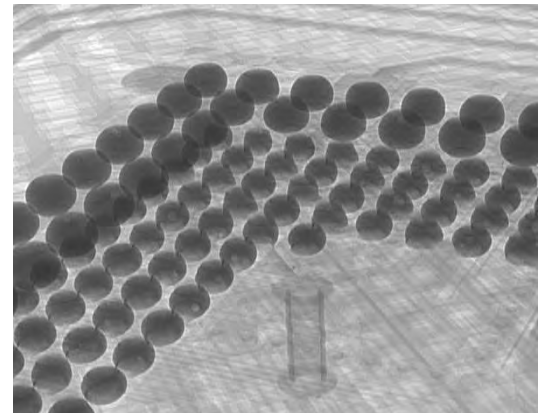
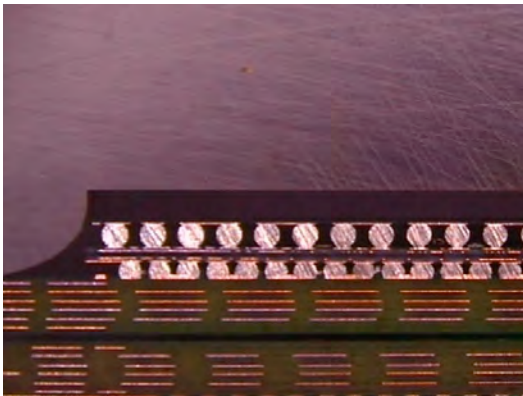


**Figure 22.** Transmission X-Ray of ENiG Forced Reworked Module.





**Figure 23.** ERSA image of ENIG finish with forced rework. **Figure 24.** 3D X-Ray image of PoP on PCB with ENIG finish.



**Figure 25.** Cross section of Under-filled Module with forced rework on ENIG finish. **Figure 25.** 3D X-Ray of OSP Forced Reworked Module.

## Conclusions

Work to date has established successful primary attach processes for package on package assembly using transfer fluxing of dippable Type V solder paste. In addition the TT PoP Fluxing fixture has shown it's viability in volume manufacturing. Both combinations of PCB surface finish (ENIG and OSP) demonstrated excellent process yields. A rework process for under-filled PoP packages was developed and effectively demonstrated in a manufacturing setting. By successfully executing the Build Matrix with no electrical failures, TT Electronics has shown it's capability to effectively assemble PoP packaging technology.

## Acknowledgments

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