Reliability of Embedded Planar Capacitors under Temperature and Voltage Stress

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Abstract

In this work the reliability of an embedded planar capacitor laminate under temperature and voltage stress is investigated. The capacitor laminate consisted of an epoxy-$BaTiO_3$ composite sandwiched between two layers of copper. The test vehicle with the embedded capacitors was subjected to a temperature of 125°C and a voltage bias of 200 V for 1000 hours. Capacitance, dissipation factor, and insulation resistance were monitored in-situ. Failed capacitors exhibited a sharp drop in insulation resistance, indicating avalanche breakdown. The decrease in the capacitance after 1000 hours was no more than 8% for any of the devices monitored. The decrease in the capacitance was attributed to delamination in the embedded capacitor laminate and an increase in the spacing between the copper layers.

1 Introduction

The basic building blocks of an electronic device consist of active and passive components on an interconnecting substrate. These passive components consist of capacitors, resistors and inductors and result in no power gain in the electronic circuit. The typical ratio of passive to active components in an electronic product such as a cell phone is about 20:1 and about 80% of the board is occupied by these components [1]. The component density due to these passive components is increasing while manufacturers simultaneously strive for reductions in the number of components and product miniaturization. It has been found that the use of thin laminate known as embedded planar capacitors, as shown in **Fig. 1**, can reduce the number of surface mount components and hence reduce board size.

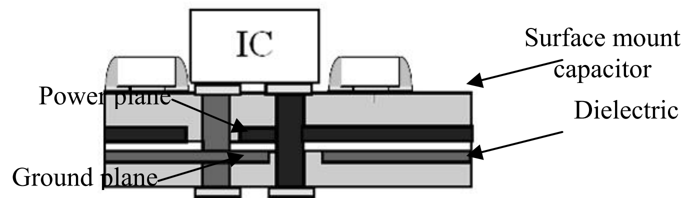


Fig. 1. Planar capacitor laminate embedded in a PWB

The concept behind an embedded planar capacitor is to utilize the capacitance between the power and the ground plane by embedding thin laminates in the printed wiring board (PWB) that serve both as a power/ground plane and a parallel plate capacitor. These laminates extend throughout the board, eliminating the need for a discrete capacitor to be adjacent to nearly every switching device. Board space taken up by these capacitors and their corresponding interconnections can be saved. Due to the lower number of solder joints the reliability of the board should improve while it's overall cost is reduced. They have also been found to reduce high frequency electromagnetic interference (EMI) as compared to discrete surface mount capacitors [2]. The key to the reduction in the number of surface mount capacitors is the low value of inductance associated with embedded capacitors due to elimination of leads and traces. Further, more than one capacitor can be formed by etching the power plane and forming multiple capacitors with a common ground plane.

The laminates for these capacitors consist of thin dielectric material sandwiched between copper layers. The dielectric material is generally a polymer ceramic composite. The advantage of this composite is that it combines low temperature processability of polymers with the high dielectric constant of ceramics [2]. The polymer typically used is epoxy or polyimide for high temperature applications. A commonly used ceramic is barium titanate, which has a high dielectric constant close to 3000. The dielectric constant of $BaTiO_3$ is size-dependent and exhibits a peak value of 5000 when the particle size is close to 140 nm [3]. With an increase in the ceramic loading the dielectric constant of the composite increases. An increase in ceramic loading beyond 55-60% by volume decreases the capacitance due to the presence of voids and pores in the composite when the theoretical maximum packaging density is exceeded [4]. Typically, for reliability reasons the maximum ceramic loading should be lower than 50% by volume, which limits the maximum dielectric constant close to 30 [5].

Although these capacitors have many advantages, the reliability of these devices will determine the breadth and success of their practical application. This depends on the failure mode of an embedded capacitor will generally lead to failure of the PWB, since these capacitors are not reworkable. The failure mode can be a change in capacitance, dissipation factor, or insulation resistance. Possible failure modes and mechanisms due to temperature and voltage stress are discussed in this paper. Reliability tests are conducted by stressing the boards at a temperature of 125°C and a voltage of 200 V. Previous

publications on embedded capacitors have not reported how insulation resistance of the dielectric varies during reliability tests. In the current test, along with capacitance and the dissipation factor, insulation resistance is also monitored in-situ.

2 Failure modes and mechanisms due to temperature and voltage stress

The parameters of an embedded capacitor can change with time due to temperature and voltage stress. The failure mode is typically a decrease in capacitance or insulation resistance.

2.1 Decrease in capacitance

The capacitance can decrease with time due to thermal deformation and delamination in the capacitor laminate. These phenomena are driven by the thermo-mechanical stresses developed at the dielectric-Cu plane interface. Stress arises due to the difference in the coefficient of thermal expansion (CTE) between the dielectric and the Cu plane. Possible sources of thermal stresses can be variations in the ambient temperature, self heating due to power dissipation and solder reflow. The thermal stress due to CTE mismatch can be expressed by the following equation [6]:

$$\sigma = c\int_{T_1}^{T_2}\left[\frac{\alpha_p - \alpha_i}{\frac{1}{E_p} - \frac{1}{E_i}}\right]dT$$

(1) where c is a geometry-dependent constant, α is the coefficient of thermal expansion (CTE), E is the modulus of elasticity, and the subscripts p and i denote the dielectric and the Cu plane, respectively. Deformation and delamination can increase the spacing between the copper planes and hence decrease the capacitance. The capacitance of a planar capacitor is given by the expression:

$$C = \frac{k\varepsilon_0 A}{d}$$

(2)
where k is the dielectric constant, ε_o is the permittivity of free space, A is the plate area, and d is the spacing between the plates.

Another possible mechanism of decrease in capacitance is ageing in the $BaTiO_3$ and other ferroelectric ceramics [7]. It has long been known that the dielectric constant of unpolarized ceramics suffers a loss of 15-20% in the course of a year. Ageing can be described by the well known equation [8]:

$$\frac{C}{C_0} = 1 - k\{\log(t)\}$$

(3) where C is the capacitance after time t, C_0 is the initial capacitance, k is the dielectric ageing rate, and t is the time. Ageing is a gradual process in dielectrics made of barium titanate. It begins after the capacitor's last excursion beyond the Curie point. Capacitors can be restored to their original capacitance by heating them above their Curie point for a

period of time. The ageing process is thermally activated and the ageing rate increases with an increase in temperature [9]. It is known that the dielectric ageing can be reduced by lowering the tetragonality of the perovskite structure [10]. It was reported by Yamamatsu *et al.* [10] that higher oxygen partial pressure during firing increases the ageing rate in a multilayer ceramic capacitor (MLCC) with $BaTiO_3$ dielectric. The reason for this increase was attributed to an increase in the cation vacancies due to higher oxygen partial pressure.

The capacitance can also drop due to residual stress relaxation in the polymer matrix [10]. The residual stresses in the polymer matrix generated during the curing process can be relaxed by exposure to temperatures above the glass transition temperature (T_g). Polymer chains can freely move above T_g, and their total volume increases. An increase in free volume leads to the decrease of the dielectric constant since the dielectric constant of free volume is equal to 1.0. Therefore the capacitance can decrease after exposure to temperature above T_g.

2.2 Decrease in insulation resistance

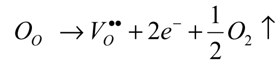
Insulation resistance can decrease due to voltage and temperature and is generally a concern in high dielectric constant multilayer ceramic capacitors (MLCC) [12]. The accelerated life is known to follow this well-known empirical equation [13]:

$$\frac{t_1}{t_2} = \left(\frac{V_2}{V_1}\right)^N \exp\left(\frac{E_a}{k}\left(\frac{1}{T_1} - \frac{1}{T_2}\right)\right)$$

(4) where t is the time-to-failure, V is the voltage, N is the voltage exponent, E_a is the activation energy, k is the Boltzmann constant, T is the temperature, and the subscripts *1* and *2* refer to the two stress conditions.

Typically there are two modes for a decrease in insulation resistance [14]. In the first mode, there is an abrupt drop in insulation resistance which is known as avalanche breakdown (ABD). In the second mode, the drop in the insulation resistance is more gradual, which increases the self-heating due to an increase in the leakage current and subsequent failure. This second failure mode is known as thermal runaway (TRA). A higher voltage normally favors the occurrence of an ABD-type of failure mode, while a higher temperature normally favors the TRA-type of failure mode. The cause of ABD is attributed to extrinsic flaws such as porosity, delaminations, thin spots, cracks, local contamination and voids in the device. The cause of TRA is attributed to various mechanisms such as oxygen vacancy generation and decrease in the grain boundary barrier height, which are discussed below.

The mechanism of degradation in insulation resistance in $BaTiO_3$ dielectric is due to oxygen vacancy generation, and reduction in the grain boundary barrier height [15]. Under voltage and temperature stress, oxygen vacancies are generated according to the reaction:



$$O_O \rightarrow V_O^{\bullet\bullet} + 2e^- + \frac{1}{2}O_2 \uparrow$$

(5) where O_O is an oxygen atom at an oxygen lattice site, V_O is a vacancy at an oxygen site, e^- is the conduction electron, and O_2 is the liberated oxygen. The two electrons will contribute to the leakage current, which is expected to increase exponentially with time [15]. Another possible mechanism for an increase in the leakage current is a decrease in the grain boundary barrier height. Grain boundaries are found to control charge in several polycrystalline materials. In such materials the leakage current is found to depend on the barrier height of the grain boundary by the following equation [16]:

$$I = I_0 e^{-\frac{\phi}{kT}}$$

(6) where I is the current, ϕ is the grain boundary barrier height, k is the Boltzmann constant, and T is the temperature. The grain boundary barrier height (ϕ) for homogeneous grains is expressed as:

$$\phi = \frac{e^2 N^2}{8\varepsilon N_i}$$

(7) where e is the charge on an electron, N is the density of filled states in the grain boundary, ε is the permittivity, and N_i is the ionized impurity density in the grain boundary. Accumulation of ionized impurities at the grain boundaries will lead to a decrease in the barrier height, which may increase the leakage current.

3 Test vehicle and preliminary tests

The test vehicle is a 4-layer board in which layer 1 and 4 are the signal layers, and the planar capacitor laminate forms layer 2 (power plane) and layer 3 (ground plane). The power plane is etched at various locations to form discrete capacitors. Each capacitor has the power plane connected to the PTH as shown in Fig. 2. The ground plane is common for all capacitors and continuous as far as possible (except for the antipads).

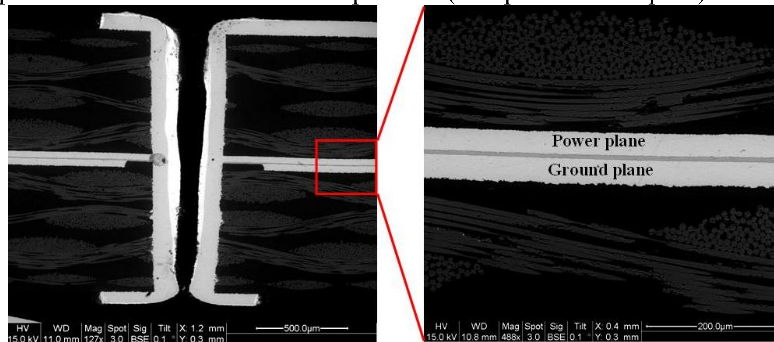


Fig. 2. Sectional view of an embedded capacitor

The dielectric is a composite of $BaTiO_3$ and bisphenol-epoxy. Since $BaTiO_3$ is a ferroelectric material it is expected that the composite would exhibit ferroelectric properties. Barium titanate exhibits a sharp increase in the dielectric constant around the

Curie temperature (T_c), which is about 125°C due to a second order phase transition from a tetragonal structure to a cubic structure. It is also known that the capacitance of a ferroelectric dielectric is a function of the applied voltage. To investigate these behaviors, the capacitance was measured as a function of the temperature and voltage as shown in **Fig. 3** and **Fig. 4**. The sharp increase in capacitance around the T_c is absent, and there is no voltage dependence on the capacitance. These plots show that the composite does not behave as a typical ferroelectric material.

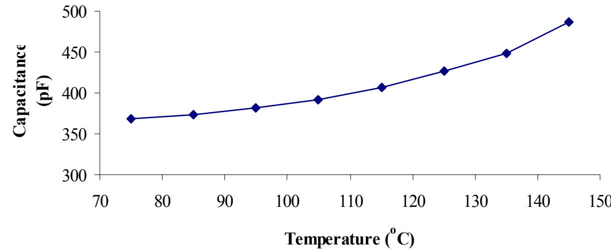


Fig. 3. Effect of temperature on capacitance.

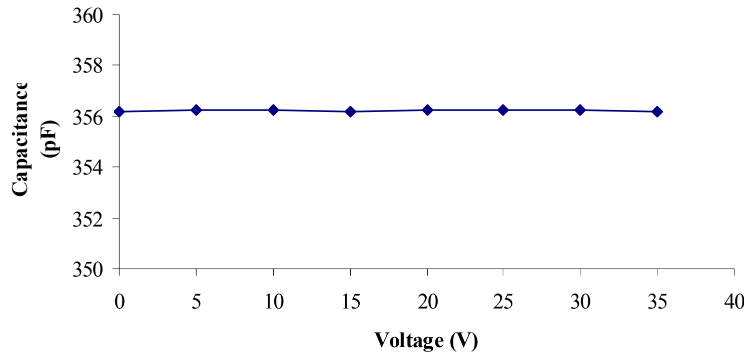


Fig. 4. Effect of voltage on capacitance

To investigate the reliability of these devices under temperature and voltage stress, a temperature of 125°C and a voltage of 200 V were applied. The temperature was selected as 125°C since the maximum operating temperature of the test board was 130°C. The applied voltage was selected such that the voltage was well below the breakdown voltage of these capacitors at 125°C. The breakdown voltage was measured at 85°C and 125°C. The sample size for the breakdown voltage measurements was 10. The results of the breakdown voltage are shown in **Fig. 5**. It was observed that the value of the breakdown voltage decreased with an increase in the temperature. The reduction in the breakdown voltage can be explained by an increase in free volume of the polymer matrix. The breakdown electric field (E_b) is given by the expression [16]:

$$E_b = \frac{W_{th}}{el_x}$$

(8) where W_{th} is the energy needed to break the bond of the polymer, e is the charge on the electron, and l_x is the mean free path of the charge carrier. An increase in the free volume of the polymer at a higher temperature increases the mean free path of the charge carrier (l_x) and the breakdown electric field (E_b) reduces. The breakdown voltage at 125°C was found to be 355.7 ± 40.1 V. The devices were stressed at 200 V so that the applied voltage was less than the breakdown voltage. In other studies [18] on accelerated life testing of MLCCs the applied voltage selected was 50% of the breakdown voltage.

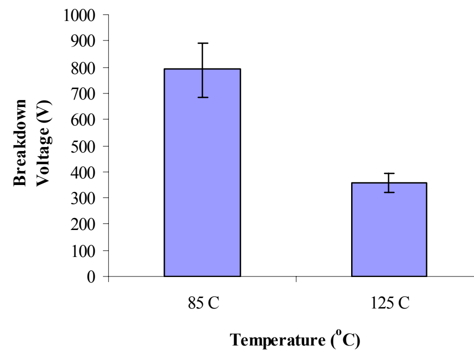


Fig. 5. Breakdown voltage at 85°C and 125°C

4 Reliability under temperature and voltage stress

The test board had 80 capacitors, each of area 0.026 in^2, out of which 33 capacitors were selected for reliability investigation. The boards were preconditioned at 105°C for 48 hrs to remove any trace of moisture. The failure criteria selected were:

- 20% decrease in capacitance at 100 KHz
- Drop in insulation resistance to 1.1 MΩ (The value of the resistor attached in series with each capacitor) at 10 V
- Increase in dissipation factor by a factor of 2 at 100 KHz

The test board was subjected to a temperature of 125°C. Initial measurements performed at this temperature were used as the baseline value to detect any shift in the parameters. Subsequently, a voltage of 200 V was applied across all the capacitors for 1000 hrs. Three parameters, capacitance, insulation resistance, and dissipation factor were monitored in-situ once every hour.

The capacitance was found to decrease with time; however the decrease was not significant enough to be considered a failure. A distribution of the decrease in the

capacitance is shown in **Fig. 6**. It was observed that the maximum decrease in the capacitance for all capacitors was less than 8%.

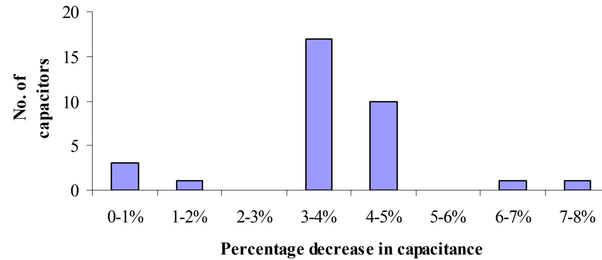


Fig. 6. Distribution of decrease in capacitance.

Capacitance can decrease because of an increase in the spacing between the copper planes or a decrease in the dielectric constant due to applied stress. A typical plot of a decrease in capacitance is shown in **Fig. 7**.

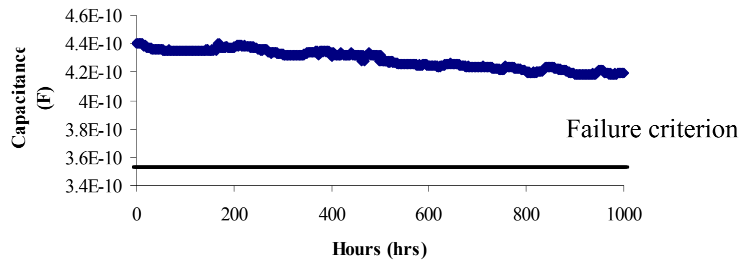


Fig. 7. Typical plot of capacitance with time

Dissipation factor was found to decrease with time. This meant that the capacitor was improving after stress was applied. A typical plot for the dissipation factor is shown in Fig. 8.

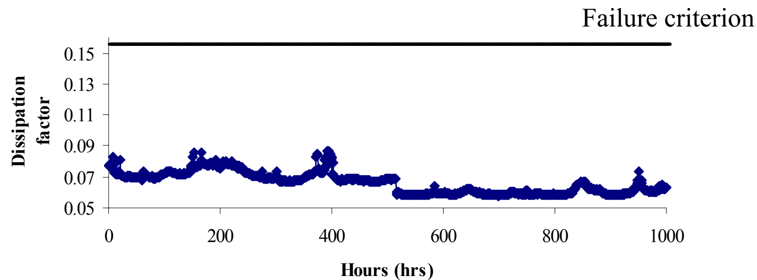


Fig. 8. Typical plot of dissipation factor with time

The only failures observed were due to insulation resistance. Six out of 33 capacitors failed due to a sudden drop in the insulation resistance, implying avalanche breakdown

(ABD). A typical plot of insulation resistance in a non-failed capacitor with time is shown in **Fig. 9**. In non-failed capacitors, insulation resistance was found to fluctuate but also displayed a gradual increase with time. This gradual increase in the insulation resistance was consistent with the trend of dissipation factor. The dissipation factor is the ratio between power dissipated in the dielectric (in the form of heat) and the total power transmitted through the dielectric. A decrease in dissipation factor implies a decrease in power loss through the dielectric. Since the power loss due to heating had reduced, it can be concluded that the leakage current through the dielectric had also reduced leading to an increase in the insulation resistance.

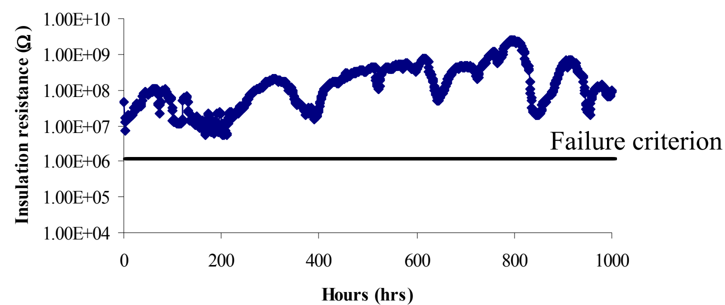


Fig. 9. Typical plot of insulation resistance of non-failed capacitor with time

The insulation resistance of the failed capacitors also showed a fluctuation with a gradual increase but this was followed by a sudden drop suggesting ABD type of failure mechanism. A typical plot of the insulation resistance in a failed capacitor is shown in Fig. 10. The behavior of insulation resistance in this composite is different to what is observed in dielectrics of pure $BaTiO_3$ [14] [15] [16] (where the insulation resistance is found to degrade by TRA). Furthermore, insulation resistance of non-failed capacitors was found to increase gradually with time.

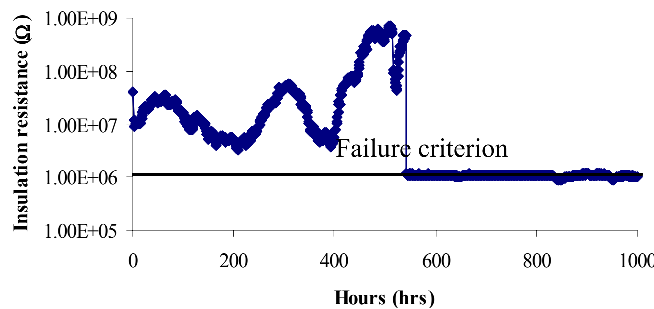


Fig. 10. Typical plot of insulation resistance of failed capacitor with time

5 Failure analysis

Failure analysis was performed to identify the root cause of the decrease in capacitance. The distance between the Cu planes was measured at 3 different locations: A, B, and C using an environmental scanning electron microscope (ESEM). At each location 12 measurements were performed as shown in **Fig. 11**. Four unstressed and four stressed capacitors (125°C and 200 V for 1000 hrs) were selected.

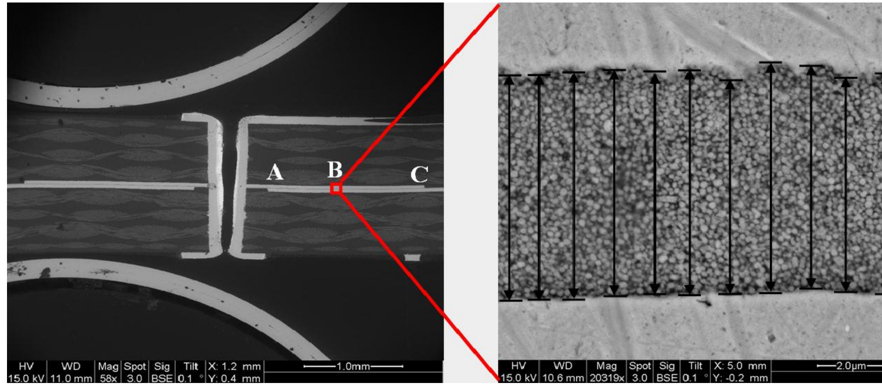


Fig. 11. Location A, B, and C for failure analysis

The results of the measurements performed are shown in

Table 1. It was observed that the spacing between the Cu planes was not uniform and was larger at the edges of the capacitor. After stressing the capacitors by temperature and voltage, the spacing between the Cu planes was found to increase at all locations. This increase in the spacing between the Cu planes was expected to cause a decrease in capacitance. Furthermore, delamination was also found at multiple locations in the embedded capacitor laminate of the stressed capacitor as shown in Fig. 12. This delamination may have been due to the thermal stresses developed at the dielectric-Cu interface and may have reduced capacitance.

Table 1: Measurements of spacing between the Cu planes

	Location A (µm)	Location B (µm)	Location C (µm)
Unstressed	6.6 ± 0.36	6.2 ± 0.36	6.6 ± 0.38
Stressed	7.2 ± 0.37	6.6 ± 0.39	7.2 ± 0.49

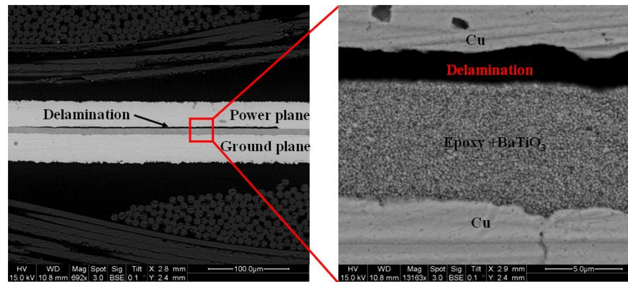


Fig. 12. Delamination at the dielectric-Cu interface

6 Conclusions

The reliability of an embedded planar capacitor laminate with epoxy-$BaTiO_3$ composite dielectric was investigated during temperature and voltage stress conditions (125°C and 200 V). The failure mechanisms under these conditions were found to be avalanche breakdown and delamination in the planar capacitor laminate. It was also found that the $BaTiO_3$-epoxy composite behaved differently than a typical ferroelectric material. The capacitance of the composite dielectric was constant with voltage and there was no increase in the capacitance around the Curie temperature of $BaTiO_3$. Furthermore, insulation resistance of non-failed capacitors was found to increase with time. This behavior is uncommon in a pure $BaTiO_3$ dielectric. The reason for the increase in insulation resistance during temperature and voltage stress is still under investigation. It is expected that the cross-linking density in the epoxy matrix increased with time due to the applied temperature. An increase in the cross-linking density might hinder the motion of charge carriers and increase the insulation resistance.

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