Overview of Quality and Reliability Issues in the National Technology Roadmap for Semiconductors

Technology Transfer # **98013448A-TR**
SEMATECH
January 30, 1998

Abstract: This document is an update to the 1994 Quality and Reliability Roadmap issued in support of the 1994 National Technology Roadmap for Semiconductors. This report revisits the challenges, constraints, priorities, and research needs pertaining to quality and reliability issues. It also provides key project proposals that must be implemented to address concerns about reliability attainment and defect learning. An expanded section on test-to-test, diagnostics, and failure analysis; an edited version of the Product Analysis Forum Roadmap; and an appendix containing a draft report highlighting reliability issues is included.

Keywords: Design, Failure Analysis, Packaging, Quality Management, Reliability, Reliability Modeling, Silicon

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Acknowledgements

SEMATECH wishes to thank the following persons and organizations for their contributions to this document and the work leading up to it:

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	Kola Olasupo, section manager, Q&R Engineering
Digital Equipment	Bob Deysher, group quality manager
Hewlett-Packard	Dennis Eaton, reliability manager
IBM	Bharat Bhargava George Prokop Hugh Sweeney, manager, Memory and Special QA
Intel	Steve Huber, Assembly TD, Q&R manager
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Lucent	Carl Peridier, IC reliability engineer
Motorola	Nick Lycoudes, Reliability Engineering manager
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Consultant	Dino Barpoulis, co-chair, Quality Council
	National Laboratories and Semiconductor Research Corporation
Livermore	Mike Fluss, deputy director
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Packaging	Don Denton, leader (TI), Richard Blish (AMD), Ron Bracken (SRC), Dennis Eaton (HP), Gail Heinen (TI), Steve Huber (Intel), John Jackson (NSC), Nick Lycoudes (Motorola)
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Test, Diagnostics, and Failure Analysis	Dino Barpoulis, leader (consultant), Richard Clark (Intel), Nick Lycoudes (Motorola), Jerry Soden (Sandia), Hugh Sweeney (IBM), Dave Vallett (IBM)

Additional thanks also are due to the following persons for assisance in preparing the *Product Analysis Forum Roadmap* that appears within this document:

Sudhakar M. Kudva, Intel Corp.	Bob Ash, Motorola
Richard Clark, Digital Equipment corp.	Joseph Serpiello, American Telephone and Telegraph
Dave Vallett, International Business Machines	Ken Huffman, SEMATECH
Ted Hasegawa, National Semiconductor Corp.	Larry Wagner, Texas Instruments
Glen Gilfeather, Advanced Micro Devices	Matt Thayer, Advanced Micro Devices
Seshu Pabbisetty, Texas Instruments	Saeed Kazmi, Advanced Micro Devices
Robert Shreeve, Hewlett-Packard	Dick Ross, International Business Machines

1 EXECUTIVE SUMMARY

This document is an update to the 1994 *Quality and Reliability Roadmap* (Q&R Roadmap) that was issued in support of the 1994 *National Technology Roadmap for Semiconductors* (National Roadmap). This report revisits the challenges, constraints, priorities, and research needs pertaining to Q&R issues. It also introduces key project proposals that must be implemented to address concerns over reliability attainment and defect learning.

Key findings in this report include the following:

- Outlooks vary on what it will take to satisfy customers in the year 2000 for quality and reliability.
- Continued stretching of existing processes and rapid introduction of significantly changed materials illustrate the need for a new reliability strategy. This should include new projects and funding to establish understanding of mechanisms of failure, models, incorporation of models into the design systems; and metrics for reliability defects in process and test as part of the equipment cost of ownership (COO).
- Scaling of reliability models with the projected changes in technology described by the National Roadmap is an issue that presents several excellent research opportunities.
- Customer application requirements in more severe environments continue to escalate the need for improved electrostatic discharge (ESD) protection. The technology direction of more wiring per chip and increased pad and pin counts raises the question of when limits on ESD will be reached.
- Serious gaps exist in TCAD and CAD tools for product designs that do not adequately simulate the effects of failure mechanisms. Exploration is needed in the development of methodologies for TCAD and CAD tools to allow determination of performance (i.e., electromigration).
- Worldwide demand continues to drive faster, lighter, smaller, cost-effective systems for packaging ICs. Current approaches eliminate a packaging level through chip-to-board connection or smaller chip scale packaging. These pose two general issues: reliability expectations in customer use environments and tools for package reliability analysis.

Emphasis on defect learning will be found in this update through an expanded section on test-to-test, diagnostics, and failure analysis and inclusion of an edited version of the *Product Analysis Forum Roadmap*. Also, reliability issues are highlighted in a draft report in the appendix.

2 INTRODUCTION

In the 1994 issue of the Q&R Roadmap, significant challenges in reliability technology were explored and reliability was scaled overall against yield learning. To meet the 5X level of reliability improvement expected by customers between 1994 and 1998, defect density (defects/chip) learning must be accelerated beyond the 3.9X projected, with required yields of 95% compared to the 84% yields planned. The significance of the challenge in defect density learning is illustrated by considering the high resistive contact via defect by itself. Current designs number contact vias in the tens of millions, with that number scaled upwards in the strategic time frame. Even if the current reliability levels are retained (notwithstanding the

extrapolated 1.0–0.1 failure units [FITs] in the strategic time frame) as future reliability requirements, there can be no room for high resistive contact via defects. The via process must be perfect to meet yield, reliability, and cost objectives. This challenge stretches existing process capabilities and is compounded by additional challenges and opportunities raised by the introduction of new materials and processes. An adjunct group was formed by the Reliability Technical Advisory Board (RTAB) during this update period to tackle the challenge of electrical overstress (EOS)/ESD. Formation of an ESD benchmark/standards group is anticipated in 1997.

3 ROADMAP OVERVIEW: QUALITY AND RELIABILITY ISSUES

A key issue carried forward from the 1994 Q&R Roadmap is the shortfall in defect density learning for yield, compared to improvements expected by customers in quality and reliability from 1992–1998. Outlooks vary on what it will take to satisfy year 2000 customers for quality and reliability (see Table 7 and Table 9). Some believe customer expectations for quality and reliability can be achieved by maintaining the current levels in test escapes (shipped product quality level [SPQL]) early life (EL), and end of life (EOL) failure rates at year-end 2000. Others project continued reduction in meeting the customer's challenge of 1.0–0.1 FITs in the strategic time frame. What is evident is that the projections made in 1994 for 1997 have been achieved in test escapes and EOL, but not in EL reliability. Indeed, for EL the learning curve has flattened out, with no improvement between 1992 and 1997.

Whether continued learning to 1.0–0.1 FITs or no further learning to meet customer satisfaction in quality and reliability is accepted as the objective, either expectation will be difficult to achieve with the continued stretching of existing processes and the rapid introduction of the most significant change in material set that the industry has seen (Cu, Low k dielectrics, oxi-nitride gates, etc.). A new reliability strategy, projects, and funding will be needed to establish understanding of mechanisms of failure, models, incorporation of models into the design systems, and metrics for reliability defects in process and test as part of the equipment COO.

An example of a particular defect type, contact/interlevel vias, illustrates how complexity will place extreme requirements on process perfection. Already, this process must achieve tens of millions of vias per chip without high interface resistance to meet yield, quality, and reliability objectives. This problem is compounded by limitations in testability, diagnosability, and failure analysis for process and design learning. That is why the test section in the 1994 Q&R Roadmap has been expanded here to include test, diagnostics, and failure analysis roadmaps.

Scaling of reliability models with the projected changes in technology described by the National Roadmap presents several excellent research opportunities. The National Roadmap shows gate oxides decreasing to 4.5 nm in 1998 and to 3.4 nm in 2004, with fields increasing in excess of 5.0 MV/cm. Susceptibility to gate dielectric breakdown will increase, and the gate conduction mechanism will change from Fowler-Nordhiem tunneling to direct tunneling when gate oxide thickness falls below 35–40 Å. There is a strong need to understand the reliability implications of these changes to assess the true cost of making them.

Customer application requirements in more severe environments continue to escalate the need for improved ESD protection. The technology direction of more wiring per chip and increased pad and pin counts raises the question of when limits on ESD will be reached. No method of comparative measurement is in place for the industry other than the existing Human Body Model

(HBM), Charged Device Model (CDM), and Machine Model (MM). The industry needs a standard for comparative measurement, metrics, and models that fit within a technology family.

Serious gaps exist in technology computer-aided design (TCAD) and CAD tools for product designs that do not adequately simulate the effects of failure mechanisms. Exploration is needed in the development of methodologies for TCAD and CAD tools to allow determination of performance (i.e., electromigration). Several university R&D programs funded through Semiconductor Research Corporation (SRC) show considerable promise for establishing the physical and electrical behavioral models needed. These programs must be brought to fruition and integrated with design systems that can be deployed commercially.

Worldwide demand continues to drive faster, lighter, smaller, cost-effective systems for packaging ICs. Current approaches eliminate a packaging level through chip-to-board connection or smaller chip scale packaging. These pose two general issues: reliability expectations in customer use environments and tools for package reliability analysis.

Research projects are proposed to address the opportunities of top reliability issues.

4 OVERVIEW OF SILICON TECHNOLOGY RELIABILITY CONSTRAINTS

Future silicon reliability constraints will be driven by technology scaling, process complexity, new material introductions, device demands and customer requirements. Technology scaling will impact reliability by increasing electric fields across dielectrics as well as increasing stresses on all elements of the structure. Process complexity will increase the risk of damage to circuits, raising the risk of latent damage. New materials are planned to improve performance, but their behaviors have not been adequately characterized and modeled. Future designs require more performance, resulting in increased temperatures and reduced reliability margins. Finally, customers are demanding improved performance and functionality without compromising quality and reliability.

The challenge will be to model and predict silicon reliability concurrently with the increase in process complexity, rapid technology scaling, new material introduction, while assuring customers that product requirements are being met. Ideally, reliability scaling models, similar to technology scaling models, should be developed and verified.

Table 1 describes the significant silicon reliability constraints that must be addressed. Of major importance to the industry are the following:

- Gate dielectric reliability
- Electromigration
- Electrostatic discharge
- Multilevel interconnects
- Hot carrier injection
- Antenna, wafer charging effects
- Junction temperature increase
- Soft error/single event upset

This list is incomplete, and other items identified in this report also require appropriate attention. It is key that the industry identify, characterize, and control potential failure mechanisms so that reliable products can be manufactured and delivered to customers.

Table 1 Prioritization of Reliability Related Technology Constraints (Year 2000 Projection)

	Silicon									
	A	**B**	**C**	**D**	**E**	**F**	**G**	**H**	**I**	**Total**
Gate Dielectric Reliability	1	4	1	3	5	1	1	5	4	**25**
Electromigration	5	5	3	6	6	5	3	13	1	**47**
ESD	6	6	8	2	8	3	5	9	2	**49**
Multi Level Metal/Dielectric Integrity	12	8	10	5	1	10	2	3	8	**59**
Hot Carriers	9	1	2	8	12	6	4	11	7	**60**
Defectivity, Cleanliness	4	9	4	1	15	7	13	1	12	**66**
Wafer Charging/Antenna Effects/Ultra Thin Oxides	2	17	15	16	4	2	7	2	3	**68**
Noise Margin/Coupling	13	2	5	4	7	9	14	12	6	**72**
Latch-up	15	7	9	10	13	4	6	4	11	**79**
Leakage Isolation	8	14	6	11	10	11	9	10	15	**94**
Tools for Reliability Checking	3	12	17	17	9	8	12	7	9	**94**
Pkg. Induced Failures	14	13	14	15	3	15	10	8	10	**102**
Soft Error (Single Error Upset)	11	16	16	13	2	14	16	14	5	**107**
Cost Effective Reliability & Qualification	7	11	7	14	14	17	8	17	13	**108**
Mixed Signal Requirements for Transistor Matching	17	15	13	2	16	12	11	6	17	**109**
Perf./Power/Reliability Trade-offs	10	10	11	7	11	16	15	15	16	**111**
Increasing Max. Tj	16	3	12	9	17	13	17	16	14	**117**

1 = Highest Priority

4.1 Reliability of Gate Dielectrics

Problem Statement

The susceptibility to gate dielectric breakdown will increase because of the following:

1. Thinning of the dielectric
2. Small increases (after correcting for band bending) in the gate electric field
3. Increase in the gate area/die (especially if large decoupling capacitors are needed)
4. Increased sensitivity to post-gate processing

Furthermore, as the gate oxide thickness is scaled below ~50 Å, the gate conduction mechanism will change from Fowler-Nordhiem tunneling to direct tunneling. This could impact, positively or negatively, the reliability of the gate dielectrics.

Key Issues

These issues include the following:

1. Measuring time-dependent dielectric breakdown (TDDB) requires large sample sizes, yet may not measure the failure mechanism that occurs during normal device operation. AC measurement capabilities are very limited. Without statistically valid, meaningful characterization, it will be difficult to address the other key issues.
2. There is still uncertainty about the model for field acceleration of dielectric breakdown under DC biases. Modeling of high frequency effects is less developed. Validated physical and statistical models are required to predict reliability and to design screens.
3. The transition to direct tunneling could introduce new failure modes. Scaled technologies will have less tolerance for drifts in transistor parameters.
4. Gate dielectric reliability will be increasingly sensitive to the complete process flow, not just to the gate oxidation step.
5. Other issues include diffusion through the dielectric from the p-channel poly gates and accurately accounting for band bending in determining the electric field in the dielectric.

Research Needs

These needs are as follows:

1. Understand and control the impact of post-gate processing on gate oxide reliability.
2. Develop rapid methods of qualifying gate dielectrics.
3. Increase the use of TCAD tools.
4. Develop practical methods to do statistically valid characterization gate oxide reliability that accurately reflect the performance of real devices.
5. Characterize the impact of direct tunneling on dielectric breakdown and investigate if any new failure modes (e.g., instabilities) are introduced.
6. Develop predictive DC and AC models for gate oxide reliability.

4.2 Electromigration

Problem Statement

Present and planned reductions of metal-interconnect dimensions are reducing and making more uncertain the margin for error in designing and manufacturing metal interconnects of adequate reliability. Significant efforts are needed to optimize and measure reliability performance.

Key Issues

Materials engineering and building-in reliability approaches are required to optimize existing and developing aluminum-based metallization systems and associated processes and materials. The approaches involve methods to understand and utilize the interactions of the constituent materials, processing materials, processes, thermal history, and processing equipment. They require methods to identify and control aspects that affect interconnect reliability in, for example, the design of the metal system and the design and operation of the processes and processing equipment used to deposit and treat the metal and associated interlayer-dielectric films.

Gaps and deficiencies exist in the tool set for measuring reliability of interconnects, e.g., in evaluating vias, characterizing the effect of pulsed-current stresses, and characterizing susceptibility to stress voiding. Gaps also exist in characterizing the early reliability of the interconnect system. To help fill these gaps requires a better understanding of the effect of accelerated stress conditions on the metal system so that more accurate estimates can be made of the actual acceleration of stress test, and assurances given that the conditions of the stress test are related to use conditions.

Copper-based metallizations offer the advantages of lower resistivity and higher potential resistance to electromigration if processing problems can be overcome. The decision to use such metallizations will depend partly on how well aluminum-based systems can continue to be optimized. Work is needed first to solve problems related to copper deposition, containment, and integration with adjacent materials.

Research Needs

These needs include the following:

1. Develop materials engineering and building-in reliability approaches.
2. Identify and control parameters of the deposition process that affect metal film quality, e.g., film temperature, material purity, and substrate texture.
3. Develop reliability models for aluminum-based vias.
4. Develop measurement (standard) methods and structures for characterizing reliability of vias, susceptibility to stress voiding, pulsed-current stresses, and early reliability of metal systems.
5. Assess the impact of copper interconnect and its potential resistance to electromigration.

4.3 Electrostatic Discharge

Problem Statement

The continued Human Body Model requirement on ESD robustness of >2KV, the Machine Model requirement of >200V, and the Charged Device Model of >1KV will constrain the ability to scale to smaller geometries and to operate devices at lower voltages. New protection circuit

designs must account for process technology variations and design rel cases to different fabrication facilities. Additionally, with increasing pad counts and higher density circuits, space available for effective ESD will be at a premium.

Key Issues

Silicon technology strongly influences ESD capability. Designs that function well in one technology do not necessarily show similar performance in newer submicron processes. Circuit elements must withstand heating effects, sink large amounts of current, and remain undamaged by high electric fields.

Key process parameters that influence ESD performance must be identified and characterized. It is critical that transistor engineering understand the impact on junction profiles and spacing for ESD and other wearout mechanisms such as hot carriers. As gate oxide thicknesses are reduced, it is important that dielectric breakdown voltages are not exceeded before ESD devices turn on.

Unfortunately, the implementation of ESD protection is iterative. Capability of the process is characterized on test structures that provide design guides for protection circuitry. This approach, which relies on empirical results rather than using accurate simulation tools, does not allow for robust technology development.

Also limiting ESD issues has been the lack of consensual standards and test methods. Differences in tester capabilities and their calibration can result in different ESD threshold voltage values. Test methods also influence results, based on which combination of pins is selected for ESD testing.

Research Needs

These include the following:

1. Develop predictive methods that can be used to evaluate the impact of technology variation on the effectiveness of ESD circuits.
2. Develop better models and methods for predicting robustness of circuits under different test methods (HBM, MM, CDM) and the correlation between these techniques.
3. Develop methodology and design for circuits in submicron technologies that must operate in multivoltage environments.
4. Develop specifications for test equipment capability and calibration standards.

4.4 Multilevel Metal/Dielectric Integrity

Problem Statement

Aggressive scaling and increased performance requirements of semiconductor devices are producing the following results:

1. An increased number of metal interconnect layers will impose additional constraints to the selection of materials and their integration.
2. Smaller via/interconnect line feature sizes, often involving many different materials and interfaces within a 1μm3, will aggravate interface problems.
3. New materials such as Low k dielectrics and low resistance metals to achieve the projected performance targets are unlisted.

4. Increased die sizes and novel assembly options such as C4 may result in increased mechanical and thermal stresses.

Key Issues

Key issues include the following:

1. The impact of a high mechanical stress environments on the performance and reliability of silicon semiconductor devices.
2. The reliability of new dielectrics and low resistance metals as interconnects.

Research Needs

Research needs are as follows:

1. Improved experimental and modeling techniques for materials characterization (thin film mechanical properties and interface adhesion strengths) in the micron/submicron regime, including in and around vias.
2. Improved modeling of metal migration/void formation under thermomechanical stresses and thermomechanical/electromigration combined stresses.
3. Reliability of new dielectrics, low resistance metals under thermomechanical and current/voltage environments.
4. Improved experimental and modeling techniques to evaluate the intrinsic properties of packaging materials and their adhesion/interface properties among themselves and to the silicon die.
5. Modeling capability for the assembled package/silicon system, with focus on large die and advanced packaging methods, such as C4.
6. Basic understanding of thin film knowledge and its measurement.

4.5 Hot Carrier Injection (HCI)

Problem Statement

Aggressive performance requirements of MOS devices will require continual channel-length reduction and improved source-drain engineering. Even with simultaneous reduction in power supply voltages as devices scale down, hot carrier effect is most pronounced with the reduction of channel length and thinning of gate dielectric. Hot carrier effect can impact both device design and technology development as it lowers device current drive and thus limits device speed performance. Further, scaled technology will be sensitive to small drift in parameters.

Key Issues

Key issues are as follows:

1. Accurate hot carrier degradation modeling and simulations are critical, since overestimation of this effect can put unnecessary constraints on device design and prevent it from realizing its maximum speed potential, whereas underestimation of this effect can jeopardize device long-term reliability. Accurate modeling is essential to correlate wafer-level hot carrier reliability testing with actual operating conditions in order to optimize device performance without reducing device reliability.

2. The conventional Isub(max) measurement techniques are not sufficient. A unified, industrywide, built-in reliability approach is needed. If the impact of HCI-induced degradation is first observed during process development and product qualification, it will be too late. This information must be built into design libraries. Additionally, an industry-wide accepted technique is needed.

Research Needs

These needs include the folowing:

1. Correlate wafer level-hot carrier reliability testing with actual deep submicron device operating conditions at low power supply voltages (2.5 volts and below).
2. Establish common AC requirements for HCI.
3. Develop simulation models to account for the combined effects of, and coupling among, various hot carrier degradation mechanisms. (Should a new figure of merit be established?)
4. Establish design and processing rules and guidelines for hot carriers, with pertinent software tools to validate and check for adherence to these rules and guidelines.
5. The effect of HCI degradation on sub-0.3 μm PMOS devices over operating condition is becoming pronounced. As such, better understanding of HCI model for PMOS devices are needed.

4.6 Wafer Charging/Antenna Effects/Ultra-Thin Oxides

Problem Statement

Gate oxide and transistor scaling will require a better understanding and a reduction of the effects of process-induced charging damage. High power and high density plasmas, with the effects of such schemes as magnetic confinement, will only enhance the charging issue. Common processing steps such as plasma enhanced deposition, etching, ashing, and implantation may become significant contributors to wafer charging.

Key Issues

The charging concern is driven by two primary issues:

1. *Processing Issue*: Thin oxides are expected to be less tolerant to wafer charging. For example, if the poly (or contacting metal) charges to the point where the field in the gate oxide reaches 10 Mv/cm, severe damage can occur to the gate oxide. Table 2 indicates how ultrathin oxides will become less tolerant to charging.

Table 2 Effects of Charging on Ultrathin Oxides

Tox	Charging Voltage Required to Produce Severe Damage to Gate Oxide
200 Å	20 V
120 Å	12 V
90 Å	9 V
60 Å	6 V
45 Å	>4.5 V (1998-Roadmap)
35 Å	>3.5 V (2004 Roadmap)

2. *Design Issue*: The widely used design scheme for antenna protection (diode protection) is rapidly becoming ineffective. When the antenna ratio (area of thick-oxide/area of thin gate oxide) exceeds a critical value (~ 100/1), the designer must tie the gate to a diode for protection. The diode provides full protection (independent of polarity of charging) only if the diode in parallel with the gate oxide can break down before the 10 Mv/cm across the oxide is reached. For diodes that break down at 10 V, the diode can provide protection only for oxides >100 Å. Thus, for certain process steps, standard diode protection may not be sufficient protection for <100 Å gate oxides.

Research Needs

Research needs are as follows:

1. In situ equipment charging monitoring techniques
2. Novel charge neutralization techniques
3. Novel antenna protection design schemes
4. Magnetic confinement of plasmas (need for better understanding of physics)
5. Neutral beam etching (etch rate versus charging tradeoffs)
6. Uniformity of plasma etching versus charging tendency

4.7 Increase in Max Tj

Problem Statement

Current 100 MHz devices are expected to generate about 9 W at 3.3 V operating voltage. For a 150 MHz device, one would expect about 12.5 W at 3.3 V. If the operating voltage is lowered to about 2.5 V, generated power is effectively lowered to about 10.0 W, which still is higher than the previous generation (100 MHz at 3.3 V) by 1.0 W. Thus, one has a faster part at lower voltage while generating the same amount of power as the prior generation. With future technologies (projecting to year 2000), the number of transistors and frequencies will scale up, and both will induce increased power consumption; only voltage will be scaled down. Will voltage be reduced fast enough to control power consumption? No, judging by the simple example above, which did not even include an increase in the number of transistors.

Key Issues

Key issues are as follows:

1. Power generated will scale up faster with frequency than operating voltage can/will be reduced.
2. An increase in power means increased in Tj max. Device characteristics definitely would be impacted, as would diode breakdown voltages and (in the worst case) maybe even latch sensitivity. Designers would have to design the part over a wider temperature range.
3. Much more efficient thermal modules would be needed for power dissipation.

Research Needs

Research needs are as follows:

1. Research in chip/package manufacturing/design
2. Exploration of the use of finite element analysis to determine heat flow path in multilevel metallization structures
3. Study of the effect of increasing layer of metallization on Tj max, and the effect of self-induced heating of upper layers of metallization on electromigration

4.8 Soft Error/Single-Event Upsets

Problem Statement

The downward scaling of the power supply is expected to continue to be driven by improvements in the performance/power ratio. The susceptibility of memory circuits and internal microprocessor caches to single-event upsets/software errors is expected to increase dramatically with decreased Vcc.

Key Issues

Key issues include memory and logic considerations are as follows:

1. Memory devices depend on storing a charge in the cell during the writing operation sufficient to be reliably detected during the reading (sensing) operation. It is well known that ionization-producing charged particles such as alpha particles (emitted from trace amounts of uranium and thorium found in the ultra-large-scale integration [ULSI] or packaging materials) can induce charge loss in the cell (data state upset). More recently, it has been shown that cosmic rays (the high energy neutron component) can have a similar effect on memories. The latter mechanism is difficult to prevent and may enhance the need for error correction.
2. Although error detection/correction is common in memory systems, it may impose significant performance and/or density penalties for caches in microprocessors. Furthermore, aggressive scaling of Vcc, along with dramatic reductions in capacitance needed for very high speed logic operation, raise the question of the single-event upset/software error susceptibility of logic circuits.

Research Needs

Research needs are as follows:

1. Improved detection capability for ionizing particle emissions from ULSI and packaging materials. Detection capability of at least 0.001 alpha/cm2*hr is needed.
2. Improved physics understanding of soft error/soft error upset (SE/SEU) due to cosmic rays, modeling of such physics, and ideas for device hardness
3. Development of appropriate cosmic ray measurement techniques for acceleration factor determination
4. Improved methodologies for both accelerated and non-accelerated measurement of the SEU/SE susceptibility of memory and logic circuits
5. Development of efficient simulators to model SE/SEU and evaluate the susceptibility of specific circuits
6. Design (non-error correction) solutions for SE/SEU upsets
7. Materials solutions for SE/SEU upsets

4.9 Defectivity, Cleanliness

Problem Statement

Clean processes are key to developing and maintaining process control. They are critical to ensuring that wearout phenomena do not significantly occur during the useful life of the component and that defect densities are at acceptable levels. The projections for increased density, increased die size, and customer expectations of reduced reliability fallout all require an accelerated reduction in defect density.

4.10 Noise Margin/Coupling

Problem Statement

The reduction in the power supply, together with tighter timing requirements (performance improvement) and increased noise deriving from switching very high currents are expected to severely limit noise margins. Capacitive coupling between adjacent nodes also can have severe yield or reliability implications. Examples are signal crosstalk and device stressing at voltages that exceed the power supply.

4.11 Latch-up

Problem Statement

Scaling requirements commonly result in increased immunity to latch-up. The high increase in the on-chip currents involved may result in increased parasitic resistance voltage drops or increased impact ionization currents, potentially compromising latch-up immunity.

4.12 Leakage Isolation

Problem Statement

Attempts to reduce transistor leakage currents in the subthreshold regions can be effected by silicon reliability mechanisms such as HCI. In particular, changes in parameters such as drain

current in off state (Idoff) need to be modeled and understood in terms of carrier trapping and interface trap generation.

4.13 Tools for Reliability Checking

Problem Statement

Tools based on modeling of failure mechanisms such as HCI, electromigration (EM), TDDB, etc., should be available for reliable use of future CMOS transistors and interconnect schemes. Rapid identification is required for situations where use conditions exceed reliable operation.

4.14 Package Induced Failures

Problem Statement

Mechanical and thermal stresses due to coefficient of thermal expansion (CTE) mismatches between mold compounds and silicon can impact chip functionality and performance. Appropriate mechanical models need to be developed to account for interactions between the package and silicon.

4.15 Cost Effective Reliability and Qualification

Problem Statement

Rapid introduction of new technologies is increasing time pressure on qualifying processes that meet reliability requirements. Given the higher cost of manufacturing at this introduction phase, material costs (especially in finished die form) contribute significantly to the overall cost of qualification. New methodologies and approaches need to be developed that not only reduce overall qualification costs, but also meet timelines for technology introduction.

4.16 Mixed Signal Requirements for Transistor Matching

Problem Statement

The required mix signal output is dependent on multiple transistors being matched with the appropriate characteristics. Models should be developed that accurately predict output behaviors based on nonlinear transistor characteristics.

4.17 Performance/Power/Reliability Tradeoffs

Problem Statement

At a constant voltage, performance increases at the expense of increased power and reduced reliability. Tools should be developed to help assess potential process changes in terms of transistors and interconnect performance, chip power dissipation (and temperature increase), and increased contribution of failure mechanisms (e.g., HCI, TDDB, latch-up, etc.) to overall chip reliability.

4.18 Key Project Proposals

Project Summary

Project Name*:* Reliability Of Thin Oxides in Direct Tunneling Regime

Project No.: TBD

Thrust: TBD

ST & Sandia Project Leaders: TBD

Summary of Problem and Alignment with the National Roadmap

The National Roadmap shows that the thickness of gate oxides will decrease to 4.5 nm in 1998 and to 3.4 nm in 2004, with sustained electric field increasing to over 5.0 MV/cm. Both requirements will lead to failure regimes (direct tunneling will be first) of which little is known. Therefore, there is a strong need to study the reliability implications so that the true cost of making these changes can be predicted.

Approach

To meet the need for predicative reliability models in these new failure regimes, this project will address the following:

- Industry will produce side-by-side capacitors (with different areas), transistors and standard evaluation circuits with oxide thickness between 6 and 3 nm.
- Sandia National Laboratories will characterize the defect level, wafer-level reliability (WLR) and long-term TDDB, transistor stability and HCI.
- Sandia will develop a statistical model and a field acceleration model from the data.
- Industry will perform life tests on corresponding standard evaluation circuits (SEC), and results will be compared with the test structure data.

Project Objectives and Benefits

These are as follows:

- Identification of any new failure models, or discontinuities in existing failure modes, resulting from the transition from direct substrate to gate tunneling
- Fast, meaningful, standardized methods to qualify the reliability of thin oxide processes
- Predictive oxide reliability models that will allow maximizing performance by confidently reducing reliability safety margins
- Ability to benchmark oxide reliability

Table 3 Project Overview: Reliability Of Thin Oxides in Direct Tunneling Regime

Objective	Task	Performance Metrics	Deliverables	Due	$K
1. Characterization of thin oxide capacitors	1. Industry supplies capacitors with multiple thickness	Capacitor with oxide thickness of 6 nm, 4.5 nm, and 3.4 nm	SEMATECH companies supply capacitors	+6 mo from start	
	2. Characterization at Sandia of supported capacitors	1. CV, V Ramp, TDDB measurements 2. Failure analysis of failed capacitors	Sandia documents results	+12 mo	
	3. Data analyzed by Sandia	1. Gate current vs. field 2. TDDB distribution 3. WLR to TDDB	Sandia documents results	+15 mo	
2. Transistor reliability	1. Industry supplies transistors splits processed with capacitors	Transistors with different oxide thickness	Capacitors/ transistors manufactured by SEMATECH member companies	+6 mo	
	2. Sandia performs pre-stress transistors characterization	1. Transistor characterized 2. DC stressing of transistors	Sandia documents transistor characterization	+12 mo	
3. Industry evaluation of long term reliability of corresponding Standard Evaluation Circuit	1. Process SEC on same wafers with transistors and capacitors	SEC circuits with different oxide thickness	Industry processes SEC	+13 mo	
	2. Do long-term life test	Test circuits	Document results	+24 mo	
	3. Failure analysis on all failures	Failure modes identified on circuits	Document results		
	4. Correlate with failure rates and failure types fund in transistors and capacitors	Correlated SEC data with capacitor and transistor data	Document correlation	+24 mo	
				+24 mo	

Objective	Task	Performance Metrics	Deliverables	Due	$K
4. Developing predictive models	1. Modeling of gate current leakage 2. Modeling of TDDB 3. Modeling of HCI and transistor instabilities	Gate current model developed TDDB model developed HCI model developed	Document gate current leakage models Document TDDB model Document HCI model	+30 mo +30 mo +30 mo	
5. Development of rapid standardized thin oxide reliability qualification	1. Specification of test structures 2. Specification of test method 3. Specification of data analysis	Test structure designed Test method developed Data analysis procedures developed	Document details of oxide reliability test structures Document test methods of oxide reliability rest structures Document data analysis procedures for oxide test structures	+36 mo +36 mo +36 mo	
Universities, suppliers, partners and dependencies: $1050K total					

Project Summary

Ratification date: 1995 SETEC (EDSC) statement of work (SOW)

Rev. date: N/A

Project Name: CAD Reliability Assessment Tools for Electromigration

Project No.: TBD

Thrust: TBD

SEMATECH & Sandia Project Leaders: TBD

Summary of Problem and Alignment with National Roadmap

There are serious gaps in CAD tools for product design because they do not adequately simulate the effects of failure mechanisms. As a result, product designs cannot be evaluated adequately and optimized for electrical and reliability performance. Needed are tools to simulate and evaluate the impact of design on changes in the electrical performance of the product due to the effects of failure mechanisms that occur with product use.

Approach

Develop/evaluate methodologies for CAD tools to determine the implications of circuit-design selections on the timewise degradation of product performance. Calculate electrical performance changes with time of circuit units (considered individually and in interaction with others) and of the product. Accomplish this by using predicted resistance increases with time of interconnect lines and vias in circuit units considering 1) current-densities expected for currents required by the circuit and linewidths selected and 2) calculated operating temperature, which includes the effects of joule heating in the circuit element and in other metal levels.

Project Objectives and Benefits

Objectives:

1. Develop and validate both AC and DC electromigration models
2. Develop methodologies for evaluating context-specific designs rules sensitive to the effects of DC and AC electromigration models
3. Standardize tools to include reliability considerations in product designs
4. Save costs by developing designs that optimize product performance and reliability

Table 4 Project Overview: CAD Reliability Assessment Tools for Electromigration

Objective	Task	Performance Metrics	Deliverables	Due	$K
1. Develop and validate both AC and DC electromigration models					
2. Develop methodologies for evaluating context-specific designs rules sensitive to the effects of DC and AC electromigration models					
3. Standardize tools for including reliability considerations in product designs					
4. Save costs by through ability to develop designs that optimize product performance and reliability					
Universities, Suppliers, partners and dependencies:			**Total:**		

5 IC PACKAGING TECHNOLOGY ISSUES/CONSTRAINTS

5.1 Introduction

Worldwide demand will continue for electronics systems that perform a variety of functions, such as information management, telecommunication, control, etc. Emphasis will accelerate on faster, smaller, lighter and especially cost-effective systems to perform these functions.

The result will be a continued drive for smaller, more effective and efficient semiconductors and for improved methods of semiconductor packaging and semiconductor device-to-board attach methods. For example, current silicon design capabilities are reportedly in the picosecond range, whereas equipment system (computer) capabilities are reportedly in the nanosecond range. To handle market demands and the gap in silicon vs. package technologies, two approaches have emerged for handling the semiconductor device-to-system substrate interface. These include direct chip-to-board attach (DCA) or chip-on-board (COB) and smaller, more varied (application optimized) semiconductor die packages (i.e., chip scale packaging [CSP]). The advent of known good die (KGD) has led to renewed interest in DCA and COB and has effectively transferred these packaging reliability issues to the original equipment manufacturer (OEM).

Packaging is going through a revolutionary change, from overmolded leadframe-based packages to nonmolded or partially molded ball grid array (BGA) and chip scale package (CSP)-type packages. The materials are significantly different from those that the industry has spent years developing. Therefore, it is expected that there will be an initial increase in the package failure rate until the industry moves down the learning curve.

In reviewing semiconductor reliability, two general and four specific issues have been identified as challenges/constraints for package reliability by year 2000. General issues include 1) reliability expectations in customer use environments and 2) tools for package reliability analysis. They are thought to affect the following specific issues:

1. Integrity of organic interfaces after thermal, humidity, or mechanical stress
2. Integrity of first-level package interconnections (chip-to-package internal connections) after thermal, humidity, or mechanical stress
3. Integrity of second level package interconnections (package-to-board connections) after thermal, humidity, or mechanical stress
4. Modeling for age, wearout, and correlation to environmental stress

5.2 Reliability Expectations In Customer Use Environments

Problem Statement

Customer expectations for the reliability and robustness of IC products are continually being raised, consistent with the concept of continuous improvement. For example, many customers are now requesting a minimum level 2 moisture sensitivity (popcorning), as defined by the Joint Electron Device Engineering Council (JEDEC). At the same time, some external environments to which ICs are exposed are becoming more varied, and in some cases more extreme. For example, in soldering components to a printed circuit board, 220°C is the most frequently specified peak temperature for vapor phase and/or infrared reflow methods. However, customers have expressed a strong desire to use temperatures up to 245°C. Their rationale is that printed circuit boards contain both large and small components, and that to get the largest components hot enough to

solder, the temperature of the smaller often must exceed the 220° JEDEC specification. The higher soldering temperature directly conflicts with the desire for a higher level of popcorning resistance.

An example of changing environmental conditions in product use is the widespread use of portable equipment such as cellular telephones. In actual operation, these devices generally are used in “human-compatible” environments. However, while not in use, they often are left inside automobiles where temperature excursions of over 20-40°C a day are possible. Such temperature excursions are not common for equipment that remains in office or home environments. Portable equipment, such as cellular telephones, laptop PCs and palmtops, also are subjected to power cycling much more frequently than desktop PCs and workstations, resulting in increased power cycling stresses. Furthermore, many products, in becoming more environmentally friendly, have “power down” modes to save energy, which also increases power and temperature stresses on integrated circuits.

Integrated circuits are being used more extensively in automotive under-hood applications where temperature excursions can exceed 100°C (even during circuit operation), and humidity can vary widely. Similar or more extreme conditions can occur in military applications. In the drive to reduce package costs, the plastic package is slowly replacing the ceramic package in many automotive and military applications. The military also wants to purchase more commercially available circuits, which are most often packaged in plastic. Plastic packages thus can be expected to eventually meet more extreme environmental conditions, which will present particular challenges for plastic package robustness.

As ICs become more complex, larger dies and larger packages with higher pin counts will emerge. Depending on package construction, this could lead to more stress on the die attach, more delamination, more fatigue on corner leads, and warpage. For all packages, it could result in fatigue on the solder balls. This will exacerbate package stresses under the more stringent environments noted above.

Key Issues

These issues are as follows:

1. Understanding is needed of the actual requirements for product robustness as a function of customer use conditions. For example, it may be desirable to have different specifications on products, depending on the environmental extremes that they receive in the end product.
2. Materials properties (e.g., expansion coefficients, resistance to moisture) may not meet some customer environmental requirements.

Research Needs

It will be necessary to design accelerated tests that correlate with field environmental conditions, and to develop acceleration models for these tests.

5.3 Tools For Package Reliability Analysis

Problem Statement

The need to suppress delamination of critical interfaces within IC packages is well recognized, yet most process development and selection efforts are not designed experiments. End-of-line measurements are used to see whether and where the package has delaminated after various stresses. The ability is needed to predict and verify performance derived from fundamental materials properties, geometry and physics-based models. Performance predictions and measurements must be quantitative so that it is possible to assess and maximize margin vs. requirements. Bulk and interfacial fracture mechanics parameters are lacking for many key material combinations and are limited by finite element analysis (FEA) models based on linear stress vs. strain rather than fracture mechanics principles. Furthermore, good adhesion measurement tools and the standards to prove reproducibility are not available. Until interfacial strength predictability and short-loop diagnostic testing are available, optimizing package performance in a timely fashion will be very difficult.

Key Issues

1. Materials data is insufficient for the following:
   a. Strength, modulus & Tg (glass transition temperature) measurement and variance with time for all properties (viscoelastic)
   b. Stress/strain vs. temperature, humidity and strain rate, especially for thin films
2. Variation of moisture concentration with depth is generally ignored.
3. Relative activity of bulk vs. interfacial moisture transport is unknown.
4. Thin film strength, ductility and thermal measurement techniques are not widely developed and deployed.
5. Fault isolation techniques are needed.

Research Needs

These needs are as follows:

1. Characterize potential measurement tools, including
   a. High frequency scanning acoustic microscopy (SAM)
   b. High resolution X-ray (plus tomography) and laminography
   c. High resolution Moire interferometry
   d. Imaging techniques for defects using scanning electron microscopy (SEM), acoustic, infrared (IR), etc.
   e. In situ imaging of crack propagation under stress
2. Establish adhesion measurement standards.
3. Characterize electrical test structures to provide unique signatures for assembly/packaging issues.
4. Characterize viscoelastic properties and models for relevant packaging materials.

5. Improve destructive physical analysis (DPA) techniques (i.e., deprocessing to isolate lethal fault site[s])

5.4 Integrity of Organic Interfaces After Hermal, Humidity, or Mechanical Stresses

Problem Statement

Components of current and future IC packages are brittle silicon die, metal conductors and plastic composite materials. Interfaces of these different materials experience high levels of stress from thermal mismatch, poor heat dissipation and moisture degradation, which may result in loss of integrity during operation or following environmental stressing. Bulk properties of more mature packaging components may be known and somewhat predictable, the interfaces are poorly characterized and are the initiation point of delamination and fracture.

Failures associated with poor interfacial integrity are package cracking during surface mount, and/or delamination during thermal stressing. The resulting reliability issues of interfacial failure may be openings or shorts in the conductors, parametric shifts, ingress of contamination with leakage, fatigue of interconnects, or unpredictable thermal performance.

Some interfaces where delamination negatively impacts reliability are encapsulating plastic compound to die, lead frame, first level interconnection (wires or flip-chip bumps), package substrates or heat spreaders. Other areas of concern are as follows:

- Die attach material to die and or die paddle
- Composite materials (resin separation from fillers)
- Package substrate laminates, vias and conductors
- Underfills to flip-chip bumps, die coats and substrates
- Warpage and bending affecting planarity or causing shifts in properties

As the evolution to more complex multilayer organic packages continues, it is necessary to understand generically the stresses applied, strengths of materials, and fundamentals of adhesion to assure packages that meet the requirements of semiconductor applications.

Key Issues

These issues are as follows:

1. Prediction of stresses exerted by materials of the IC packages under environmental conditions and the strength of the bulk materials and interfaces
2. Effect of voids and delamination on reliability of the product
3. Effect of surface chemistry and morphology on adhesion
4. Crack propagation

Research Needs

These needs are as follows:

1. Materials properties data: CTE, modulus, strength, fatigue life and creep
2. Interfacial strength of material couples as a function of surface and adhesive
3. Degradation mechanisms at interfaces
4. New materials to support IC packaging applications

5. Models to predict interfacial behavior
6. Standardized test methods for accurate materials characterization

5.5 Integrity of 1st Level Package Interconnection (Chip-To-Package Internal Connection) After Thermal, Humidity, or Mechanical Stresses

Problem Statement

Die and package geometries are shrinking and area ratios are becoming smaller. Alternative package designs (such as chip scale packaging) are placing ever-increasing demands on the die-package interconnect or, in the case of direct chip attach, die-substrate interconnect. The situation is aggravated by customer requests to withstand harsher external environments.

Die shrinks lead to tighter pitches; while a 100 μm pad pitch currently can be wire bonded in production, the packaging roadmap indicates 70 μm will be a production requirement by the year 2000. Fine pitch wirebonding requires thinner wire and a smaller bonded interface. The wires will be closer, weaker and more likely to be displaced by the encapsulant during the molding operation.

Below 70 μm it is likely that wire bonding will be replaced by either tape automated bonding (TAB) or flip-chip. Although both technologies are in limited use today, widespread acceptance will require more detailed reliability studies of lower cost processing alternatives, such as electrodeposited (vs. evaporated) solder for flip-chip structures. Additionally, flip-chip attachment to organic substrates requires underfill. Interfaces at the underfill to solder, silicon and substrate need to be better understood, especially in relation to the distance from the neutral point and after thermal and/or humidity stress conditions.

Copper metal may be used as an alternative to aluminum to enable higher on-chip current densities. While the chemistry and kinetics of aluminum corrosion in microcircuits has been well studied, corrosion of thin copper-doped films is less well understood. Additionally, information will be required on the stability of the interconnect-copper interface under conditions of temperature, humidity and mechanical stress.

Key Issues

These issues are as follows:

1. Interaction of the interconnect materials with the top metallization and adjacent passivation
2. Integrity (intermetallic enbrittlement, Kirkendall voiding, etc.) of the intermetallic system
3. Movement of the interconnect induced by the molding compound
4. Effect of residual contaminants on the die and from the encapsulant
5. Scaled-down interconnect joints approaching minimum strength to withstand stress induced by the encapsulant.
6. Attachment of large chips to an organic substrate requiring a better understanding of the effect of TCE mismatch on the selection criteria between direct chip attach (flip-chip) or chip on board (wire bond)

Research Needs

These needs include the following:

1. Thermomechanical models that relate the effect of reducing bonding pitch on reliability
2. Development and verification of models that address the effect on reliability of flip-chip underfill materials, adhesive failure and manufacturing defects (e.g., voids)
3. Standardized design rules for features on test chips that will measure/rank the reliability of interconnect systems
4. Models for the molding operation to help establish design limits for fine pitch wirebonding, TAB and flip chip
5. Model verification studies
6. First level interconnect-copper studies on corrosion mechanisms and interfacial reliability

5.6 Integrity of Second-level Package Interconnection (Package to Board Connection) After Thermal, Humidity or Mechanical Stresses

Problem Statement

The emphasis on faster, smaller, lighter and more cost-effective electronic systems will continue to drive the search for alternate approaches to semiconductor packaging and assembling of electronic systems. As a result, the current trend toward for increased use of DCA and smaller, more optimized chip packages will continue.

Direct chip attach methods present very similar problems to those encountered when considering first-level intermetallic interfaces integrity (see above). However, they are further aggravated by repeated process steps required for the attachment of additional components and the presence of a greater number of materials, than when encapsulating single semiconductor chips.

In the case(s) where a semiconductor device is packaged, the interfaces to the system board present new challenges. Narrower spacings (pitch, etc.) and type of leads (ball vs. pin vs. ribbon, etc.), necessitate different manufacturing methods and have different reliability characteristics. The great variety of packages (see National Roadmap's Packaging Roadmap), each with its own shortcomings on moisture exposure, thermal, mechanical and other stresses, present new challenges. These challenges include the need to perform more evaluations/characterizations, plus the need for new tools to make these evaluations.

Key Issues

These issues are as follows:

1. Reduced chip and package geometries result in reduced spacing (pitch, etc.) for both DCA and packaged chips assemblies. This high density condition makes it easier for fatigue, corrosion and other degradation failures to occur. These issues are further complicated by the type of package leads (micropins, balls, ribbons, etc.)
2. Heat removal from high density boards becomes more difficult. The result is higher thermal gradients in multilayer boards, multichip modules, etc. Higher temperatures make it easier for failures to occur.

3. Reduction in spacing may result in degradation of performance and reliability. Smaller amounts of residue from board assembly processes are sufficient, in the presence of higher electric fields, for metallic migration, corrosion, etc., to occur.
4. Thermomechanical stresses and residues from multiple assembly processes, required to attach different components, create circumstances for degradation of performance and subsequent failure. For example, mechanical stresses (bending) cause warpage and other piezoelectric effects that may lead to failures.

Research Needs

These needs include the following:

1. Thermomechanical models that relate the effect of reduced node pitch (pad, etc.), new interconnect materials and methods, on reliability. These needs exist for DCA methods as well as packaged chip board assembly (e.g., pitch vs. solderability, vs. metallic migration, etc.).
2. Development and verification of models that address the effect on reliability of underfill materials, adhesive failure and manufacturing defects (e.g., voids) for both DCA and packaged chip board assembly.
3. Thermal management models and enhancement methods/techniques, e.g., heat spreading/sinking materials and methods that promote thermal management and failure avoidance.
4. Thermomechanical methods and models for strategic component placement on system boards (proper board architecture). These methods (design rules) should help minimize thermomechanical stresses encountered during manufacturing and equipment use (i.e., device to board attach processes such as IR, bending, warpage stresses during manufacturing, and subsequent equipment assembly and use).

5.7 Modeling for Age, Wearout, and Correlation to Environmental Stress

Problem Statement

To meet demands for increased electrical and thermal performance, packaging is employing new materials such as organic substrates and liquid encapsulants. These materials and the interfacial surfaces joining them may not be capable of meeting current Mil Std/JEDEC-based reliability stress requirements. Historically, the semiconductor industry has relied on Mil Std and JEDEC-based reliability testing to ensure robust field performance for both severe and commercial markets. The transition to organic-based packaging provides an opportunity to reevaluate these standards and generate reliability models based on current and expected market use segments, such as communication, office automation, and automotive. Failure to provide these data could result in a plethora of differing requirements based on the needs and capabilities of individual manufacturers and suppliers.

Key Issues

These issues include the following:

1. Consolidation of environmental requirements for various market applications
2. Generation of materials characterization data for use in models
3. Fundamental interface property identification

4. Availability of tools for interface integrity evaluation
5. Lifetime predictions based on failure and defect mechanism

Research Needs

These include the following:

1. Models to predict the onset of interface delamination from thermal, mechanical, and moisture stress
2. Molecular modeling of moisture diffusion and degradation in organic materials
3. Probabilistic and fatigue modeling for various use and stress conditions
4. Tool development for interfacial integrity evaluations
5. Evaluation of bulk organic material characteristics under specific stress conditions

5.8 Modeling for Age, Wearout, and Correlation to Environmental Stress

Problem Statement

To meet demands for increased electrical and thermal performance, packaging is employing new materials such as organic substrates and liquid encapsulants. These materials and the interfacial surfaces joining them may not be capable of meeting current Mil Std/JEDEC-based reliability stress requirements. Historically, the semiconductor industry has relied on Mil Std and JEDEC-based reliability testing to ensure robust field performance for both severe and commercial markets. The transition to organic-based packaging provides an opportunity to reevaluate these standards and generate reliability models based on current and expected market use segments, such as communication, office automation, and automotive. Failure to provide these data could result in a plethora of differing requirements based on the needs and capabilities of individual manufacturers and suppliers.

Key Issues

Key issues include the following:

1. Consolidation of environmental requirements for various market applications
2. Generation of materials characterization data for use in models
3. Fundamental interface property identification
4. Availability of tools for interface integrity evaluation
5. Lifetime predictions based on failure and defect mechanism

Research Needs

These are as follows:

1. Models to predict the onset of interface delamination due to thermal, mechanical, and moisture stress
2. Molecular modeling of moisture diffusion and degradation in organic materials
3. Probabilistic and fatigue modeling for various use and stress conditions
4. Tool development for interfacial integrity evaluations
5. Evaluation of bulk organic material characteristics under specific stress conditions

6 SILICON DESIGN TECHNOLOGY CONSTRAINTS

6.1 Overview

Future technologies will produce larger, more complex, higher-performance chips. Advancing technology means increased densities, smaller geometries and higher speeds, which will make circuits more susceptible to noise and crosstalk. More advanced technologies mean new challenges in meeting the ESD/latch-up requirements of new applications. Each reduction in feature size and spacing dimensions brings a new set of limitations and the challenge of overcoming them.

At the same time, customer expectations are growing for quality, early life reliability, and long-term life reliability. It will be imperative to address quality and reliability during the design phase in order to meet customer expectations.

An advance in capability of design tools, models and methodology is required if the industry is to stay on the leading edge of reliability. Tools are required to simulate the failure mechanisms of concern. Modeling work is needed for such mechanisms as hot carrier, electromigration, latch-up, ESD, electromagnetic interference (EMI), contact and via, antenna effect, crosstalk, resistance/capacitance (RC) delays, oxide life, etc.

The advancement of technology and customer quality and reliability requirements will make accuracy of design models and tools a critical area of concern. Models not only need to be formatted and the resulting parameters derived, they also must be verified continually throughout the design and manufacturing process. Only in this way can long-term reliability of the final product be assured.

Improving quality on the larger chips requires improvement in test coverage. This will require continued development of advanced design for test techniques and standards. This will include requirements for standardized (or dedicated) pins, built-in self test (BIST) for array and logic, and boundary scan chains for reduced pin count during test and burn-in. Mixing analog with digital on the same substrate could increase these requirements. The minimization of DC leakage will enable the use of I_{DDQ} techniques. Diagnostics will be necessary to facilitate failure analysis and corrective actions on defects.

Since early-life reliability defectivity can be expected to track defect density, improving early life reliability on larger chips can be expected to require an improvement in burn-in effectiveness. Designing chips to be more thoroughly exercised during screening, able to withstand higher voltage and thermal acceleration, or support new screening techniques (e.g., I_{DDQ}) will be required.

Long-term product reliability will require assurance that wearout mechanisms do not significantly contribute to the failure rate within a product life. Wearout mechanism must be managed by design ground rules, yet pushing clock frequencies and performance may limit how much margin can be afforded in the ground rules. More sophisticated wearout models may be required.

Table 5 Prioritized Matrix of Silicon Design Technology Constraints

Item	Company					
	A	B	C	D	E	F
1. Accuracy of design models (7)	2	2	1	3	1	1
2. Design tools/methodology (6)	1	3	2	1	2	2
3. Noise/crosstalk/latch-up (3)	6	1	3	4	5	3
4. Design for testability (4)	4	4	8	2	4	4
5. Low I_{DDQ}(9)	8	9	4	7	3	5
6. Design for burn-in (5)	5	7	10	6	7	6
7. Die level burn-in (2)	3	6	11	11	8	7
8. ESD 4KV min (1)	11	5	6	14	6	8
9. Low voltage (10)	7	13	5	16	12	9
10. Design for speed test (13)	13	10	12	9	9	10
11. Routing >150K gates (17)	14	8	16	5	11	11
12. Soft error rate (8)	10	15	13	8	13	12
13. Intradie variation (16)	9	11	14	12	17	13
14. Decoupling caps (15)	16	14	15	10	16	15
15. Cost effectiveness (14)	17	17	7	17	15	16

6.2 Discussion of Silicon Design Technology Constraints

6.2.1 Constraint #1: Accuracy of Design Models and Tools

Advancement of technology will continue to make this a critical area of concern. Models not only need to be formatted and the resulting parameters derived, they also need to be verified continually throughout the design and manufacturing process. Only in this way can long-term reliability of the final product be assured. By doing this, an adequate database will be acquired to assure the continued integrity of results from tools used in the design methodology.

Key Issue/Research Opportunity

Advancement is needed in device physics modeling and related parameter extraction methodology.

6.2.2 Constraint #2: Design Tools and Methodology

An advance in capability of design tools, models and methodology is required if the industry is to stay on the leading edge of reliability. Tools that simulate the failure mechanisms of concern are required. Modeling work is needed for such mechanisms as hot carrier, electromigration, latch-up, ESD, EMI, contact and via, antenna effect, crosstalk, RC delays, oxide life, etc. Work also is required in checking software for the same mechanism to close the loop in the design process. Low power/low voltage is the direction of future technologies. At lower voltages with smaller device widths, drivers have less capability. Bigger ICs with longer interconnect lengths will present larger loads to these less-capable drivers. The overall design objective still will be higher

performance. The design process, with its tools and methodologies, needs to address the reliability issues inherent in this combination of contradictory requirements and capabilities. Such items as HCI, time-dependent dielectric breakdown (TDDB), ESD, crosstalk, etc., must be addressed in the design process.

Key Issues/Research Opportunities

These issues and opportunities include the following:

1. Modeling work on failure mechanisms and related software tools to enable incorporation of these modeling capabilities into the design methodology
2. Mix-signal design tools and methodology integrated with digital tools

6.2.3 Constraint #3: Noise/Crosstalk-Inducing Latch-up

Advancing technology means increased densities, smaller geometries, and higher speeds that will make circuits more susceptible to noise, crosstalk and induced latch-up. The design process, with its associated tools and models, must address the layout issues of power, ground and signal relationships, simultaneous switching, and the creation of parasitic devices to minimize exposure in the areas of concern.

Key Issue/Research Opportunity

Work is needed to understand field effects and transmission line effects as applied to sandwich metal structures, thinner lines, thinner interlevel metal (IM) dielectrics and the related planarization issues, and lower voltage drivers for bigger die to meet higher performance requirements and techniques for reducing noise, crosstalk, and interaction among various mix-signal blocks.

6.2.4 Constraint #4: Design for Testability

Leading-edge technologies will continue to require the development of advanced design for test techniques and standards. This will include requirements for standardized (or dedicated) pins, BIST for array and logic, and boundary scan chains for reduced pin count during test and burn-in. Any analog mixed with digital on the same substrate could increase these requirements. The minimization of DC leakage will enable the use of I_{DDQ} techniques. Diagnostics will be necessary to facilitate failure analysis and corrective actions on defects. Some layout constraints might be required to facilitate any intra-circuit probing for which plans are being made.

Key Issues/Research Opportunities

These include the following:

1. New approaches on automatic test generation. Methods are needed to test circuits for application and capability, especially for test generation. Design methodology then should be tied into the new automatic test pattern generation (ATPG)
2. Design for testability for analog, boundary scan for analog, and mix-signal
3. A new approach to reduce test development effort, incorporating modular, reusable integration of existing blocks

6.2.5 Constraint #5: Low I_{DDQ}

Low I_{DDQ} has been used as a first screen for defects. To facilitate this, the design process needs to result in a circuit that has a low I_{DDQ} state. Otherwise, this test will not apply.

Key Issue/Research Opportunity

Improvement is needed in design for testability to give better control of establishing a low power state which addresses the maximum amount of active circuitry. This becomes more important as power-down sequences become more prevalent.

6.2.6 Constraint #6: Design for Burn-in

The demand for lower failure rates requires the use of burn-in on many products. The design process (methodology and tools/models) must assure functionality across the entire circuit at the expected burn-in conditions. With more robust designs, burn-in can be enhanced. Use of standard pins, boundary scan chains, BIST, and minimal DC leakage will facilitate both burn-in and screening.

Key Issues/Research Opportunities

These are as follows:

1. Design methodology, tools and models ensuring functionality at burn-in condition
2. Alternative methodology to burn-in, especially for high pincount devices
3. Replacement of traditional burn-in with other approaches

6.2.7 Constraint #7: Die level Burn-in

Burn-in is required on many products to meet the required failure rates. The design process (methodology and models) must assure that the product is functional at the burn-in conditions to be efficient and to minimize the amount of product that escapes burn-in.

Key Issues/Research Opportunities

These include the following:

1. Develop methodology for die level burn-in prior to packaging.
2. Develop approaches to identify defective subpopulations to eliminate the need for product burn-in after initial introduction
3. Develop alternative methods to burn-in, especially for high pin count devices

6.2.8 Constraint #8: ESD 4KV Minimum

More advanced technologies mean new challenges in meeting the ESD/latch-up requirements of new applications. Each reduction in feature size and spacing dimensions brings a new set of limitations and the challenge to overcome these limitations. In addition, the industry is moving to a higher level (4KV) of required protection in HBM and new requirements for CDM. Meeting these levels means new techniques and more stringent design controls. Input capacitance of ESD structure (C > 1pF) degrades signal integrity for analog/mix-signal high frequency circuits (3-5 GHz). The problem is circuit-dependent .

Key Issues/Research Opportunities

These include the following:

1. Better understanding of the device physics of ESD phenomena as the industry moves to 0.25 μm and below, and development of modeling and simulation tools
2. Advancement in equipment used to simulate the ESD event; this includes new probes and pulse sources, and understanding of their interactions for all categories (HBM, CDM, MM)

6.2.9 Constraint #9: Low Voltage

Advanced technologies, with their tighter geometries and new structures, are driving the need for lower operating voltages and low device leakage. Requirements for lower power and higher speed in more and more applications are also driving this need. Better understanding is needed in how all factors affecting reliability scale with other requirements and changes in circuit structures. The resulting models will require continuous attention.

Key Issue/Research Opportunity

Advancement in modeling techniques applicable to finer scaling (0.25 μm and below) will be seen at lower voltages. How do scale factors work as deep submicron geometries are approached?

6.2.10 Constraint #10: Design for At-Speed Test

It would be desirable to test circuits at their designed-for operating speeds or the inherent limits of the silicon, whichever is faster. In general, this would require much advanced development in testers and associated handling hardware. Improvements in the design process to address “design for testability” will facilitate meeting this objective by increasing the access to speed critical portions of the circuit.

Key Issue/Research Opportunity

The relationship (and correlation) between at-speed testing and critical-path testing needs to be better understood as it applies to the more advanced technologies faced in the National Roadmap time frame. An example is if all critical paths are accessible due to design for testability and there is correlational assurance through adjacent transistors and long-running parallel lines.

6.2.11 Constraint #11: Routing for Maximum Reliability for Large Blocks

Routing algorithms for increasing levels of density are an area of concern. Many reliability issues (crosstalk, metal migration, long-wires, etc.) are addressed as part of the routing phase of the design process. All larger circuits are straining their ability to address these issues at this point in the design process. Just handling the resulting database can be a major problem. Certainly, more advanced methods of modeling the problems would be an improvement. Other ways to improve this problems are needed. There is concern that the inability to handle the task could actually introduce unforeseen failure mechanisms.

Key Issue/Research Opportunity

Advance the ability to handle reliability issues (crosstalk , interaction, etc.) for large blocks.

6.2.12 Constraint #12: Soft Error Rate

Soft errors are increasing with decreasing of storage charge. This error rate also is increased with elevation such as air travel. It will be necessary to address this concern during the design of the chips and systems. Cell sensitivity to ionizing radiation can be modeled and verified with accelerated testing and/or life testing.

Key Issue/Research Opportunity

It is necessary to enhance understanding in all circuit design simulation tools, and perform verification with accelerated testing and/or life testing.

6.2.13 Constraint #13: Intradie, Interdie Variation

The progression toward larger die sizes, higher density and smaller ground rules magnifies the effect of intradie variation. Planarization techniques cause variation in dielectric thicknesses, which are layout-dependent. Huge die sizes introduce variation in critical dimensions during photoprocessing. The impact of variation on capacitance and other parameters must be modeled and understood.

Key Issue/Research Opportunity

Advancement is needed in the ability to model the impact of variations introduced in processing.

6.2.14 Constraint #14: Decoupling Capacitors

The increasing density and speed of future technologies require liberal use of decoupling capacitors. The area occupied by these capacitors represents a significant fraction of total die area, which introduces a heightened product reliability risk from gate oxide defects. Since the functionality of decoupling caps is affected less by oxide leakage than by transistors, new reliability models are needed.

Key Issue/Research Opportunity

Advancement is needed in the ability to model capacitor placement for optimum performance and reliability (high-frequency effect, latch-up, multiple drain-drain voltage (VDD) pins, etc.)

6.2.15 Constraint #15: Cost Effectiveness

The advancement of technology toward larger chips and smaller, more complex circuits means greater difficulties in testing, handling, and packaging. Combining the higher cost of processing with the greater expense of manufacturing the final die/package assembly results in a cost-effectiveness issue. New methodologies, new tools, and new approaches to these and related issues may be required.

Key Issue/Research Opportunity

Development of advanced cost models is needed to deter increased costs through inclusion of design for quality and reliability.

7 TEST, DIAGNOSTICS, AND FAILURE ANALYSIS TECHNOLOGY CONSTRAINTS

7.1 Introduction

The development of reliability, testing, and failure analysis solutions is lagging the rapid advancement of microelectronics technology. Tools and techniques are not available to ensure the reliability of the next generation of ICs. Future technologies will require development of advanced test and diagnostic techniques. These improvements in test coverage and diagnosability may include logic BIST, array BIST, on-chip clock generation, reduced pin count techniques, signature analysis, and defect class structural testing. Key issues include diagnosability and failure analysis, test coverage, application vs. test program correlation, self test, and I_{DDQ} testing.

Failure analysis and diagnosability are considered particularly critical as enabling capabilities for identification and resolution of anticipated acute and chronic problems for new technology yield and reliability. Major areas of concern for the next-generation ICs include oxide and interconnect reliability.

For example, the industry cannot depend on testing to screen out an IC with one resistive via among tens of millions of such devices. At present, there are no appropriate techniques available to rapidly diagnose and localize this type of defect in a complex IC. The result is a greatly increasing risk that potentially threatens major reliability exposure for delivered ICs, as well as the inability to quickly recover through identification of root causes and implementation of corrective action.

Breakthroughs are needed in these areas. Failure analysis and root cause determination of defects is very difficult for today's complex microprocessors and ASICs. As these products increase in circuit count and complexity, diagnosability and failure analysis will become more difficult. Tools need to be developed to assist in determining the physical location of die defects, conduct physical failure analysis, and determine the precise root cause failure mechanism of each defect.

The migration of CMOS technology towards 0.10 μm feature sizes will severely challenge the device failure analysis process. There are two categories of needs: evolutionary or incremental, and revolutionary or breakthrough.

The failure analysis process is illustrated by the following major steps:

1. Fail verification
2. Fault localization
3. De-processing
4. Physical characterization

While much of the above process will be served by the evolutionary solutions, the fault localization challenge is especially acute and in need of major breakthroughs, as discussed below. It represents by far the most critical failure analysis need. Without the ability to localize faults to a die area that can be inspected in a practical and cost-effective manner, the ability to understand failure mechanisms and provide corrective action is lost.

Following is a complete, prioritized list of technology constraints/issues for test, diagnostics and failure analysis.

7.2 Discussion of Test, Diagnostics, and Failure Analysis Technology Constraints

7.2.1 Constraint #1: Diagnosability and Failure Analysis

Problem Statement

Failure analysis and root cause determination of defects is very difficult for today's complex microprocessors and ASICs. As these products increase in basic circuit count (gates, etc.) and complexity, diagnosability and failure analysis will become more difficult. Tools need to be developed to assist in determining the physical location of a die defect , conduct the physical failure analysis, and determine the precise root cause failure mechanism of the defect.

Requirements for testability and diagnosability are diverging at times (e.g., BIST). A need is anticipated for separate focus on testability and diagnosability.

Research Needs

These include the following:

1. Improved tools to generate the test diagnostics for isolating the location of failures
2. Failure analysis techniques to accommodate smaller design ground rules and more complex circuitry, and provide shorter turnaround time for physical failure analysis. Turnaround time is critical for faster learning of yield and reliability.
3. Development of techniques for diagnostics for the varied design-for-test strategies in the marketplace

Evolutionary Needs

Incremental improvements are needed to existing tools and techniques to keep pace with technology. Examples include regular increases in SEM resolution and the development of plasma delayering processes for new films. Routine developments of this nature are required across the failure analysis process as follows (order not prioritized).

- Laboratory testers (speed, vector depth, etc.)
- Parametric measurement (voltage, current resolution)
- Wet and dry delayering process for new films
- Depackaging processes
- Focused ion (FIB) cross-sectioning, milling, and deposition
- X-ray radiography resolution
- SEM resolution, acoustic microscope resolution
- Integration of computer-aided design (CAD) navigation across the failure analysis (FA) tool set
- Electron beam tester resolution, crosstalk, etc.

Revolutionary Needs

Revolutionary needs require major shifts in capability, driven by drastic changes in analytical method. Examples include high spatial resolution backside thermal mapping and backside waveform acquisition. Developments in this area are the most critical and require major

combined efforts of industry, academia, national laboratories, and analytical equipment suppliers. Following is a prioritized list of these needs.

1. Software-based fault localization tools compatible with major test methodologies (e.g., scan, I_{DDQ}, BIST, stuck-fault, AC test, dynamics, embedded cores). An especially important subset of these are tools for localization of AC or performance fails.
2. Hardware-based fault localization tools to complement and supplement the above as appropriate. Examples include migration of existing capability (waveform acquisition, emission testing, thermal mapping) to the backside of the die, and backside thinning techniques.
3. Inspection techniques beyond optical microscopy that offer high resolution without sacrificing throughput (e.g., SEM offers much higher resolution than optical but is much slower and must be done one level at a time)
4. Internal node DC microprobing capability for characterizing individual circuit or transistor parameters, or isolating leakage paths. Existing optomechanical systems are inadequate.
5. Signature analysis techniques to significantly reduce or eliminate the need for physical failure analysis.

7.2.2 Constraint #2: Test Coverage and Known Good Die

Problem Statement

As ICs become more complex in both density and functionality, the ability to test thoroughly for defects and failure mechanisms becomes increasingly more difficult. To achieve 100% defect coverage with traditional methods is impossible, so new methods and models need to be developed.

Known good die are expected to have the same quality and reliability as packaged ICs that are ready to be sent to customers (with the same type of die). Whatever is done to known good die should produce the same quality and reliability effects as the burn-in, testing, screening, etc. of packaged ICs. Another consideration for known good die is process wafer cost. Large wafer sizes and increased processing in the strategic time frame will make it prohibitive to scrap wafers. Known good die must be extricable from “maverick” wafers, posing a very significant challenge.

Research Needs

Improved methods and models are needed to achieve high defect coverage.

7.2.3 Constraint #3: Application versus Test Program Correlation

Problem Statement

As devices are placed into more complex systems, there will be an increasing need to ensure that a test program correlates well with the application on which the device must run. This will require improved means of modeling applications in order to generate test programs.

Research Needs

Improved models are required to model applications to generate test programs.

7.2.4 Constraint #4: Self Test

Problem Statement

One means of reducing test time and test cost is to design a chip to test itself at power-up, on command, or both. This is especially true for memory devices where the required test vectors are relatively easy to generate. Efforts should be made to see if this technique can be expanded to non-memory use.

Research Needs

These include the following:

1. Develop design methods to include extremely low frequency (ELF) testing at power-up and/or on command for non-memory devices.
2. Develop methods to increase fault coverage and/or testability for self-test methodologies.

7.2.5 Constraint #5: I_{DDQ} Required

Problem Statement

To improve defect detection, it is desirable to efficiently implement I_{DDQ} testing. To reduce/eliminate burn-in, it is feasible to voltage-stress ICs and sort according to increased I_{DDQ}. For both of these approaches to be implemented most effectively, ICs should be designed so that low levels of I_{DDQ} can be measured and correlated to test patterns and their corresponding defect coverage.

Research Needs

Improved design methodologies to enable low levels of I_{DDQ} to be measured at test.

7.2.6 Constraint #6: Stuck Fault Coverage

Problem Statement

A fault is defined as the case where the physical behavior of the device or circuit does not match the expected design result. in the level-sensitive scan design (LSSD) test methodology, stuck faults are defined as a DC level logic fault. Software tools are required to define these faults for a given design, and produce efficient test vectors which will capture a very high percentage of these stuck faults.

Research Needs

Improved design systems that generate tests which will have a very high coverage with a minimum quantity of test vectors.

7.2.7 Constraint #7: Tester Precision

Problem Statement

As devices become faster, it becomes necessary to measure signals at ever-decreasing time intervals. The precision of testers in this time frame will have to move from the few nanoseconds to few picoseconds.

Improvements are needed in the tester/product interface. Areas of concern include accuracy and resolution of high speed clocks and pin electronics, test vector volumes, data buffer sizes, number of I/Os, probe technology, and the mechanical interface between the tester and the device-under-test (DUT).

Focus should be on design-for-test (DFT) methods to ensure the required precision from what can be practically moved through the tester/DUT interface.

Research Needs

These are as follows:

1. Development of tools and technology to efficiently enable the testing of the product accurately, quickly, reliably, and at low cost.
2. Development of DFT methods necessary to derive the required precision from what can be practically moved through the tester/DUT interface.
3. Improved tester precision to the picosecond range and transporting same to the chip interface in the anticipated frequency and high pin-count environment. This includes better socket and probing technologies.
4. Major opportunity to create such standards as
    - Device interface board (DIB) interface standards
    - Standard interfaces between test generators and auto test equipment (ATE)
    - Interchangeability standards for test programs between ATEs
    - Mechanical interface standards for handlers

7.2.8 Constraint #8: Test Vector Generation

Problem Statement

For application-specific integrated circuit (ASIC) devices, the test programs are generated by the customer who designs the part, so that the amount of test coverage depends on the ability of that customer to generate the test vectors. Improved techniques will be required to generate these vectors in order to maximize test coverage.

Research Needs

These include improved techniques to generate test vectors for ASIC devices.

7.2.9 Constraint #9: Delay Fault Testing

Problem Statement

A delay fault is a fault that causes a circuit to most slowly achieve its intended state, or for a signal to propagate through a series of circuit elements more slowly than intended. Software tools are required that can analyze a specific design to determine critical timing paths, determine the delay faults associated with that critical path, and generate efficient test vectors that will test for a high percentage of these faults.

Research Needs

Software tools need to be developed that can analyze a specific design to determine critical timing paths, determine the delay faults associated with that critical path, and generate efficient test vectors that will test for a high percentage of these faults.

7.2.10 Constraint #10: Cost Of Test

Problem Statement

As semiconductor products grow in circuit count and complexity, the cost of providing comprehensive testing increases at a rapid rate. Development of low-cost testing techniques utilizing on-chip self test, reduced pin counts, and reduced test vector requirements will be necessary. Development of test/burn-in costing techniques and models also would be helpful.

Research Needs

These include development of design systems to include sophisticated on-chip test capability with minimum pin count and test vector capabilities

7.2.11 Constraint #11: Handling Large Test Programs

Problem Statement

As devices grow to include larger and larger functional blocks and the need to maximize test coverage increases, larger functional test programs will need to be carried in tester memories. Testers will need to be designed to handle such large test programs without compromising test time.

Research Needs

These include improvement in the design of tester memory to enable large test programs to be run without increasing test times.

7.2.12 Constraint #12: Thermal, Noise, and Power Requirements

Problem Statement

Future test techniques will need to address environmental test requirements, including power dissipation, temperature control, and Vdd/Gnd noise levels. Analytical models will be needed to predict power dissipation, noise, delta I (DI/DT), and thermal chip behavior.

Research Needs

Develop analytical models to predict power, noise thermal chip behavior, and delta I.

7.2.13 Constraint #13: Interface Requirements

Problem Statement

With respect to requirements in the tester/product interface, areas of concern include accuracy and resolution of high speed clocks and pin electronics, test vector volumes, data buffer sizes, number of I/Os, and probe technology.

Research Needs

These include development of tools and technology to efficiently enable accurate, quick, and low-cost product testing.

7.2.14 Constraint #14: Product Tracking

Problem Statement

Pertaining to requirements in the product/data interface, areas of concern include standardization of design/test information (including test vectors), footprint/probing, information, product tracking data (lot, wafer, die location, date, binning, etc.), and test program generation data.

Research Needs

These include development low-cost, easily implementable methods to track product.

7.2.15 Constraint #15: Room Temperature Test

Problem Statement

Testing at non-ambient temperatures is not desirable from a cost and performance perspective. Techniques are needed to model and understand product performance at the sub-ambient and elevated temperatures and to translate this information into tests that can be performed at ambient temperatures.

Research Needs

These include development of efficient techniques for generating room temperature tests which will detect defects that normally occur at elevated and sub-ambient temperatures.

8 PRODUCT ANALYSIS FORUM ROADMAP

8.1 Summary

This section presents an FA technology roadmap that addresses a broad set of semiconductor industry needs through the year 2007. It is derived from 1994 National Roadmap. The material for this section has been gathered by member company failure analysis representatives who comprise SEMATECH's Product Analysis (PA) Forum. This section is intended as a roadmap of future challenges for the following professionals:

- Those involved in performing failure analysis for CMOS ultra large scale integration (ULSI) circuits and their variants
- Suppliers of equipment and services to the FA community
- Various strategic planning organizations in the semiconductor industry, e.g., design, test and process development groups

This section includes relevant elements of the semiconductor technology roadmap, which serves as the primary driver of the FA capabilities, resulting FA challenges, and key capabilities needed to meet these FA challenges through the technology generations.

8.2 Introduction

Failure analysis has been an integral part of the fast-growing semiconductor industry, for its contributions in accelerating the pace of improvements in device performance, manufacturability and cost. FA customers are typically corporate development groups, manufacturing facilities, quality, reliability engineering, and end-customer service organizations. The demands from these customers throughout the short existence of the industry have remained the same: faster, more successful analyses at a reasonable cost. Since failure analysis by definition is a reactive step, i.e., the analytical tools and methods needed are specific to the failure type, the failure analysis technologies often lag the manufacturing technologies. This typically leads to longer throughput times, lower success rates and higher cost. Also, the move from one generation of manufacturing technology to the next appears to be accelerating, which compounds the problem. Therefore, a conscious effort needs to be made to anticipate as much as possible the FA challenges of the future and prepare a roadmap of capabilities given the best knowledge available today.

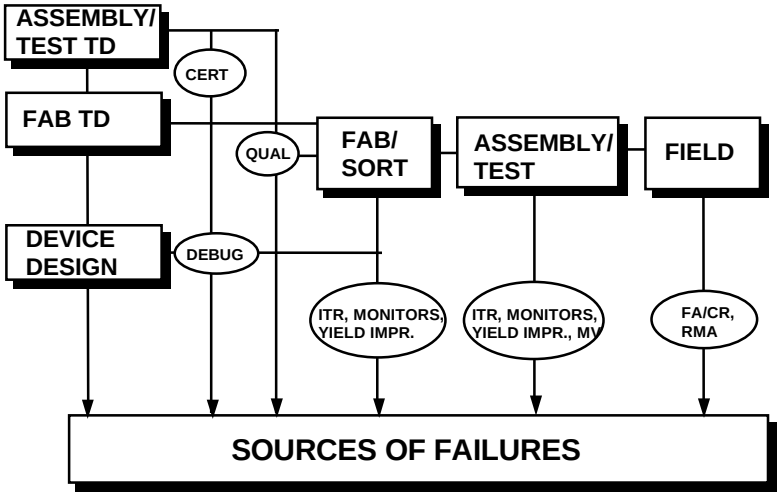

Figure 1 Sources of Failures in Relation to Device Life Cycle

FA as a process is inherent to the development and manufacture of ICs. Failures occur at all stages of development, certification and manufacturing of ICs, and during the final application in an intermediate site (system manufacture) or end-customer's site. Technologies that were needed to perform FA in the 70s were fairly simple and inexpensive. With the advent of very large scale integration (VLSI) and smaller geometries, these technologies have grown in complexity and cost, and this trend is expected to continue. Future technology roadmaps published by several industry organizations pose an even greater challenge, and point to a need for not only rapid evolution of existing FA technologies but a need for breakthroughs as well. This section addresses the key challenges posed by the National Roadmap on failure analysis, and proposes possible solutions given the constraints of the current state of the art. The guidelines are likely to change with time, and may be rendered obsolete/invalid if the key technology drivers or the resulting FA challenges change. Wherever new capabilities are needed, effort has been made to stress the need for further development. As new capabilities become available, future roadmap documents will incorporate those capabilities.

8.3 Purpose and Scope

The technologies addressed here are limited to the failure analysis of silicon CMOS ULSI circuits as defined in the National Roadmap. These include memories (both volatile and non-volatile), random logic devices, ASICs and programmable memory and logic devices. To a lesser extent, this section may apply to bipolar and other silicon technologies. Any applicability of these capabilities outside this scope is coincidental.

8.4 Roadmap Generation Process

Information in this section was processed in individual PA Forum meetings, and a consensus approach was used to arrive at the final roadmap. As such, this roadmap may not reflect each SEMATECH member company's exact plan of record, but rather a consensus on the most likely average scenario.

8.5 Failure Analysis as a Process

The FA process can be divided into an approximately linear flow, consisting of five logical blocks. Wherever possible, the roadmap refers to these blocks.

8.5.1 Assure Failure Validity

In this process step, the failed units have been received from an automated test environment, and are verified on a laboratory tester using a reduced test set as being valid failures. The failures are then characterized to detect any patterns or common characteristics, so that a reduced number of failed units can be identified for further in-depth analysis.

Table 6 Key Failure Analysis Drivers Extracted from the Roadmap

	Intro to Manufacture Date	1995	1998	2001	2004	2007
	Minimum feature size, microns	0.35	0.25	0.18	0.12	0.1
	Memory size (DRAM) MB	64M	256M	1G	4G	16G
	Gates per chip	800K	2M	5M	10M	20M
	Interconnect levels	4 to 5	5	5 to 6	6	6 to 7
PRIMARY	Max power - high performance proc., W	15	30	40	40-120	40-200
ROADMAP	Max power - portable proc., W	4	4	4	4	4
DRIVERS	Min supply voltage, V	2.2	2.2	1.5	1.5	1.5
	Number of I/O pins	750	1500	2000	3500	5000
	Speed of processor - off chip, MHz	100	175	250	350	500
	Speed of processor - on chip, MHz	200	350	500	700	1000
	Chip size, microprocessor, mm sq.	400	600	800	1000	1750
	Chip size, DRAM, mm sq.	200	370	500	750	1000
	Package Technology, processor (leading)	Flip chip	Flip chip	Flip chip	Flip chip	Flip chip
	Package Technology, memory (leading)	DIP	Cube?/ Others	Cube?/ Others	Cube?/ Others	Cube
ADDI-TIONAL	Materials - Gate ox thickness Tox-eff, nm	7-12	4-6	4-5	4-5	<4
DRIVERS	Materials - Metallization	Al	Al, Cu	Al, Cu	Al, Cu	Al, Cu
	Materials - ILD	Oxide, Air, Polyimide, Low Dielectric				
	Design Methodology - Database	Flat	Hierarch.	Hierarch	Hierarch.	Hierarch.
	Design Methodology - Model	Behavioral	Behavioral	symbolic	symbolic	megablock

Common hardware tools used in this process step are bench testers for logic and memory, parametric analyzers and logic analyzers. Common software tools are those used for signature analysis. At the end of this step, enough information is commonly available to determine if the failures are package-related or die-related.

8.5.2 Localize/Characterize Faults.

This process step is used to isolate the defective areas in the failed units. The defective areas may be in the package or on the die, and a number of tools may be needed to isolate the defects down to a smaller area on the package or die. Some die analysis tools used in this process step are the e-beam tester, emission microscope, charge induced voltage alteration (CIVA), and thermal mapping tools. Typically these techniques require the chip to be in a fully functional state. Some circuit modification may be needed at this point, for which a tool such as focused ion beam may be used. At the end of this process step, there is usually enough information available to determine what deprocessing step needs to be used to obtain access to the defect that caused the failure.

8.5.3 Sample Preparation/ Defect Tracing

This step involves tools that are normally used to deprocess a die/package, so that the analyst can gain access to the actual defect. At the die level, this may involve local or global delayering. For packages, it may involve cross-sectioning. Some of the tools used for this purpose are plasma etchers, reactive ion etchers, mechanical polishers, chemical etching agents etc. The type of tool used depends on the hypothesis as to what the nature of the defect may be, and also on the technology on which the die is built.

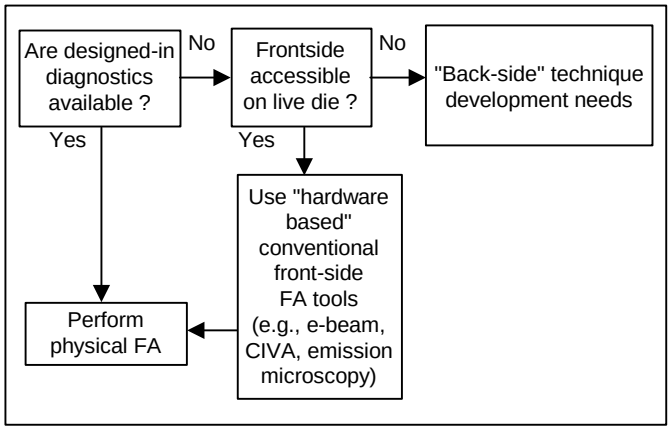

Figure 2 Flip Chip FA Flow

8.5.4 Physical/Chemical Characterization

This is usually the final major step in a typical root-cause analysis effort, involving tools that image and analyze the composition of the defect. Typical tools used in this step are acoustic microscopes for packages, optical microscopes, scanning electron microscopes, transmission electron microscopes, auger electron microprobes, etc.

8.5.5 Root Cause Determination

Root cause determination involves using existing data or generating new data to link the defect to a specific process step or steps in the manufacturing flow. Since most of the procedures used for this step are specific to the proprietary nature of the manufacturing processes, no off-the-shelf solutions are discussed in this publication.

8.6 Discussion

The key elements of the National Roadmap are shown in Table 6. The elements that affect the FA process as it is known today have been selected and shown here. They include transistor size, transistor density, packaging technologies, device speed etc. These and other possible changes in technology are shown in this chart.

8.6.1 Significance of the National Roadmap to the FA Community

The key drivers, namely higher speed, smaller geometries, multiple metal layers, lower voltages, larger die, and new packaging technologies all have significant impact over how FA is accomplished. New packaging techniques, (e.g., flip chip) reduce physical observability to almost nil and drive the need for software tools to localize the failure. Smaller geometries drive the need for smaller and more effective non-contact probing technologies. Higher speed and lower voltages also drive better non-contacting probes and drive the need for more noise immune probing environments. Multiple metal layers drive the need for better deprocessing and microsurgical tools. Furthermore, these changes in technologies may lead to entirely new defect/failure mechanisms, which may drive the need for capabilities that are not mentioned in this paper. Additional drivers, also referenced in the tables, such as differences in packaging technology, materials used for metallization, and design methodologies all have implications towards how the failure analysis tools and methodologies need to evolve.

Perhaps the largest impact is driven by the move from conventional to flip chip technology, which severely limits observability into the circuits from the top of the die. On one hand, development of package reworking technologies may be needed. On the other hand, tools that allow fault localization without the need for physical tools and tools that allow in situ observation of flip-chip defects also may be needed. In fact, the entire FA flow may be affected by the presence or absence of built-in diagnosability by design. An example of that flow is given in Figure 2**.**

Also, new materials drive the need to develop newer deprocessing technologies to etch copper and other materials. New hierarchical design databases drive the need for tools that translate the data into layout information that analysts can use in the lab.

In general, the needed technologies fall into two categories: evolutionary improvements to existing technologies, and breakthroughs to address needs that do not exist today. Technologies such as the logic tester, e-beam probers, mechanical probers, focused ion beam (FIB) milling tools, SEMs need to continue to improve their spatial resolutions. In other areas, such as backside sample preparation and probing, new technologies are needed to address the expected complexity and smaller geometries. Breakthroughs are needed to be able to cost-effectively perform FA on these devices.

Table 7 details each one of the technologies and the consensus view of the SEMATECH PA Forum as to how these technologies will progress with the semiconductor technology. Evolutionary changes are shown with continuous bar graphs, and revolutionary changes are shown with a break in the bar, and a new bar taking its place. The timings of the beginning and the end of the bars are a consensus opinion of the PA forum.

8.7 Future Activities

Traditionally, failure analysis development has been a reactive process of finding solutions to problems created by changes in design, process or test. With the accelerating rate of change in semiconductor technology, a more proactive approach is necessary even to maintain the ability to analyze failures, let alone improve it.

Using this section as a guideline, a development strategy must be put in place for each step of the FA process flow, as they are interdependent and all are necessary to ensure the ability to determine root-cause failure mechanisms. These strategies must contain the following:

1. A thorough understanding of the semiconductor technology drivers that affect each process step
2. A prioritized list of failure analysis needs derived from each driver, indicating specific requirements, e.g., minimum number of diagnosed nodes or transistors
3. A detailed plan for effecting solutions at a reasonable cost and schedule

Most importantly, a focused, cooperative effort is needed between industry, academia, equipment suppliers, and research labs. Designers, test engineers, process developers, and failure analysts also must be involved as a cross-functional team to identify and prioritize needs and orchestrate solutions that address trade-offs, such as silicon area, cost, performance, diagnosability, yield, and others.

As the industry interaction improves, future versions of the roadmap document will be modified as dialog continues between the supplier and SEMATECH member companies. As breakthrough technologies become better known, more definition will be added to the items on the Roadmap. Consequently, the Roadmap is expected to be a living document, continuously updated based on the best available information on the state of the industry.

The ability to improve yield and reliability through failure analysis must be designed-in, not left as an afterthought.

8.8 Conclusion

Both evolutionary and revolutionary technologies are needed to address the FA challenges through the year 2007. The key technology drivers that cause revolutionary changes, i.e., flip chip, design and test methodology changes, etc., have been shown, and the Roadmap has documented the technology changes.

Of immediate concern to this community are two specific technology areas: design for fault/defect isolation, and breakthrough technologies needed for observation from the back of the die. Both are driven by the difficulty caused by the flip chip technology in the process of observing the failed location. These technologies need to be nurtured and made commercially available. Action from the SEMATECH and supplier communities is strongly urged.

Other areas in the Roadmap are no less important, and it is hoped that the supplier community will take note of the revolutionary or breakthrough steps needed at different times. Continuing dialogue with the supplier community is encouraged to ensure these transitions take place in a timely manner.

Table 7 Year 2000 Base Customer Expectations

FA STEP	Capability	1995	1998	2001	2004	2007
ASSURE FAIL VALIDITY	IN-LAB LOGIC TESTING	Low cost logic testers + I_{DDQ} BIST				
	IN-LAB MEMORY TESTING	Raster testers				
	PARAMETRIC CHARACTERIZATION	Semiconductor parametric analyzers				
	LOGIC ANALYSIS	Logic analyzers		Logic analyzers with S/W assist		
LOCALIZE/ CHARACTERIZE FAULTS	INTELLIGENT FAULT LOCALIZATION	Software trace back				
			Fault simulation software for combinational logic			
		Increasing level of designed-in diagnosability (DMA, Scan, BIST, etc.)				
	NODE MEASUREMENT	Mechanical probers				
		Electron beam-based tools				
			Scanning probe testers, backside meas. tools			
	THERMAL DETECTION/ MAPPING	Front side heat-sensing tools				
				High-resolution backside thermal mapping tools		
	LIGHT SENSING/MAPPING	Visible emission microscopy				
			Infrared emission microscopy			
	MICROSURGERY	Focused ion beam tools				
DEFECT TRACING/ SAMPLE PREP.	DELAYERING	Reactive ion etch/Plama-based etch tools				
		Wet etch techniques				
		Mechanical polishing				
	DELID/DEMOUNT	Mechanical				
		wet/dry etch				
		Die removal jigs and tools				
	X-SECTIONING	Focused ion beam tools				
		Mechanical cross sectioning				
	SAMPLE PREP FOR ANALYSIS TOOLS	Plasma coaters, focused ion beam tools				
	ASSEMBLY INTEGRITY VERIFICATION	X-ray radiography				
		Acoustic microscopy (delamination only)				
	POSITIONING ON ANALYSIS SITE	Laser markers, CAD-based navigation				
PHYSICAL/ CHEMICAL CHAR.	THIN FILM DELAM	Acoustic microscopy				
	OPTICAL IMAGING	Optical microscope				
			Confocal microscope			
			IR optical laser scanning scopes			
	SURFACE IMAGING		Scanning electron microscopes			
			Scanning probe technologies (AFM, etc.)			
	ELEMENTAL ANALYSIS	Energy/wavelength X-ray analysis				
			Auger electron spectroscopy			
	STRUCTURAL CHARACTERIZATION	Transmission electron microscope				
	BULK ANALYSIS	Chem lab				

Table 8 Base Customer Expectations at 85C

Market Segment	Company A 1997 - 2000	B 1997 - 2000	C 1997 - 2000	D 1997 & 2000	E 1997 - 2000	F 1997 & 2000	G 1997 & 2000	H 1997 - 2000
Memory								
SPQL(dpm)			70 - 30	5 to 25	50*		20	
EL(dpm)			100 - 40**	100 to 350	200*		50 to 500	
EOL(FITS)			30 - 15	3 to 10	150*		3 to 260	
ASICS								
SPQL(dpm)	<100		70 - 30	<10	50	10 to 100*****		
EL(dpm)	<5000****		100 - 40	175 to 700	200	50 to 1000		
EOL(FITS)	<100		30 - 15	5 to 20	150	10 to 100		
Analog								
SPQL(dpm)		<5 - <3						
EL(dpm)		<220 - <100						
EOL(FITS)		<5 - <3***						
HiEnd uP								
SPQL(dpm)	<100		140 - 60	<10	50		10 to 100	
EL(dpm)	<1000****		200 - 80**	175 to 700	200		100 to 1000	
EOL(FITS)	<100		60 - 30	5 to 10	150		10 to 300	
Low End uP								
SPQL(dpm)			70 - 30	<10	50		15 to 200	
EL(dpm)			100 - 40**	700 to 2800	200		100 to 2000	
EOL(FITS)			30 - 15	20 to 80	150		125 to 500	
Auto								
SPQL(dpm)								0
EL(dpm)								100
EOL(FITS)								N/A
Communication								
SPQL(dpm)								55
EL(dpm)							1000	
EOL(FITS)							100	

Notes:
- **EL + 1 yr at 85C = 8650Hrs.**
- **EOL = 10 yrs at 85C + 87600 Hrs.**
- *** At 70C not 85C for SPQL, EL, EOL.**
- **** In FITS not dpm**
- ***** At 55C not 85C.**
- ****** W/O burn-in by customer cost decision.**
- ******* For ASICS and DSPs, Lifetime: 25yrs for telecom, 15yrs for remote terminal.**

Table 9 Q&R Learning/Customer Expectancy

	Actual '93[1]	Projected[1] '97		Actual '97	Projected 2000
SPQL (dpm)	25-2000	Memory	3.4–25	3.4–70	3.4–50
		ASIC	10–100	<10–500	10–500
		High End µ	5–500	<10–140	<10–500
		Low End µ	5–50	<10–70	<10–500
		Auto	5–300	0–200	0–10
		Comm	5–100	10–55	5–100
EL (dpm)	50-3000	Memory	3–350	50–350	3–500
		ASIC	5–1000	50–700	5–1000
		High End µ	5–1000	54–1000	5–1000
		Low End µ	10–2800	54–2800	10–2800
		Auto	5–1000	100–500	5–100
		Comm	-500	50–1000	5–1000
EOL (FITS)		Memory	3–25	3–260	3–260
		ASIC	1–150	5–150	1–150
		High End µ	5–300	5–150	5–300
		Low End µ	3–120	8–150	3–500
		Auto	5–100	20–700	5–50
		Comm	10–600	10–100	10–100

Notes:

- 1994 Q&R Roadmap identified an ~5X improvement need for Q&R between Y/E '92 actuals and Y/E '97 projected.
- ~5X improvement achieved in SPQL and EOL by Y/E '97. EL remained flat.
- Some companies project no change in Q&R customer expectancy between 1997 and 2000.
- The best attainability in EL is projecting a 5-20X improvement from 1997 to 2000.

[1] From 1994 Q&R Roadmap

APPENDIX
National Technology Roadmap for Semiconductors Reliability Focus Section Draft

Device Reliability Modeling, Measurement, and Wafer Level Reliability

Scope

The process integration section of the 1994 National Roadmap concluded with six *Critical Issues*, of which three are directly related to reliability as barriers to future technology generations. The three issues were as follows:

1. *Modeling (TCAD tools for device/process/reliability/circuit/design simulation)*
2. *Reliability (TCAD tools, models, and data base for designed - in reliability)*
3. *Test, Burn-in, and Failure Analysis*

In the intervening time, there has been good progress through university funded R&D programs in device and packaging reliability modeling and simulation. Further R&D effort now will be necessary to update these models to the new material set that the 1997 National Roadmap contains, in addition to the scaling of technology. An expanded treatment of the National Roadmap focus sections and reliability R&D needs can be found in the SEMATECH Quality and Reliability Technology Roadmap, February 1997.

For conventionally scaled CMOS:

- Below 180 nm, the key reliability issues will be the quality of very thin gate oxides and very shallow junctions, hot carrier reliability, and adequate protection against latch-up, or ESD failures. Similarly, at 180 nm the divergence in speed/performance with AI and SiO2 will drive the implementation of Low k dielectrics and Cu at 130 nm.
- At 100 nm, Tox is expected to scale to about 2.0 nm, and to be lightly doped with nitrogen. For thin “nitrided” oxide, a key challenge will be understanding the mechanisms of basic oxide conduction and reliability wearout failure potential.
- Plasma-induced damage will become more severe as the oxide thickness scales and back-end-of-line (BEOL) processing becomes more complex from added metal levels. Tunneling current will increase for “hyper” thin oxides and the impact on oxide reliability could be significant.

Electromigration characteristics improved with the introduction of Cu will need further improvement by the 70 nm technology nodal. Resistive contact vias will be a significant challenge as the number of vias is scaled and will require process perfection. Integration of updated reliability models into global TCAD tools that will have predictive capability for device, process, reliability, and circuit design simulation has lacked progress and continues as a *Difficult Challenge*.

Reliability defined as a *Critical Issue* in the 1994 National Roadmap is redefined as a barrier when considering the introduction of the major process/material changes planned, together with the flattening out of reliability improvement over the past four years (as shown in the SEMATECH Q&R Technology Roadmap). Even to retain the existing level of reliability, the introduction of the new process/material set must be free of unresolved reliability issues and at defect densities capable of supporting yield and reliability objectives. Plan yields and defect

densities for first-year of production in the 1997 National Roadmap will cause an uplift in failure rate, but will return to current failure rates by the third year. This presents a *Difficult Challenge* for *Reliability Measurements* and *Wafer Level Reliability* to reduce the exposure of the first year failure rate uplift to customers.

Reliability test and measurements will need to move:

- From the IC to test structures
- From DC to AC.
- From packaged part to wafer
- From single device serial test to multi-device parallel test
- From measuring failures to measuring failure predictors
- From burn-in reliance to Test, Measurement, and WLR

WLR measurements that will be needed are shown in the Table 11, Potential Solutions.

The SEMATECH Quality Council sponsored work on process monitors and controls, and separately the proposal entitled *End of Line Monitor Optimization* (published May 17, 1996 and available from the Quality Council) should be used for reference.

Diagnostics and Failure Analysis is a *Difficult Challenge*. Achieving aggressive technology learning curves will depend on diagnostics and failure analysis turn-around. Revolutionary advances in tools and techniques will be necessary to accomplish this. Flip-chip packaging will drive the need for backside analysis techniques and software fault localization. Scaling will drive smaller, effective, probing. MLM will drive the need for new deprocessing/microsurgical tools.

Table 10 Overall Technology Requirements

Technology Requirement	1997 250 nm	2000 180 nm	2003 130 nm	2006 100 nm	2009 70 nm	2012 50 nm
Q&R Customer Requirements						
Quality (dpm)	3–500	0.1–500	0.1–500	0.1–500	0.1–500	0.1–500
EL (dpm)	50–2800	5–2800	5–2800	5–2800	5–2800	5–2800
EOL (FITs)	3–700	1–500	1–500	1–500	1–500	1–500
EOL (FITs) (from 1991 SRC/SIA Reliability Study Projections)	1–10	0.1				
Product/Process Requirements @ 60% Yld.						
Do (d/sq.m)	1703	1419	1182	984	821	684
A (sq. cm)	3.0	3.6	4.3	5.2	6.2	7.5
Yld Def/Chip	0.51	0.51	0.51	0.51	0.51	0.51
Rel./ Def/ Chip	0.005	0.005	0.005	0.005	0.005	0.005
EL (dpm) (Y.D./100)	5000	5000	5000	5000	5000	5000
EL (dpm) (Y.D./500)	1000	1000	1000	1000	1000	1000
80% Yld. (Third Yr.)						
Do (d/sq.m)	1240	1033	862	718	598	498
A (sq. cm)	1.80	2.20	2.60	3.10	3.70	4.50
Yld Def/Chip	0.22	0.22	0.22	0.22	0.22	0.22
EL (dpm) (Y.D./100)	2200	2200	2200	2200	2200	2200
EL (dpm) (Y.D./500)	440	440	440	440	440	440
Scaled Max.	6E+05	9E+05	3E+06	8E+06	2E+07	
Current Density (A/sq.cm)						
Al Limit			1E+06			
Cu Limit					1E+07	

Notes: EL = 1 yr at 85C
EOL = 10 yrs at 85C
EOL, Communications = 25 yrs at 85C

Table 11 Potential Solutions

	1997 250 nm	2000 180 nm	2003 130 nm	2006 100 nm	2009 70 nm	2012 50 nm
Global Modeling, Verification, Predictive Design Tools						
Channel Hot Carrier Degradation	Scaleable CHC models for source-drain engineering. Model stabilizing effect of deuterium vs. hydrogen on interfacial passsivation. Hierarchical models for process/device simulation that support physically based circuit simulation					
EM and Stress Voiding	Hierarchical models for process/interconnect simulation that support physically based circuit simulation					
Salicides	Modeling of min. poly buffer layer thickness, silicide to junction edge, and max. allowed mechanical stress.					
Charging Effects	Modeling of charging effects/physics during plasma processing					
Shallow Junctions	Models defining leakage as a function of geometry, barrier layer, plug, metallization, and allowed mechanical stress.					
Hyper-Thin Gate Oxides	Modeling of leakage physics below 50A level due to direct tunneling. Models of Hi k dielectrics for hot carrier/TDDB.					
Isolation	LOCOS replaced by STI/SOI. Modeling of mechanical stresses, leakage, dynamic charging on AC reliability of SOI.					
Soft Error		Modeling for charge burst from high energy neutrons and charge collection (upset) of device cells.				
ESD	Process/simulation models for ESD at the device level with validation using “benchmark” standard ESD structures.					
Burn-In		Overvoltage testing issue resolved (higher I drive - lower Bvii). Modeling of performance verses burn-in needed.				
Staring Materials	Models for defect/impurity levels, EPI, and SOI on yield/reliability.					
Latchup	Need holding voltage maintained greater than Vdd max. Scaling with 3D simulation vital					
Global TCAD Integration						
* Berkeley Reliability Tool (BERT)						
StaRS Simulator (Vanderbilt)						
ERNI (MIT)			------ Narrow options, update to new material set, and integrate with Global TCAD tools.			
SEU Simulator (Vanderbilt)						
Other Reliability Simulators						

	1997 250 nm	2000 180 nm	2003 130 nm	2006 100 nm	2009 70 nm	2012 50 nm
Wafer Level Reliability						
In Process Testing	Diodes (Do, Stability, Leakage) - Dielectrics (Do, Adhesion)					
	Interconnect (Em, Stress Migration, Corrosion, Bonding, Extrusion)					
	MLO/ILO Integrity (Leakage, Extrusion, Step Coverage)					
	Contact Vias (Resistance, EM) - Gate Oxide (VLF, VBD, TDDB, QBD)					
	Hot Carriers (NFET, PFET, Vt, Idln, Idsat, Gm) - Particle Counts					
	Mobile Ions (Temp/bias, Thick fields) - WLR (V screens, I_{DDQ}, Yld)					
	Maverick Controls (Wafer level, Chip Grading, Cost)					
Reliability Algorithm	Predictability of F/R from WLR data					
Diagnostics and Failure Analysis (Non Evolutionary Tools/Techniques)						
Assure Fall Validation			Logic Analyzers with Software Assist			
Backside Characterization of Faults	Scanning Software for Combinational Logic.					
	Hi-resolution Backside Thermal Mapping.					
	Infra-red Emission Microscopy.					
Physical/Chemical Characterization	IR Optical Laser Scanning Scopes.					
	Scanning Probe Technologies					
Packaging Reliability						
	SEV/Pb Bumps, Alpha Free Solder, DCA					
Architecturally Driven Solutions for Technology						
					Beyond Cu	
			Self Correcting Circuits for Drift			

Table 12 Difficult Challenges

Difficult Challenges > 100 nm and < 100 nm	Summary of Issues
Reliability: Maintaining reliability, or improving it, with each technology generation	In the past four years, reliability has essentially remained flat and not improved. Even to maintain the current reliability levels means that the new materials/processes to support scaling of technology will need to be introduced without any uplift from new failure regimes and defects. Current prevalent defects, i.e., resistive vias, cannot be allowed to scale with the technology and will require breakthrough technology to be eliminated. This is necessary, but not sufficient. By plan, first year production yields have been reduced in this National Roadmap to 60%, increasing reliability defect densities across technology generations. This places a difficult challenge on testing and WLR to reduce the outgoing level of reliability defects and meet customer expectations. Technical breakthroughs will be required to meet reliability expectations.
Global integrated modeling, simulation, verification tools: predictive capability for reliability	Identified in the previous National Roadmap as a Critical Issue as well as Reliability, the goal of a global integrated for modeling and simulation tool with device, process, reliability, and circuit design simulation has seen little progress. There has been some excellent R&D at universities supporting modeling needs. However, in many instances the work needs to be expanded to cover the new materials and structures. The major effort of integration into a global integrated modeling/simulation system has yet to even unfold and will require technical breakthroughs in software/system development.
Test, burn-in, and failure analysis: cost-effective methods consistent with integration and performance trends.	The overvoltage issue must be resolved to retain the benefit of burn-in, especially in light of first-year yield assumptions. Test, diagnostics, and failure analysis will require non-evolutionary tools and techniques to achieve the turnaround times necessary to support the aggressive learning curves planned.

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