

Semi-Additive Process (SAP) Utilizing Very Uniform Ultrathin Copper by A Novel Catalyst

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Abstract

The demand for miniaturization and higher density electronic products has continued steadily for years and this trend is expected to continue, according to various semiconductor technology and applications roadmaps. The printed circuit board (PCB) must support this trend as the central interconnection of the system. There are several options for fine line circuitry. A typical fine line circuit PCB product using copper foil technology, such as the modified Semi-Additive Process (mSAP), uses a thin base copper layer made by pre-etching. The ultrathin copper foil process (SAP with ultrathin copper foil) is facing a technology limit for the miniaturization due to copper roughness and thickness control. The SAP process using sputtered copper is a solution, but the sputtering process is expensive and has issues with via plating. SAP using electroless copper deposition is another solution, but the process involved is challenged to achieve adequate adhesion and insulation between fine pitch circuitries.

A novel catalyst system, liquid metal ink (LMI), has been developed that avoids these concerns and promotes a very controlled copper thickness over the substrate, targeting next generation high density interconnect (HDI) to wafer level packaging substrates and enabling 5micron level feature sizes. This novel catalyst has a unique feature, high density and atomic-level deposition. Whereas conventional tin-palladium catalyst systems provide sporadic coverage over the substrate surface, the deposited catalyst covers the entire substrate surface. As a result, the catalyst enables improved uniformity of the copper deposition starting from the initial stage, while providing higher adhesion and higher insulation resistance compared to the traditional catalysts used in SAP process.

This paper discusses this new catalyst process which both proposes a typical SAP process using the new catalyst and demonstrates the reliability improvements through a comparison between a new SAP PCB process and the conventional SAP PCB process.

Introduction

The semiconductor density improvement by miniaturization has progressed in recent decades as described by the famous Moore's law and it is still progressing today. The semiconductor components are assembled on an interposer called a package substrate. The package substrate allows those components to mount to a base printed circuit board (PCB) using inexpensive soldering technology. When the semiconductor size decreases, the package substrate size is also decreased. The related PCB feature sizes then also follow with the same scaling factor. The semiconductor miniaturization brings significant economical and technical benefits and the semiconductor scale factor becomes the master for the associated package and PCB design. The semi-additive process (SAP) has recently been developed for fine-feature PCBs. However, this is mostly utilizing the thin copper foil base process because of concerns around copper adhesion to the base material. This paper describes a new SAP utilizing chemically plated copper for the base conductor.

SAP process and base copper

SAP is basically the same process concept using the panel pattern plating method that is commonly used at North American PCB fabricators. However, unlike subtractive processes, with SAP the Cu plating is selectively applied only to the pattern, resulting in thinner Cu to be etched away. The 1st step is the base copper preparation, using a copper foil and a plated copper. The 2nd step forms a plating resist with negative pattern over the base copper. Then the 3rd step plates up the circuit copper. The 4th step is the plating resist strip, and the last step is a quick etching of the unnecessary base copper. (Figure 1)

The intention with this process is to get better pattern accuracy than the subtractive process due to less copper etching. Copper etch in PCB process is a wet process by etching solution. The etching proceeds as an isotropic reaction and not like an anisotropic gas phase silicon etching. The isotropic etching ruins pattern accuracy due to different

1. Base copper preparation



2. Plating resist formation



3. Copper plate (electrolytic)



4. Resist strip



5. Quick etch



Figure 1. SAP process flow

etching amount between initial area (copper top) and last area (copper bottom). Therefore, less etching provides higher accuracy of the pattern geometry. The other benefit of this process is the electrolytic plate for the copper growth. It provides shorter process time and better economy for the manufacturing.

A type of fully additive process places a permanent plating resist over the catalytically active substrate and then plates copper on the exposed catalyst to form the circuitry. It is usually plated copper utilizing electroless plating. This gives circuit uniformity, but the process time and cost are higher than the electrolytic plating method. The fully additive method can also utilize electrolytic copper deposition, but it limits the circuitry design due to the electrical connection needed for the electrolytic plating and the lead for the electrical connection will remain as a part of circuitry like an appendix. This could result in some parasitic elements that can disturb the circuit performance.

The SAP uses a thin copper base layer for the electrolytic plating. This provides an advantage compared to a fully additive electroless plating method. There are various means of achieving thin base copper, as described in Table 1.

Table 1. SAP base copper types and advantages/disadvantages

#	Base copper type	Advantages	Disadvantages
1	Etched copper foil	Low cost Applicable to any laminate	Thick copper thickness (3~5 micron) Cannot get copper to hole wall
2	Ultrathin copper foil	Thin base copper foil (1.5~5 micron)	High cost, low peel strength concern Cannot get copper to hole wall
3	Electroless copper plate	Thinner base copper (less than 2 micron) Possible to form microvia and trace at a time	Additional plating process
4	Sputtered copper	Thinnest base copper (nanometer range)	Highest cost and longest process time Cannot coat hole wall

The etched copper foil provides the easiest accessibility. (Table 1 #1) This copper foil is sold by many manufacturers with the 12 microns thick foil most commonly used, balancing cost and foil thickness. Prior to patterning, the foil is uniformly etched to reduce the overall starting thickness. A sulfuric acid with hydrogen peroxide system is a good etchant for this purpose. The foil has enough length of tooth to get adhesion for most of the resin system, however, this tooth length limits the etched down copper thickness to around 3 to 5 microns as a minimum. Many high-density interconnect (HDI) PCB designs use this method for consumer products such as cellular phone, mother board, laptop, desktop PC and so on.

The ultrathin copper foil is also available as a commercial product. (Table 1 #2) It is usually less than 5 microns and is handled with a carrier material. The carrier material such as copper foil or aluminum foil will be removed from the surface, when the foil is laminated over the substrate. The foil tooth for the adhesion is limited to get good thickness control of the base foil, so the physical adhesion is not like regular foil. Also, tooth preparation could limit the achievable thinness of the copper foil due to the foil manufacturing process. An alternative adhesion improvement is a primer coating underneath of the foil. This promotes adequate copper adhesion, but it could be subject to additional UL testing and could affect electrical properties because of the direct contact to the conductor surface. This foil is mainly used for package substrates because of the cost and achievable performance balance, and it does not fit for most of consumer products for the same reason.

The electroless copper plate (chemical copper deposition using wet process) can be used for the SAP¹. (Table 1 #3) The copper plating process is the same as conventional electroless copper plating in the PCB process, but treatment to the base laminate is necessary to get good adhesion in general. A chemical desmear process is commonly used. Once the substrate surface has prepared texture for the adhesion, the catalyst for the electroless copper plating is applied, followed by electroless copper plating. The electroless copper needs 1.0 micron or more to get good current distribution in the panel during the electrolytic copper plating process. The chemically deposited copper has a higher etching rate than the electrolytic copper² and the control of the etch amount is important to prevent undercut generation underneath the electrolytic copper circuit.

The sputtering for the base copper deposition is not generally used for the SAP. (Table 1 #4) Although this method provides the thinnest copper for the base conductor, the process becomes a hurdle for the PCB manufacturers to use. The sputter process is performed under a vacuum and the sputter chamber can take only one panel at a time. These factors limit the equipment capacity and applicable panel size.

The final step of the SAP, quick etch, is not only to apply over unnecessary thin base copper, but also etch the necessary circuit pattern. Minimizing the duration of the quick etching process provides the best circuit conductor shape and accuracy.

This means the minimum base copper thickness delivers the best result. For this reason, the sputtered copper technically promises the best result, but it is not feasible, economically (Table 1 #4). Approximately 40microns trace and space feature size can be achieved by etched copper foil process (Table 1 #1). This is used for major consumer applications such as cellular phone and mother boards. For conductor widths <40um, the ultrathin copper foil process is used. This is used for today's package substrate manufacturing. The electroless copper plate method is used for advanced package substrates and can produce near 20-micron trace and space feature size.

Fundamentals of current challenge

The electroless copper plate is a good solution to reach beyond the copper foil method for a finer pitch design with SAP, because it is possible to use a thinner base conductor. But, the traditional tin-palladium colloidal catalyst sporadically deposits over the substrate surface and the distance between the particles is 10 or more nanometers. Also, the deposited catalyst is tin-palladium alloy, and the catalytic active points are reduced compared to a pure palladium catalyst particle. The initial copper atom deposition starts, sporadically and discontinuously, then the copper atom deposition eventually becomes aligned and densified when the deposited copper is accumulated enough. (Figure 2) This deposition mechanism is undesirable for the SAP or microvia formation which looks for a thinner base conductive layer. An ionic palladium catalyst was developed for better catalyst coverage over the substrate surface. The ionic palladium catalyst has more reactive palladium than a tin-palladium colloidal system and it has relatively higher covering density of the substrate surface than a tin-palladium colloidal system particle. However, the reduction of the copper ion to the metal atom preferentially occurs in the vicinity of palladium neighbor, so the copper deposition of the ionic palladium system is still started, sporadically. This means the minimum base copper layer thickness still has a limitation to getting enough conductivity over the panel surface.

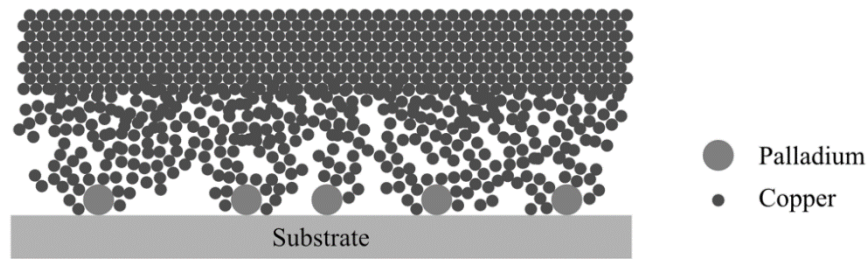


Figure 2. Schematic electroless copper deposition using conventional tin-palladium or ionic palladium catalyst

With manufacturability as the other aspect, the colloidal tin-palladium process is well matured with a long history, and it has no major issues for manufacturing today. This means it can be used in long duration without issues. The ionic palladium process is relatively new, and it is not as mature as the tin-palladium system. The high activity bath may be corrupted by some factors and the control is not as easy as the matured colloidal tin-palladium system. The bath also has a relatively short life. This brings a major economic disadvantage, especially for smaller size or high mix, low-volume production factories. The other possible issue is adhesion. Because of a porous boundary structure, it has limited chemical interaction between the substrate and deposited copper, and it is possible to intrude oxygen molecules and moisture diffusion from the base substrate. These phenomena may ruin the copper to base substrate adhesion over time.

Novel Catalyst Ink and SAP

A novel palladium deposition has been developed using palladium carboxylate. The palladium carboxylate is dissolved in properly selected organic solvents. The solution, a liquid metal ink (LMI) is prepared for a catalyst source of an electroless copper plating process.

A plated electroless copper formed by LMI palladium is prepared for the SAP. The LMI is applied over a substrate using a bar coater method and the coated film is dried in the atmosphere in a few minutes. This coating process proceeds in a cleanroom. The LMI coated substrate is cured in a convection oven for several minutes to reduce the palladium to metal palladium. Once the substrate surface is covered by the palladium metal layer, which can work as an electroless copper plating catalyst, an electroless

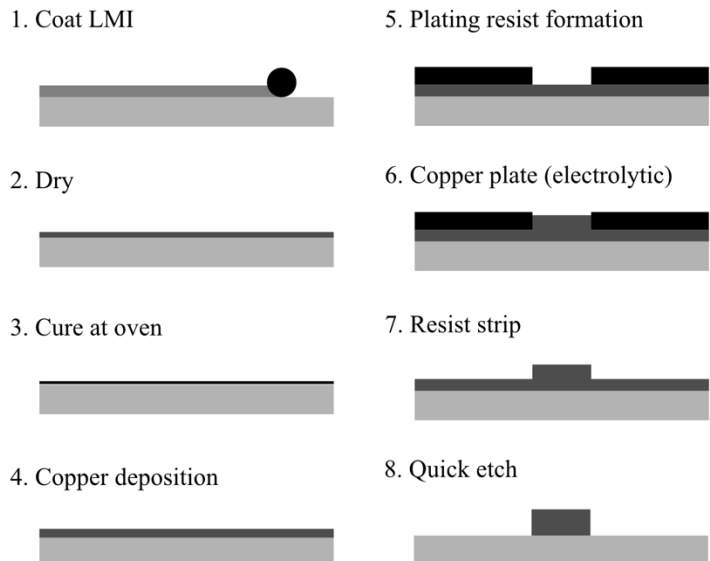


Figure 3. SAP utilizing LMI (Liquid Metal Ink)

copper plating can then be applied to achieve about 0.3 micron of copper film. This copper coated substrate can then support the SAP process. (Figure 3)

When the base conductor for the SAP is made with this process, the base copper can be very thin(0.3um) compared to conventional mSAP and it is thinner than electroless copper by the conventional catalyst process which is usually 1 to 2 microns.

The etching process is also important to achieve fine line circuitry. The industry started with ferric chloride etchant. This etchant has high activity, but the process adds copper to the etching solution and it keeps changing the composition. This uncertainty is not good for the etching speed control. Currently, the industry primarily uses copper chloride etchant. An alternative, alkaline-based etchant is used for the panel pattern plating process, with metallic tin used as an etching resist. This etching solution is designed for relatively thick copper foil and the etching speed is too fast to control SAP processes. Hence, a sulfuric acid – hydrogen peroxide system is commonly used for the SAP process. However, with this system it is possible to generate gas bubbles during the etching and it may influence etching control. The etching solution wettability to the copper can also affect the etching uniformity. Some surfactant is used to improve the etching.

A new solvent mixed etchant system has been developed for SAP. This solvent reduces surface tension and improves wettability. Although a surfactant has same capability, but it also makes unwanted forms and molecular level absorption. The new solvent mixed etchant is adjusted to relatively slow etching speeds, such as 0.5 micron per minute, and it is suitable for the new SAP system that needs less than 0.5 micron of copper.

The common palladium catalyst deposition is a water-based process. Even the palladium ion to metal deposition makes particles during the process because of a water phase reaction, as a result, the palladium deposition over the substrate surface is sporadic particles. In contrast, this LMI process allows the palladium to deposit atomically. This deposited palladium forms a few nanometer thick, ultra-thin layer depending on the LMI coated conditions and the deposited palladium is atomically aligned. The copper atom deposition during electroless plating is also atomically aligned from the beginning when this palladium layer is used for the plating catalyst. (Figure 4)

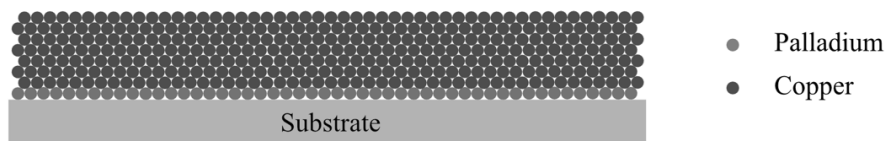


Figure 4. Electroless copper deposition using liquid metal ink (LMI)

The novel catalyst LMI allows electrolytic copper plating starting with less than 300nm of the electroless copper thickness because of this mechanism. This extremely thin copper can be etched in a very short time and it maintains the circuits three-dimensional structure very well when it is applied to this SAP circuit formation. This also minimizes the isotropic etching influence on the trace formation.

Figure 5 shows a TEM/EDS image of the palladium layer by LMI (in red). The LMI layer is deposited over a glass substrate (bottom side) and potted with epoxy resin (top side) during the sample preparation. The cross section image indicates very consistent thickness following the glass substrate topography. The LMI ink and process parameters set 8.3 nm for this test sample and this section image indicates around 8 nm of the layer thickness. The thickness control needs minor adjustment to hit the target. The organo-metal ink concentration and the coated ink thickness can control 1/10 accuracy (+/-10%) of this test, then the metal deposition thickness is possibly controlled within 0.1nm or better accuracy as nominal thickness. Also, thickness can be down to sub-nanometer thick. This thickness range is very close to gas phase processes such as MOCVD and sputter technology³.

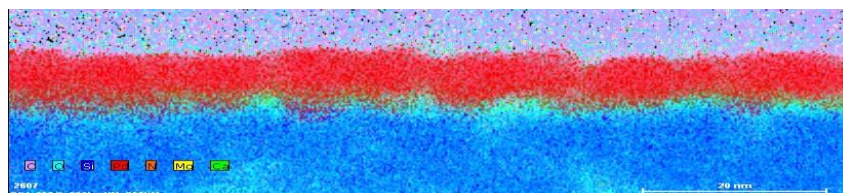


Figure 5. TEM/EDS image showing the palladium layer by LMI (red)

Here are the coating parameters used for the above and the calculation for the estimated palladium layer thickness.

Parameters

- Palladium ink concentration: 1% (by weight, as Pd)
 - Coated ink thickness (wet): 10 micron
 - Palladium density: 12.0 g/cm³
 - Estimated Palladium thickness (metal)
- $$= 1 \times 10^{-2} \times 10 \times 10^{-7} / 12.0 = 8.3 \times 10^{-10} \text{ cm} = 8.3 \text{ nm}$$

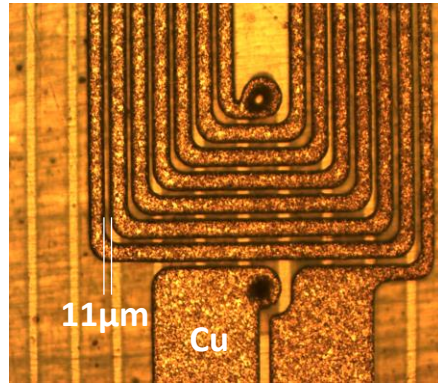


Figure 6. Flex circuit by SAP with LMI copper

Figure 6 shows an example of a flexible circuit made with the SAP utilizing LMI base copper and the new etchant. The trace width is 24 micron, the space between traces is 11 micron and the conductor height is 15 micron. It is extremely challenging to achieve clean etching with this geometry with the conventional methods and equipment. The newly developed organic solvent mixed etching chemical allows this process with conventional conveyor horizontal spray machine. This indicates the copper height is controlled to 7 ~8 micron, then 5 micron each of the trace and space design can be achievable.

Fully additive process

In addition to semi-additive processes, the LMI catalyst can be used with a fully additive process. The process is as follows. The first step is the catalyst coating over the substrate which is dried and cured. The next step is the patterning of an etching resist with positive image of the circuit. Conventional thin dry film resist can be used. This is followed by etching. The common acidic etchant such as ferric chloride system can be used. Next, the etching resist is removed with common processing. The last step is electroless plating. The substrate is dipped into the electroless copper bath and the copper is deposited over the catalyst but not in the areas where it was removed. (Figure 7)

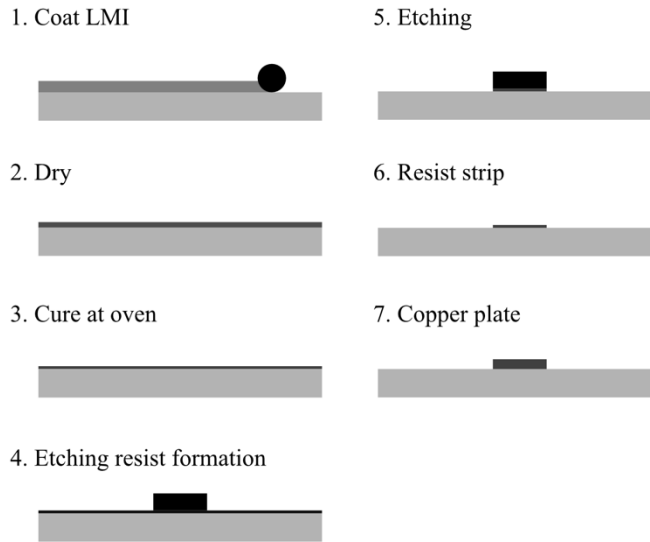


Figure 7. Full additive process with LMI catalyst

Figure 8 is an example from a test vehicle. The conductive pattern is made with the fully additive process described in Figure 7. The base material is polyimide film and the copper thickness is 1 micron. There is no issue forming a 5-micron trace. Trace copper does grow elliptically, so the copper height (thickness), will have a limit.

This height issue is not only in this fully additive process, but also it is also a concern for the fine traces by any process. Higher height geometry always needs higher adhesion against the same amount of force. (Figure 9)

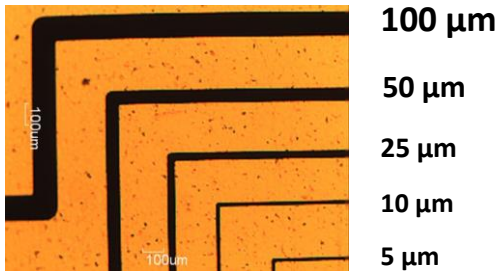


Figure 8. Test pattern formation with full additive process

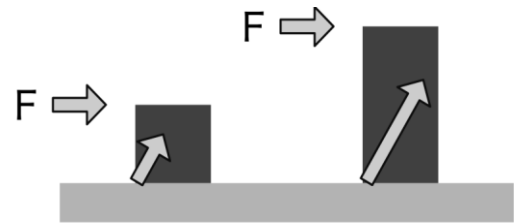


Figure 9. Force difference by trace height

Advantage of LMI ink

This unique layer structure of LMI palladium provides uniqueness for the catalyst. Table 2 shows a comparison of the types of catalyst.

Table 2. Catalyst comparison by type

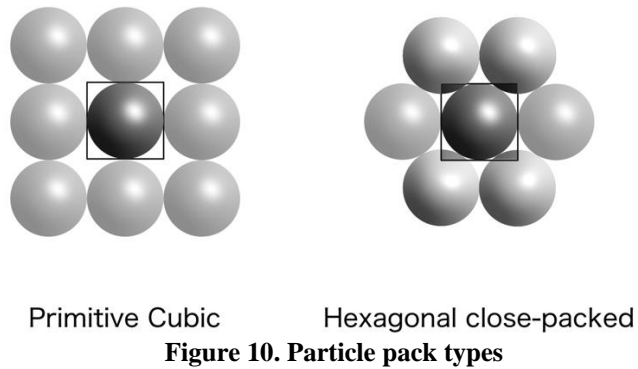
Catalyst type	Particle size (nm)	Absorbed particle ($\mu\text{g}/\text{dm}^2$)	Surface area ratio / Relative catalyst activity
Tin/Palladium	2 ~ 5 ^{4,5,6}	20 ~ 65	0.2 ~ 1.6 / 0.05 ~ 0.4
Ionic Palladium	5~10	10 ~ 35	0.1 ~ 0.4 / 0.05 ~ 0.2
LMI Palladium (Thermal)	5 (thickness)	6 (layer)	1.0 / 1.0

The colloidal tin-palladium is deposited over the substrate as a particle with stannous hydroxide. The particle size is approximately 50 nanometers. Then the stannous hydroxy layer is removed by acidic solution and the tin-palladium alloy particles reside over the surface. This tin-palladium particle size is about 2 to 5 nanometers. The absorption amount of the tin-palladium particles is about 20 to 65 microgram per square decimeter. Then the particle surface area to the deposited surface area (surface area ratio) becomes about 0.2 to 1.6. The tin-palladium alloy particle does not have 100% of the active point compared to the pure palladium because of alloying with tin and residual of stannous hydroxide. The effective active point is considered less than 50%. Also, the whole particle surface could not work for the deposition. It is considered about half of the surface area. Therefore, the effective surface ratio of the tin-palladium catalyst becomes 0.05 to 0.4 or less.

The ionic palladium is deposited over the substrate as 5 to 10 nanometer particle size. The absorption amount of the palladium particle is about 10 to 35 microgram per square decimeter. Then the particle surface area ratio becomes about 0.1 to 0.4.

The LMI palladium layer weight is 6 microgram per decimeter when it is deposited 5 nanometer thick over the substrate. The surface area ratio is obviously 1.0. And this ratio would not be changed when the deposited catalyst layer thickness is changed. This is a great advantage to get stable catalytic activity and to reduce the catalyst cost.

When the particle is a sphere and the top half hemisphere of the particle is considered the active area for the copper deposition, the active particle surface area ratio is 1.57 for the primitive cubic pack. A surface area ratio less than 1.6 means the palladium catalyst particles are not 100% covered over the substrate, and this indicates that the conventional processes do not cover entire substrate surface. By contrast, if the particles are packed as hexagonal close-packed, then the active particle surface area becomes 2.03. (Figure 10) This supports the deposition theory that is schematically described in Figure 2.



The organic solvent system of the palladium ink improves wettability to the substrate compared to water base conventional systems due to the low surface tension of the solvent. This advantage provides a benefit to form fine feature PCB design with reliability and to improve the plating for semiconductor applications. For example, the microvia and plated through hole (PTH) in PCBs is getting smaller and smaller. The uniformity of the catalyst is very important as well as cleanliness of the hole. The water base system uses surfactant (chemical approach) and ultrasonic (mechanical approach) to mitigate defect, but it is a challenge when the hole feature size and aspect ratio become smaller and higher. The novel LMI catalyst system provides a good result with less effort. Because the organic solvent system has lower surface tension, this provides better wettability naturally. Then LMI catalyst system can wet sub-micron diameter hole, even it is blind. Also the layer deposition provides good interaction to the base resin resulting in better adhesion compared to particle adsorption of the conventional method. This is similar with the vapor phase deposition, like the sputtered metal layer, and it delivers with much simpler process and equipment, and lower cost. Some of the sputtered metal is physically penetrated into the resin skin. This improves the metal adhesion. The LMI catalyst process could allow a similar effect through thermal diffusion during the thermal metal deposition process.

Summary

A novel catalyst ink (LMI) has been developed utilizing palladium carboxylate. This ink uses selected organic solvents and it provides high wettability and penetration of the catalyst to any feature of the substrate surface including hole wall and pad of a blind via hole. The coated ink is cured by either heat or chemical reducer. A very uniform palladium is formed over the substrate at a single layer of nano-scale thickness. This provides very high efficiency as a catalyst in both performance and economy. The chemical process over the ink provides sub-nanometer range particle which is very high activity as catalyst. When this LMI is used for the electroless copper plating, ultrathin copper such as 0.5 micron or less can give enough conductivity uniformness to the entire panel to run the electrolytic copper plating. Therefore, the PCB can have the fine features such as sub-10 micron trace and space when this ultrathin base copper is utilized for SAP process.

Acknowledgement

The authors would like to thank Tara Dunn from Omni PCB for her valuable inputs.

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