SMD naked film capacitor technologies for severe application environments and circuit functions

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ABSTRACT

The demand for miniaturized electronic equipment and fully-automated assembly lines for mass-production of new products require the availability of a complete range of SMD components.

In electronic circuits, common capacitor circuit functions are: AC filtering (to reduce the harmonics overlapped to the fundamental frequency), small power DC-link (to periodically supply a DC network with high currents and filtering AC ripples), input/output filtering (to reduce the voltage peaks or ripples in DC-DC converter circuits due to parasitic inductances), igniter and boost (to increase voltages and currents and so create an ignition on HID - High Intensity Discharge - Xenon headlamps).

Industrial, automotive, and marine applications add to the above mentioned requirements extremely severe environmental conditions in which this equipment is installed and required to work.

On a component level, required features are therefore: small dimensions, extremely high reliability, low inductance (to limit the switching transient voltages), high dv/dt withstanding, wide working temperature range, long expected life time, high stability vs. time and humidity and high peak withstanding voltage. Film capacitors have some properties that make them ideally suited for these applications, but have been limited in the past by limitations on the upper working temperature range and lack of availability in SMD packages.

Recent technological developments in SMD film capacitors now make them the component choice to satisfy these requirements. The lead free reflow soldering process increasing diffusion and the high temperatures involved have turned advances on SMD Naked Film Capacitors' resistance to high temperatures into a must.

This paper will discuss the technical basis on which advances have been reached in the SMD naked film technology offer for the above mentioned environments and circuit functions (AC filtering, small power DC-link, input/output filtering, igniter and boost), and will give a general guidance on which technology fits best from the requirements of capacitance, size, voltage/current, temperature and humidity resistance.

INTRODUCTION

In applications where capacitance needs to be very stable over a wide temperature range with good reliability and long life expectancy, thru-hole film capacitors are an optimum choice with a very good performance/cost ratio.

Anyway, the need of a new generation of equipment, very miniaturized and manufactured on fully-automated assembly lines, has requested several improvements in film capacitors technology to create SMD film components capable to withstand lead free (LF) reflow process, maintaining excellent electrical behavior, reliability and life expectancy.

Moreover, most of these equipment require high reliability in extremely tough environmental conditions, like severe humidity, high vibrations and wide operating temperature ranges, possibly with the addition of severe thermal shocks.

The technological improvements that have permitted to find solutions to the above-mentioned challenges will be described, highlighting the key design parameters that have been improved in order to meet the specific requirements of each application examined.

Here are the main parameters considered during the development of the right capacitor for each application:

- circuit position and electrical specification
- rated voltage and capacitance value
- physical and electrical properties of film dielectric
- film dielectric design and capacitor manufacturing technologies
- maximum capacitor dimensions needed to fit the PCB layout
- voltage peaks
- current peaks (dv/dt)
- working temperature
- humidity level
- ESR (Equivalent Series Resistance) needed in the application
- ESL (Equivalent Series Inductance) needed in the application and resonance frequency
- expected lifetime of the components

EXPERIMENTAL METHODS

Here is the description of the instruments, tools and methods used during the performed measurements. For each of them, the specific measured parameters have been specified.

Agilent E4980, HP4284A Precision LCR meter and HP4192A Impedance Analyzer (1 kHz and 1 V_{rms}): Capacitance (C), dissipation factor (tan δ), Equivalent Series Resistance (ESR).

Discharge current's curve analysis (Figure 1): resonance frequency and ESL (Equivalent Series Inductance).

The test is carried out charging the capacitor at a low voltage (≈10 Vdc) and subsequently discharging it through a short circuit. The short circuit locates as close as possible to the capacitor to avoid stray inductances. A Rogowsky current probe is used to measure the discharge current.

The value of the ESL and the resonance frequency are easily calculated from the recorded current data.

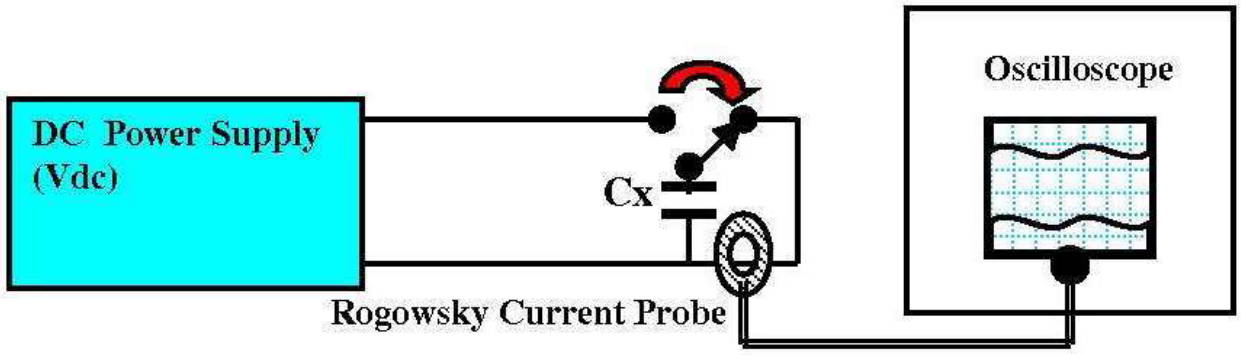


Figure 1: ESL and resonance frequency measurement system

Ripple current testing (Figure 2): self-heating vs. I_{rms}.
The test is carried out to simulate the thermal conditions of an inverter working at the extreme limit of its current withstanding capability. The use of a thermocouple on the capacitor, close to one end termination, allows the study of the capacitor's heating due to the current flow.

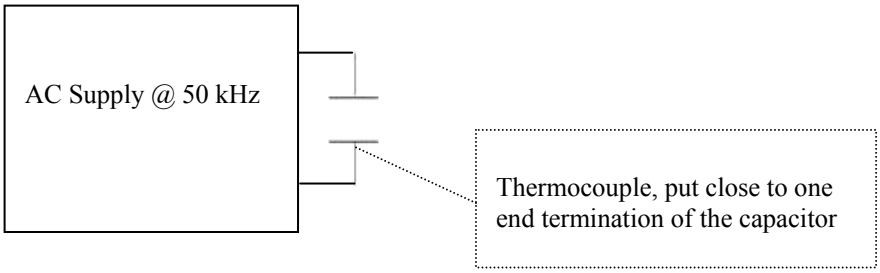


Figure 2: Ripple current testing system schematic

Charge/discharge equipment (Figure 3): δv/δt withstanding.

The capacitor is charged with a DC supply (Vo) up to the spark gap (FS) discharge voltage level, which is lower than Vo. The discharge current flows through the capacitor. The below schematic permits, thanks to very low parasitic resistance, to maximize the current value. R_2 and L_1 are parasitic values.

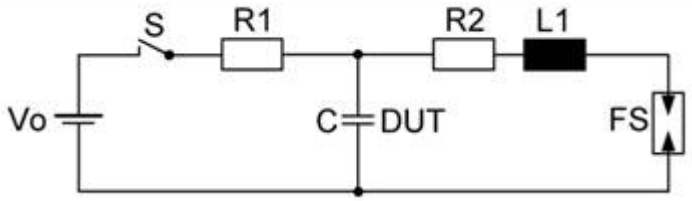


Figure 3: Charge/discharge circuit with spark gap (FS)

Kikusui TOS9201: First Breakdown Voltage - FBDV - test equipment.

The test is carried out applying the following voltage ramp (Figure 4) on the capacitor:

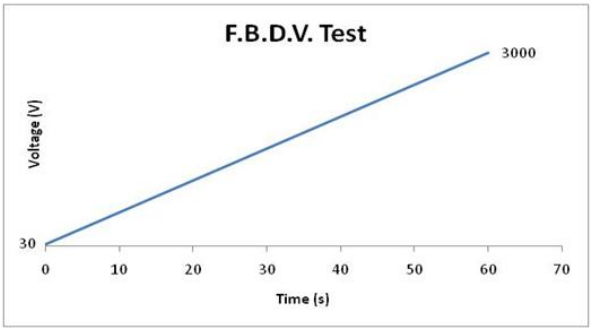


Figure 4: Voltage ramp-up used in the FBDV test

Weiss VT180 and Heraeus HC2020 humidity chambers: Damp heat tests.

DSC (Differential Scanning Calorimeter) test equipment (Figure 5): This test allows the study of polymers' behavior when they are heated up at a specific heat rate (°C/s) and it is commonly used to observe and study polymers' thermal transitions (i.e. the melting point of an amorphous/semi-crystalline polymer or the glass transition).

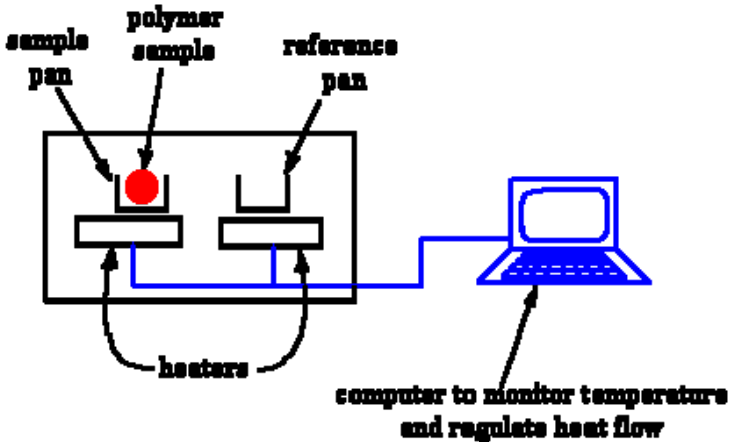


Figure 5: Differential Scanning Calorimeter test equipment.

AC FILTERING

1 - Introduction

AC filtering capacitors have the task of reducing the high frequencies overlapped to the fundamental network frequency (50-60 Hz). Usually, the first significant harmonic is between 2.5 and 6 kHz, depending on the specific equipment the filter used.

In general, film capacitors used in AC filtering are approved by ENEC, UL, and CQC and are made of metalized polypropylene film in wound technology.

These capacitors are named X or Y based on their position in the filter circuit. X capacitors are connected across the line (C3 & C4) while Y capacitors are connected between one line and the earth (C1 & C2) as shown in the following figure:

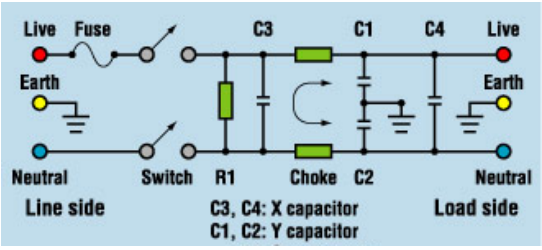


Figure 6: General purpose AC filter with X and Y capacitors

X and Y capacitors are grouped in different sub-classes based on the voltage peaks they are required to withstand, as per the following tables:

Table 1 – X sub-classes

Application	voltage peak in service	voltage peak before endurance test	IEC 60384-14 sub-class
high pulse application	> 2,5 kV; ≤ 4,0kV	4 kV for C ≤ 1µF 4/√C kV for C > 1µF	X1
general purposes	≤ 2,5 kV	2,5 kV for C ≤ 1µF 2,5/√C kV for C > 1µF	X2
general purposes	≤ 1,2 kV	none	X3

Table 2 -Y sub-classes

Application	voltage peak in service	voltage peak before endurance test	IEC 60384-14 sub-class
double or reinforced insulation	≤ 500 Vac	8 kV	Y1
basic or supplementary insulation	≥ 150 Vac; ≤ 300 Vac	5 kV	Y2
basic or supplementary insulation	≥ 150 Vac; ≤ 250 Vac	None	Y3
basic or supplementary insulation	< 150 Vac	2,5 kV	Y4

For the design of AC filtering SMD film capacitors, a careful selection of film dielectric material, based on several electrical and thermal characteristics, has been made.

Plastic film dielectrics used nowadays for capacitors are:

- PP: polypropylene;
- PET: polyethylene terephthalate;
- PEN: polyethylene naphthalate;
- PPS: polyphenylene sulphide.

Table 3: Characteristics comparison between plastic film dielectrics

Property	PP	PET	PEN	PPS
Dielectric Constant (@1 KHz)	2,2	3,3	3,0	3,0
Min Commercial Thickness (µm)	2,4	0,9	1,4	1,2
DF (% @ 1 KHz)	0,02	0,5	0,4	0,05
TCC (DC/C), -55 °C to +125 °C	± 2,5 %	± 5,0 %	± 5,0 %	± 1,5 %
Min Temperature (°C)	-55	-55	-55	-55
Max Temperature Typical (°C)	105	125	125	125
Max Temperature Extended (°C)	125	150	170	170
Dielectric Breakdown (V/µm)	400	280	300	220
Melting Temperature (°C)	178	254	266	283
Reflow & Multiple Reflows Tmax (°C) - for SMD	NO	245	245 - 255	260
self-healing	good	medium	medium-low	low

The self-healing property of film dielectrics (film's ability to self-regenerate an internal drop of insulation resistance) ensures a safe failure mode in AC filtering applications, where electrical noise and peak voltages are added repeatedly or occasionally to the fundamental frequency.

Looking at the above table, PP film is the best in terms of self-healing while it is the worst in terms of melting temperature. This "rule" applies in general for all plastic films: PET has a higher melting temperature than PP, but has lower self-healing capabilities. PEN and PPS are the most suitable plastic films for SMD applications (in particular to withstand the LF reflow process), but they have not the right properties for applications where voltage peaks, higher than the capacitor's rated voltage, are combined to the 50-60Hz network frequency.

To compare the self-healing properties of different materials, their chemical composition must be considered. The lower the ratio between the number of Carbon (C) and Hydrogen + Oxygen (H+O) atoms, the lower the possibility to have conductive Carbon residues as the outcome of the self-healing process (see Figure 7 here below):

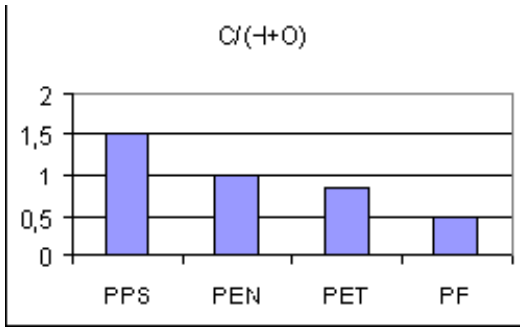


Figure 7: C/(H+O) # of atoms ratio in different plastic film dielectrics

There are also many other parameters to be considered in the study of self-healing phenomenon and, in particular, the higher the clearing energy content during the process, the higher the efficiency of the healing, taking place in the insulation between two adjacent metal layers [4], [5], [6].

In general, SMD capacitors must withstand higher temperatures during the soldering process (reflow)than radial capacitors. To reach the maximum miniaturization, a naked SMD film capacitor family has been created, where the active element is exposed to exactly the same peak temperature of the LF reflow process (up to 245°C as per Jedec 020D1[8], capacitor volume > 350 mm^3, H_{max} > 2,5 mm).

2 - Design of new naked stacked SMD PET film capacitors for AC filtering

According to the specific characteristics of the plastic film materials (see Table 3), in order to have the best behavior both in terms of self-healing property and of LF reflow process withstanding, PET has been chosen as dielectric (PP film is presently not suitable for SMD components due to its low melting temperature).

With the recent advances obtained in the manufacturing process and thermal treatment of PET film, a new naked SMD PET capacitor has been developed, suitable to be used in those AC filtering applications that do not require the approval of ENEC, UL and CQC.

This new SMD PET component cannot in fact be a certified class X or Y suppressor, but it is capable of withstanding voltage peaks as per the following table:

Table 4: voltage peaks vs AC/DC capacitor's rated voltage

AC voltage	DC voltage	Voltage peak
66 Vac	100 Vdc	300 V
143 Vac	250 Vdc	500 V
275 Vac	630 Vdc	800 V

Below is an example of an AC filtering application schematic: an electronic contactor. Notice the presence of a peak voltage limiter (LIM):

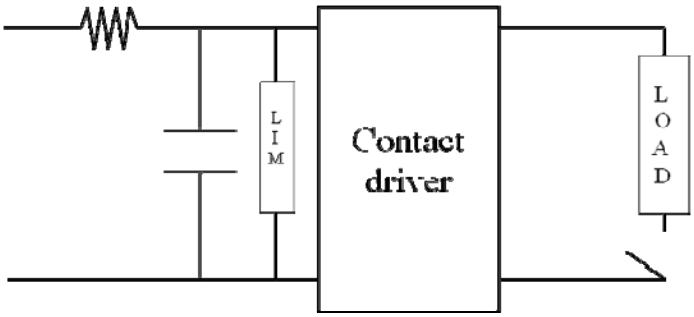


Figure 8: Schematic of AC filtering application with SMD PET film capacitor

The new naked SMD PET capacitor is an extension to the existing naked SMD PEN capacitor offerings. According to the following DSC (Differential Scanning Calorimeter) graphs, there is a big difference in melting temperature between PET and PEN:

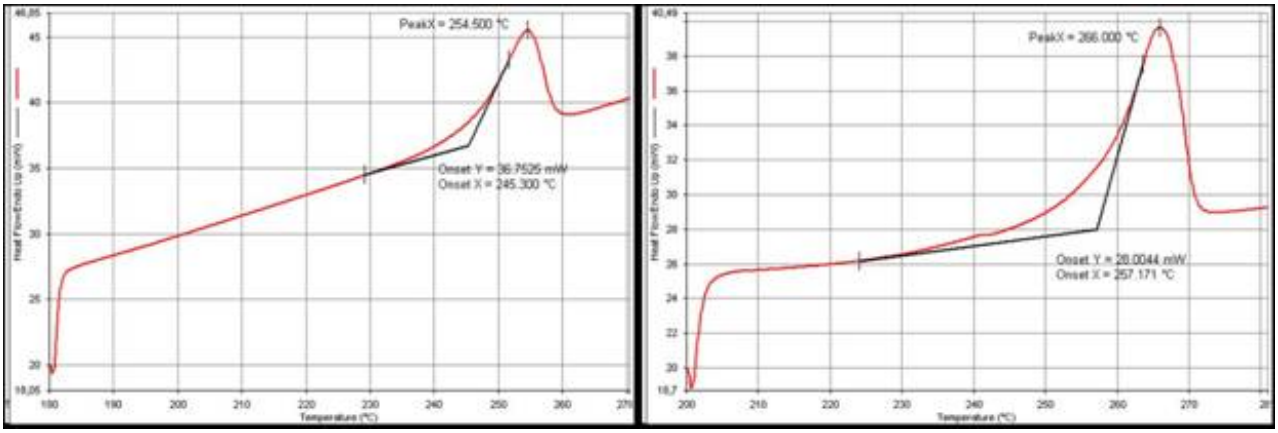


Figure 9: DSC thermograph of PET **Figure 10: DSC thermograph of PEN**

A PCB with the components e.g. of Figure 8, when going through a LF reflow process, represents a challenge for the PET dielectric, because it starts to melt at 245°C. Most of the melting happens at the peak value showed in above graph (254°C).

The preceding DSC graph highlights the fact that the PET film capacitors can withstand reflow processes with peak temperatures up to 245 °C, but with a limited time of exposure to temperatures above 217 °C. Below is a recommended reflow process profile that avoids any physical damage of the PET capacitor's physical structure:

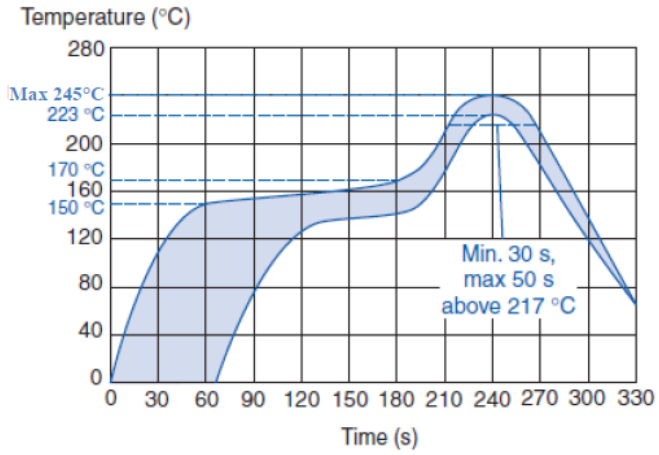


Figure 11: Reflow profile for the new stacked naked SMD PET capacitor family

In order to design a naked SMD PET capacitor capable to withstand a LF reflow process, particular attention has been given to the physical design of the plastic film raw material, to the capacitor manufacturing technology and to the thermal treatment of the capacitor during the manufacturing process.

In the physical design, the main choice was the configuration of metalized and protective films, both made in PET. Stacked technology was chosen as the manufacturing technology.

The thermal treatment, which is the core phase of the manufacturing process of plastic film capacitors in order to reach the best balance of the following aspects need a more thorough discussion:

- good adhesion of single film layers
- thermal stabilization of the component in order to withstand a LF reflow process
- compactness/brittleness ratio of the capacitors

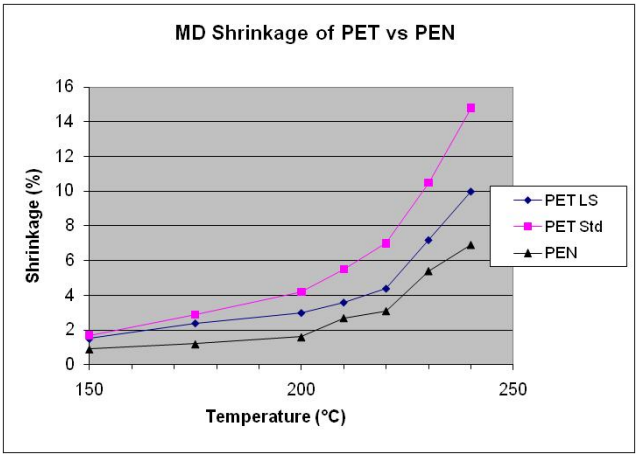
In protected SMD components (e.g. SMD in a plastic box), the reduction of the moisture sensitivity level and the withstanding of damp heat tests are the result of the encapsulation in a box with suitable resin and of the compactness of the active capacitor element.

In naked SMD components, the missing of the box and resin must be compensated by increased compactness of the capacitor element, obtained with dedicated new (and more intense) thermal treatment during the manufacturing process.

The thermal treatment has been studied starting from the shrinkage test results of PEN, PET and PET LS (Low Shrinkage). Tests were carried out on different film thicknesses.

PET LS has the same physical, chemical and electrical properties with the standard PET, but it is more strongly thermally stabilized in order to have smaller shrinkage during the thermal treatment phase in the capacitor's production flow.

The shrinkage is usually measured both along the extrusion Machine Direction (MD) and Transverse Direction (TD). The following graphs are related to 2,0 µm films thickness:



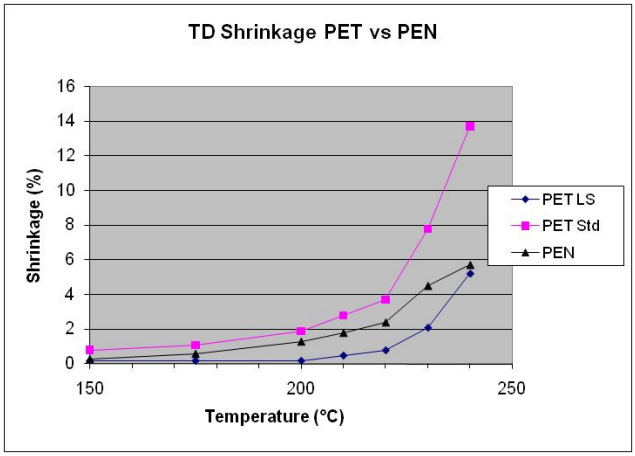


Figure 12: MD shrinkage of different films of 2,0 µm thickness **Figure 13: TD shrinkage of different films of 2,0 µm thickness**

The above graphs show the behavior of different plain films before any thermal treatment, and they were taken into deep consideration during the capacitor design phase. The shrinkage of the PET LS film is more similar to the PEN one than to the standard PET. The higher the shrinkage, the more difficult is the control of the film's physical behavior during the thermal treatment and, therefore, the more complicated to reach the right compromise between good compactness of the capacitor element and the electrical performance (dielectric strength and insulation resistance especially). This is particularly true for naked capacitors.

Figure 14 shows the difference in behavior, when the shrinkage test is carried out after thermal treatment applied on the film in order to thermally stabilize it for the reflow process and for the entire life expectancy:

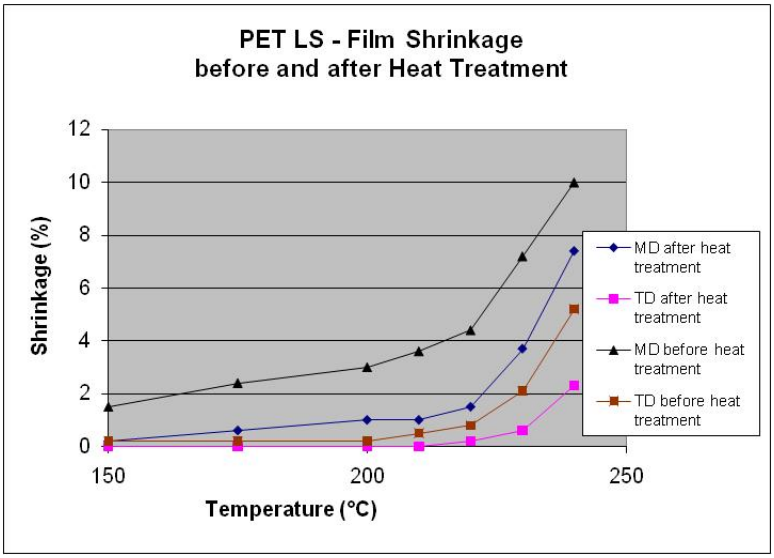


Figure 14: Comparison of the film shrinkage before and after a thermal treatment

Both MD and TD shrinkages decrease after thermal stabilization, and this characteristic permits to maintain the capacitor's good electrical performance and reliability after the LF reflow process. Figures 12 to 14 refer to plain films (not metalized films). In film capacitors, in which metalized films are used as raw material, shrinkage is reduced further, thanks to the adhesion between the metalized layers and the film layers and to the very low shrinkage of the metal itself.

All the above graphs have been created with static measurement, meaning that the points represent the difference between the final and initial dimension after the exposure of the film to a constant temperature in an oven for a specific time (15 min).

More in detail, from a dynamic perspective, films have first an expansion and then a final shrinkage as per following graph:

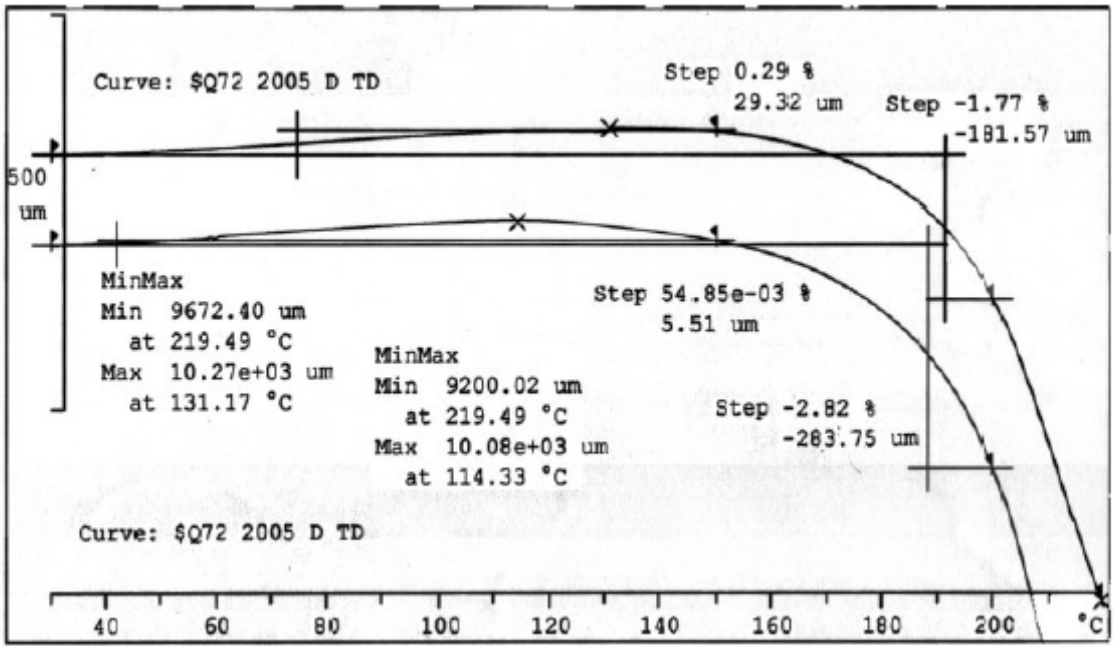


Figure 15: TMA (Thermo Mechanical Analysis) performed on the raw film material

Expansions, shrinkages and their variability along the film have been carefully evaluated during the design of the thermal treatment phase.

3 - Performances of new naked stacked SMD PET film capacitors for AC filtering

In the previous section the challenges of this design have been explained. In this section the performance obtained during this design activity will be described.

A photograph of these capacitors in different sizes is shown in the following picture:

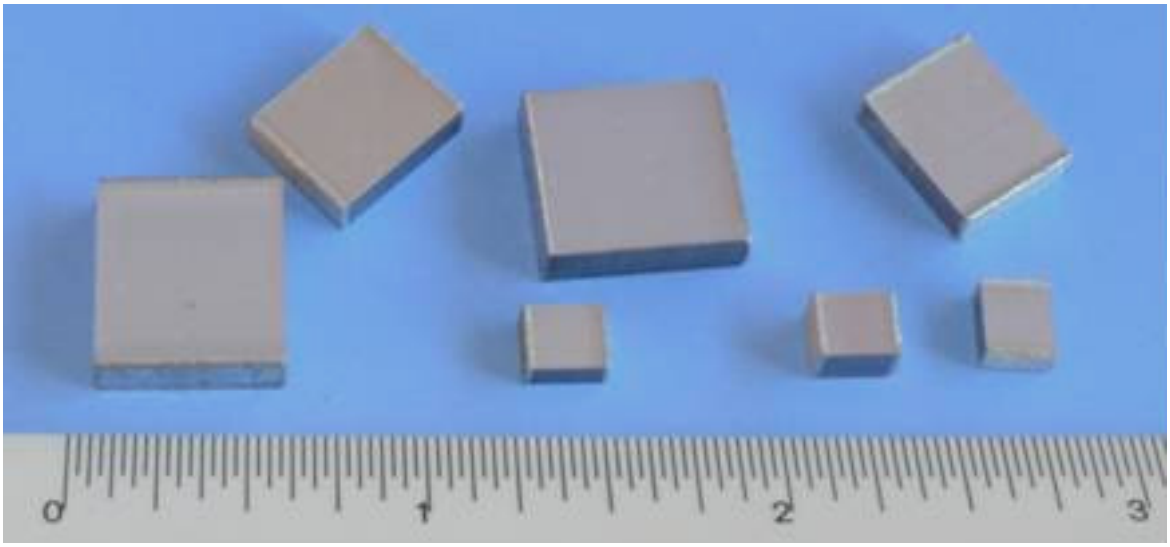
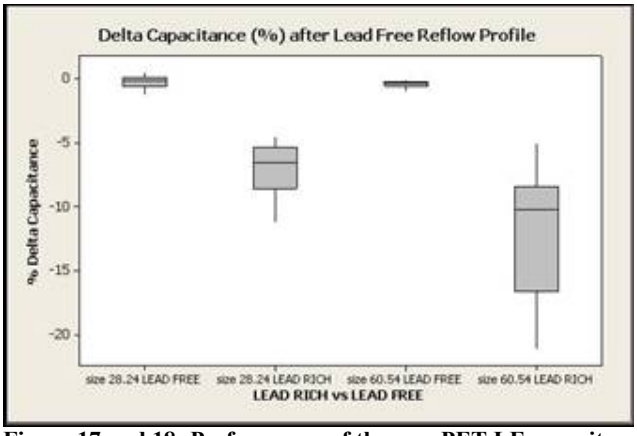


Figure 16: Stacked naked SMD PET capacitors

In the following figures, a comparison between the existing stacked naked SMD PET capacitors (treated with the standard thermal treatment for Lead containing soldering) and the new version (treated with the new thermal treatment) is shown in terms of capacitance variation in a LF reflow process:



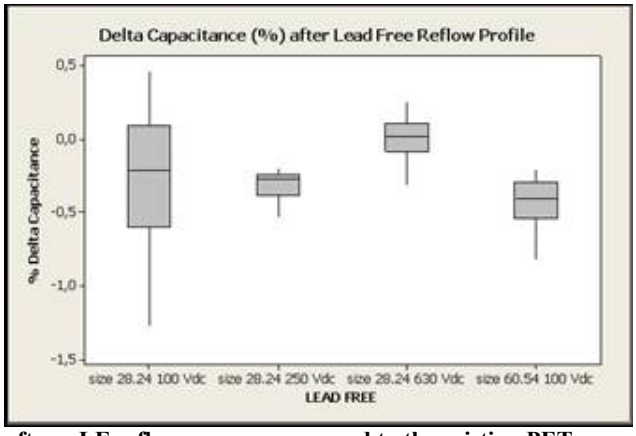
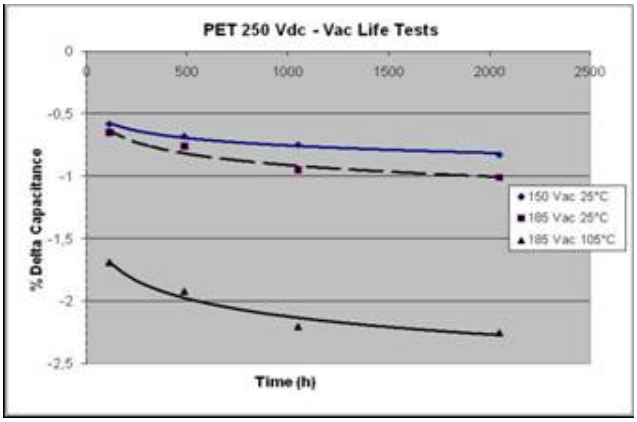


Figure 17 and 18: Performance of the new PET LF capacitors after a LF reflow process compared to the existing PET capacitors family, suitable only for lead rich reflows

Considering that the new version has been designed for AC filtering, several life tests with AC have been carried out:



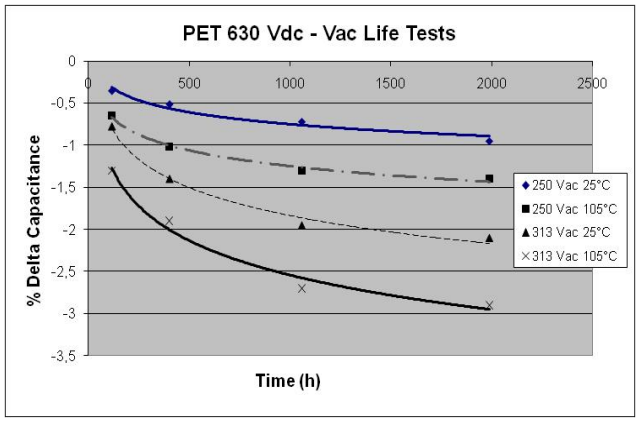


Figure 19: Vac life tests of new 250 Vdc PET capacitors

Figure 20: Vac life tests of new 630 Vdc PET capacitors

In the following graph, the capacitance variations due to a surge test performed with 10/700 waveforms (10µs to reach the peak voltage value and 700 µs to go down to half of the peak) are showed:

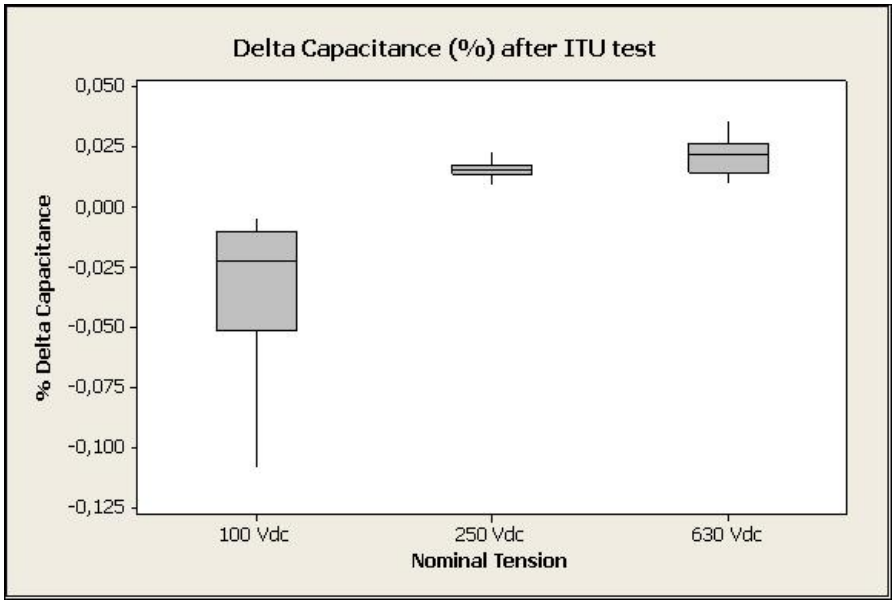


Figure 21: Graph of the capacitance variation after the surge test with peak voltages from Table 4

SMALL POWER DC LINK AND INPUT/ OUTPUT FILTERING

1 - Introduction

Hereafter some examples of a typical DC link application schematic:

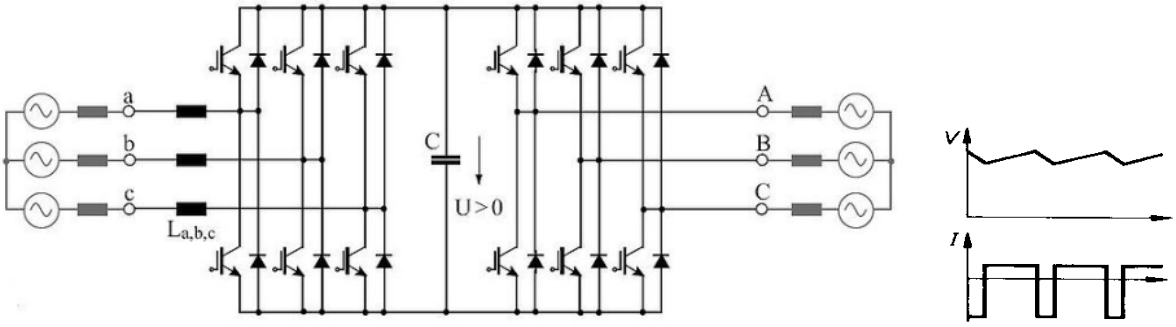


Figure 22: DC link circuit (general purpose version) and typical V/I waveforms

DC link capacitors have two tasks: to stabilize the voltage output of the rectifier, providing enough current to the load, and to filter AC ripples. Ripples are generated by the switching of IGBTs modules working between 1 kHz and 20 kHz that could damage semiconductors, batteries, or other circuit elements.

Below an example of an application schematic, where film capacitors are used in parallel to CMOS, together with an electrolytic acting as DC link, with the purpose to reduce the voltage peaks or ripples in DC-DC converter circuits due to parasitic inductances. With the below design, the total working voltage can be reduced and so the dimension of the CMOS and of the total circuit (Figure 23):

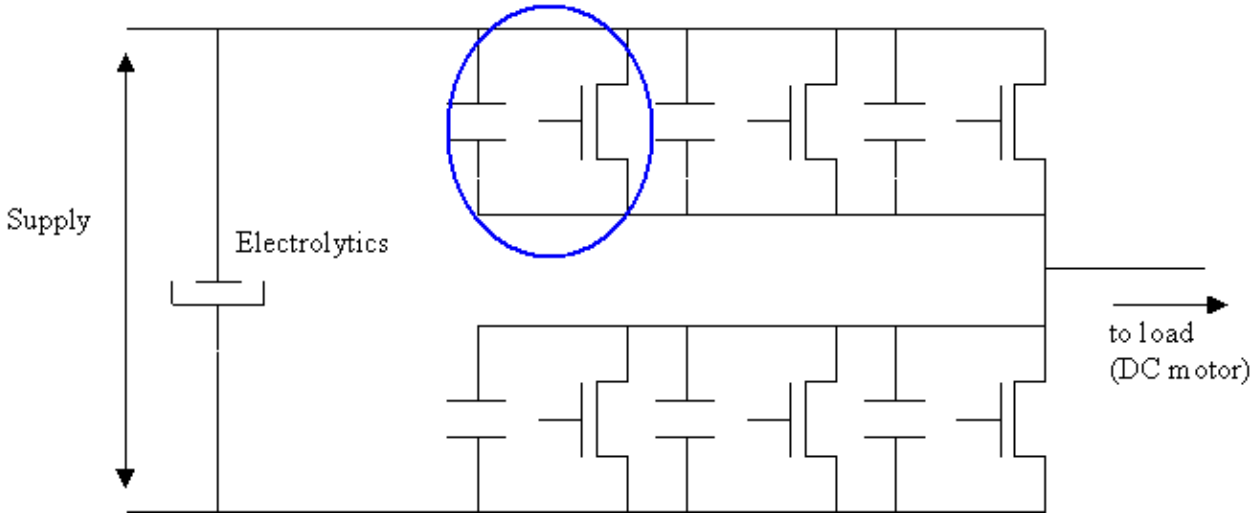


Figure 23: DC/DC converter where film capacitors and an electrolytic DC-link permit voltage peaks/ripples reduction

Below some examples of other input/output filtering schematics:

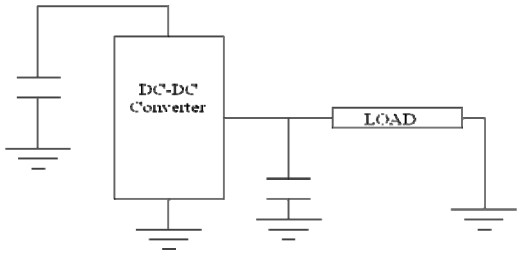


Figure 24 : input/output filtering of a DC/DC converter

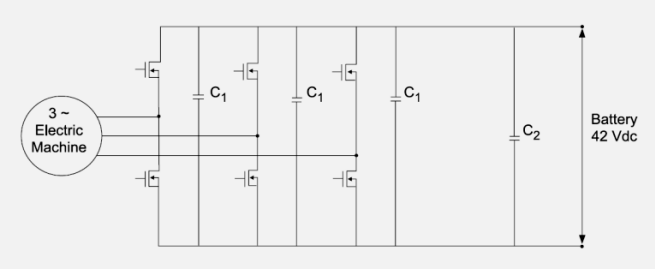


Figure 25: Input/output filtering on a AC/DC converter

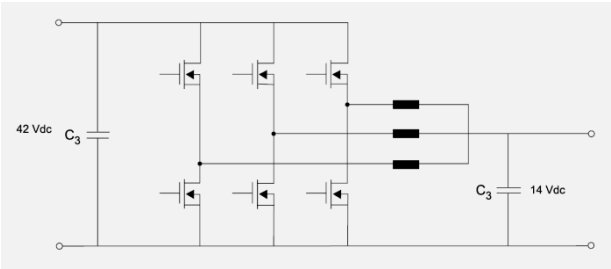


Figure 26: Input/output filtering on a DC/DC converter

In low-voltage applications (≤ 100 Vdc), capacitance requirement is in the range of 1µ - 100µF. Converters can anyway also work at higher voltages, so these capacitors have been developed up to 630 Vdc rated voltage. Furthermore, converters can be used in different equipment and possibly in extremely severe environments as automotive and marine.

For this reason, capacitors need to withstand high currents and to have good self-healing properties (being for example in parallel to a battery in automobiles) and need to withstand critical humidity conditions and intense vibrations. For all these reasons, PET dielectric is the choice.

Film capacitors are generally the typical component choice in these kinds of applications, thanks to their elasticity (robustness vs. PCB bending and severe vibrations), their "open" failure mode, their high reliability due to the self-healing and their long life expectancy.

2 - Performances of new naked stacked SMD PET film capacitors and of the jumbo naked stacked SMD PET film capacitors

In general, for mid-power applications (e.g. when an automobile battery is in parallel to the capacitor), film dielectric choice for SMD mounting is PET, due to its good self-healing, its high dielectric constant and its capability to withstand a reflow process (not the case of PP). An extension to the new naked stacked SMD PET release, already described, is the Jumbo Stacked Naked (JSN) SMD PET capacitor, that in 60.115 size at 63 Vdc can reach up to 82 µF. Higher capacitance values can be obtained in bigger sizes.

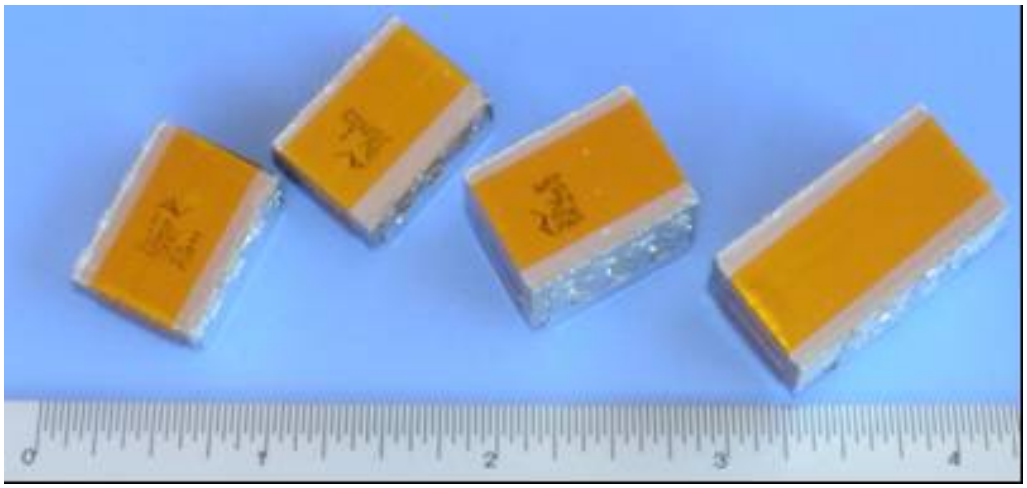


Figure 27: Jumbo Stacked Naked (JSN) PET capacitors

Lead frames can be provided in different shapes, according to the application requirements like vibration resistance or layout design needs.

Going back to the application level, usually low ESR and low ESL are crucial parameters. Several graphs and experimental ESR and Impedance measurements have been carried out (with different dielectric design technologies) on different capacitance values and voltages:

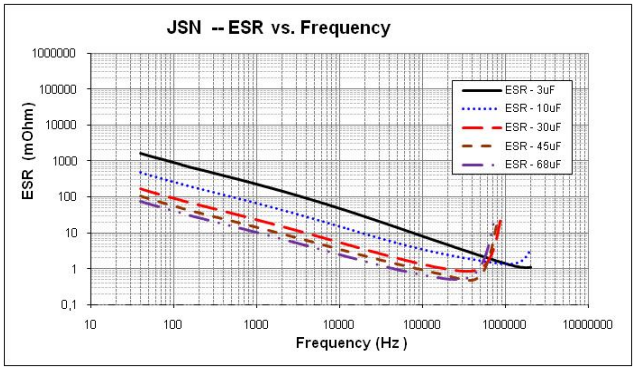


Figure 28: ESR vs frequency at 25°C

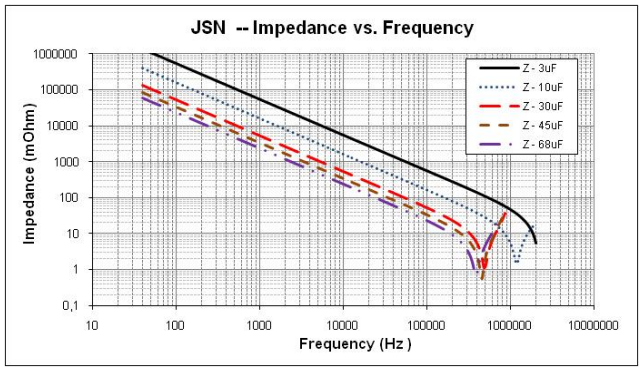
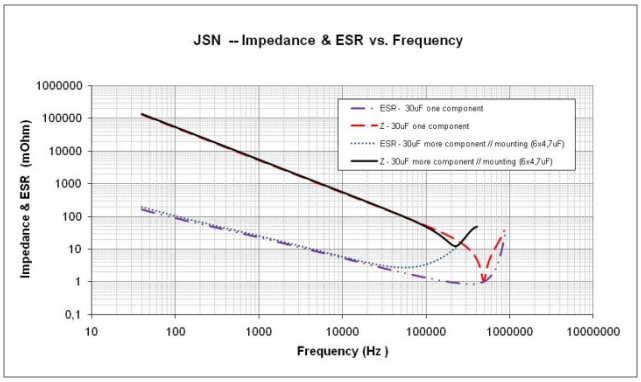


Figure 29: Impedance vs frequency at 25°C

In the below graphs, a comparison of ESR and Impedance values between a parallel connection of multiple components vs. one single component (of the same capacitance value) is showed. The single component shows higher resonance frequency with lower ESR:



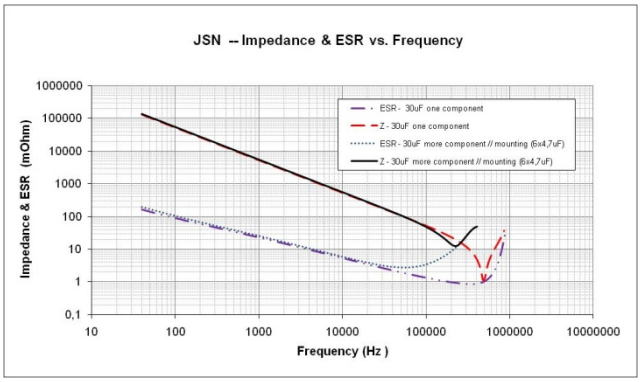


Figure 30 and 31: Comparison of ESR and Impedance vs frequency at 25°C of one component vs many components in parallel

The above measurements have been carried out measuring the ESR and Impedance with a 4 terminal system creating the contact as in the Figure 32 below for multiple components in parallel. For the single component, the contact has been applied on the middle of the lead frame.

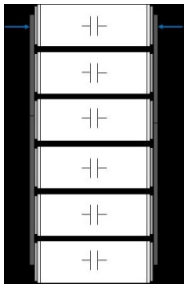


Figure 32: The four terminal contacts applied on the middle of the external component

In the graph in Figure 33, ESL values and resonance frequencies obtained with a vertical mounting have been compared to the values measured by mounting the capacitor horizontally (classical mounting):

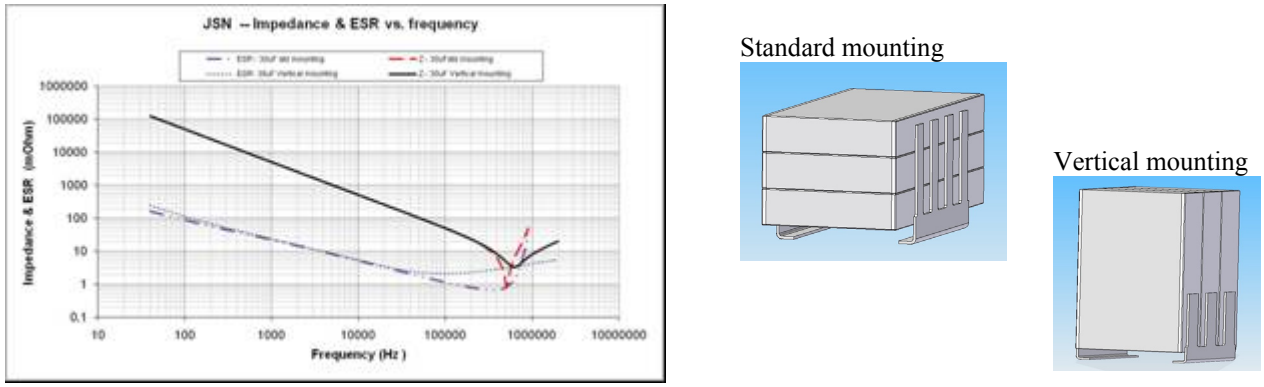


Figure 33: ESR and Impedance (Z) comparison between horizontal (standard) and vertical mounting

A single capacitor is built of thousands of layers connected in parallel through the two terminations.

The vertical mounting shows higher resonance frequency due to the fact that each single layer of the capacitor elements is vertical and the inductance (L) paths to each single layer are equal to the others. In the horizontal configuration, the L- path to each layer is different from the others due to the different height of the layers with respect to the PCB level.
The ESR of vertical mounting is higher because the connection is made only on the other end of the 2 terminations and not on the middle as happens on the standard mounting.

The developing of stacked naked SMD capacitors in PET has also extended the capacitance range per size (up to 12uF/63Vdc in 60.54) in comparison to existing stacked naked SMD PEN version (up to 4,7uF/63Vdc in 60.54). In the following graph the capacitance range of the Jumbo Stacked Naked SMD in PET is also included:

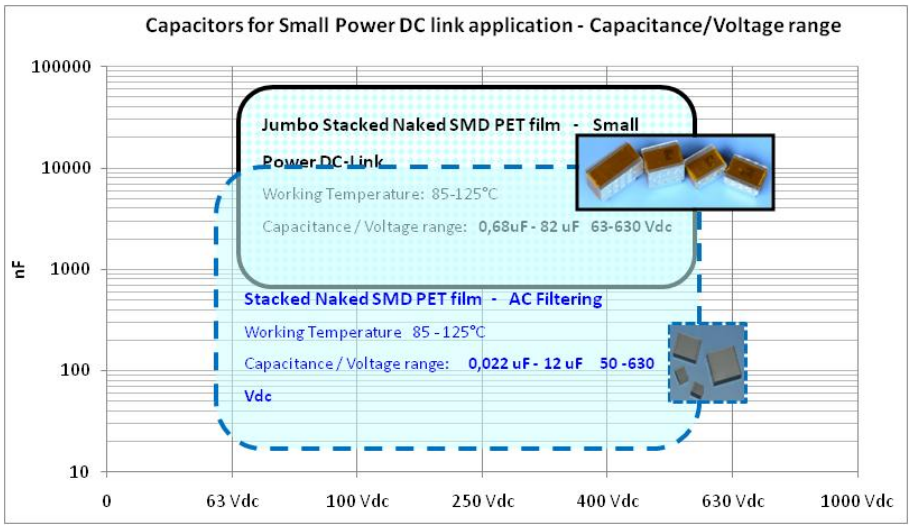


Figure 34: Capacitance ranges of Jumbo Stacked naked SMD PET and stacked naked SMD PET capacitors

Considering that these capacitors have been designed for automotive and marine environments, the following graphs of humidity resistance have been included:

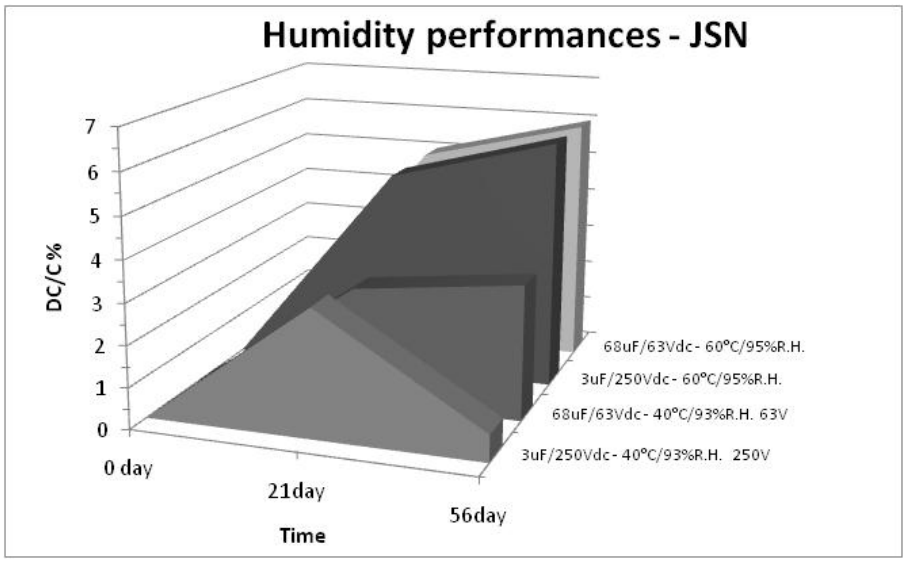


Figure 35: Humidity performances of Jumbo Stacked Naked SMD PET capacitors

The above graph shows an increase of the capacitance value within 56 days. Humidity, with its high ε_r value, penetrating inside the capacitor, increases the capacitance value. A capacitance drop is then due to a de-metallization process causing a decrease of the active area inside the capacitor (not reversible process). The fact that no capacitance reduction vs. the starting value has been observed, underlines the optimum results obtained with a naked capacitor design.

The humidity withstanding has been improved increasing the capacitors' compactness through the dedicated thermal treatment during the manufacturing process.

Since in converters the working frequency is usually between 1 kHz and 20 kHz, one important requirement is the maximum current, which the component can withstand either continuously or for a limited amount of time (duty cycle):

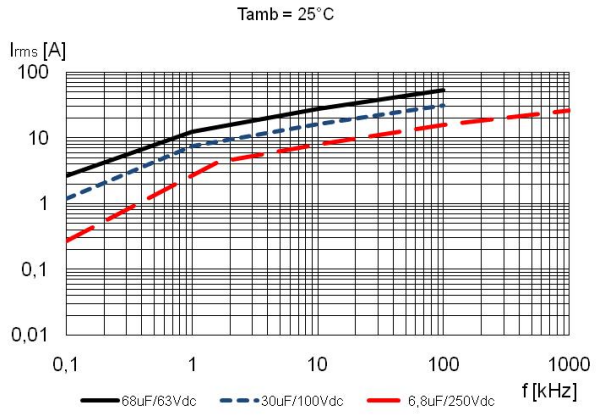


Figure 36: I_{rms} vs frequency at 25°C

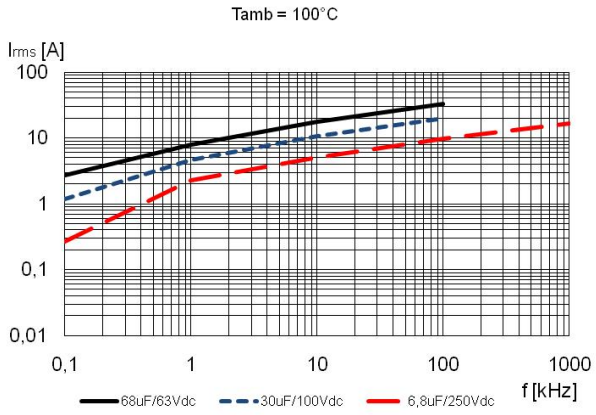


Figure 37: I_{rms} vs frequency at 100°C

An increase of the ambient temperature (e.g. from 25 to 100°C) decreases the permitted internal self heating of the capacitor (from 40°C to 25°C), explaining therefore the decrease of the maximum I_{rms} current value.

For a period shorter than the time necessary to reach the equilibrium between generated and dissipated thermal power, higher I_{rms} current can be applied according to following figures:

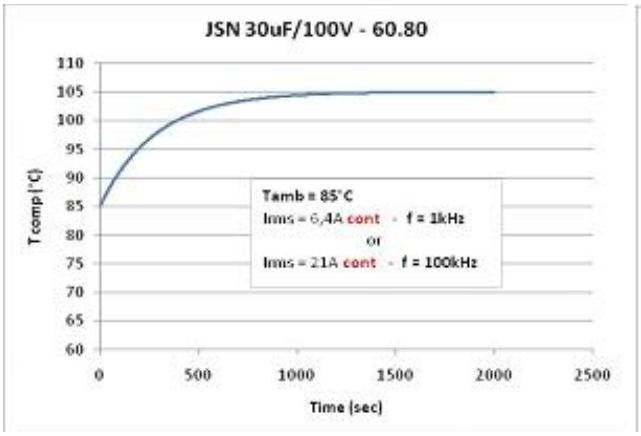


Figure 38: Self-heating with a continuous stable load

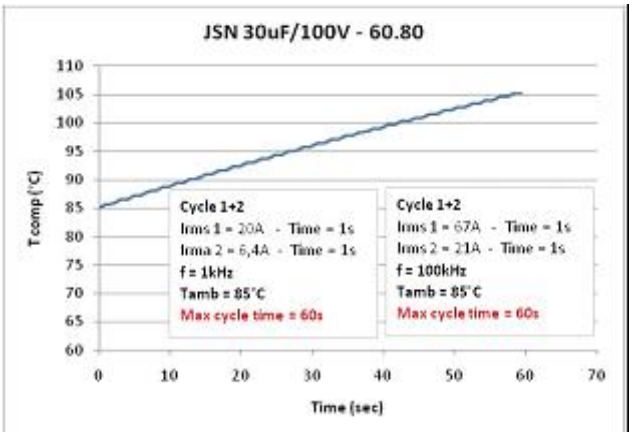


Figure 39: Self-heating with a duty cycle of 1s + 1s for 60s

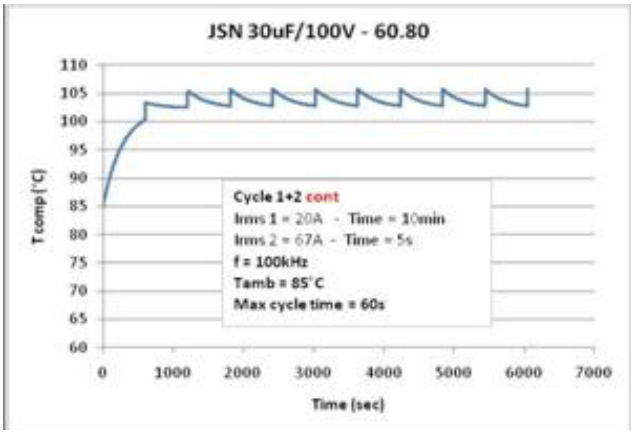


Figure 40: Self-heating with a 100% duty cycle

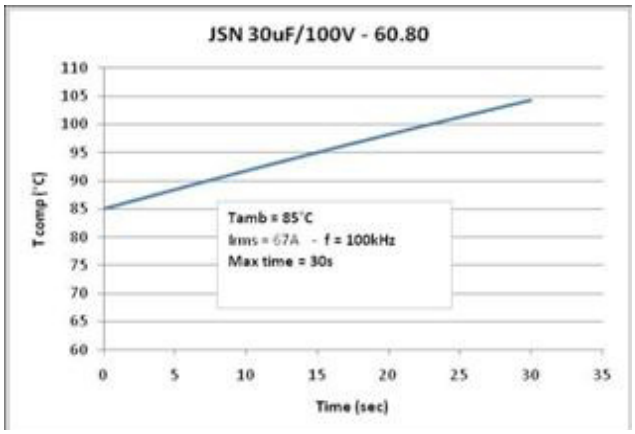


Figure 41: Self-heating for high current short timing

According to Figure 41, for short time period the increase of the temperature is quite linear, while it becomes a curve with an asymptote for longer periods.

IGNITER AND BOOST

1 - Introduction

This section will be focusing on the automotive Xenon headlamps application, for which the igniter and boost capacitors have been designed.

In comparison to conventional halogen headlamps, the Xenon system provides 200% more lighting, illuminating the road ahead and the curb side more effectively and brightly. The lighting on the road is similar to the daylight and is therefore close to the natural viewing conditions of human eyes. As a result, driving becomes more relaxing and safe. Xenon lamps need about 33% less power than halogen ones and they last nearly as long as the vehicle itself.

Presently a 35 W version is used in the automotive market. In many countries it is required by law that there is an automatic leveling and washing system (in order to prevent other road users from being dazzled and to ensure lenses are clean and have a good light distribution). These two integrated systems give a relevant contribution to the relatively high cost of the total Xenon headlamps light machines.

In the future a power reduction to 25W is foreseen, lower than the minimum limit to have a mandatory automatic leveling and a washing system in many countries. This will reduce the cost of the light machine, possibly increasing the diffusion of this technology in lower-priced car segments than the ones presently using Xenon lamps.

LED lamps, an alternative new technology, are already available in the market, but their mass production is foreseen in no less than 10 years due to the current additional technical features needed and the cost implied. A controlled bi-directional air flow system, including fans, is in fact needed in order to keep the right environment temperature and to have a good efficiency. This has a severe implication on the system reliability and on its cost.

Here is a brief explanation, how Xenon lamps work:

In order to have the ignition of the Xenon gas on the lamp, two main circuits are used:

- the first one is the ballast, that provides the right power and energy to the igniter circuit for the ignition (also in case of low battery level and cold temperature conditions)
- the second one is the igniter, whose task is the increasing of voltage and current in order to create arc inside the Xenon gas and turn the lamp on

In the schematic circuit below, C_1 and C_2 are the boost capacitors (also referred to as ballast capacitors) while C_3 is the igniter capacitor. In the market there are also layouts including one boost capacitor only:

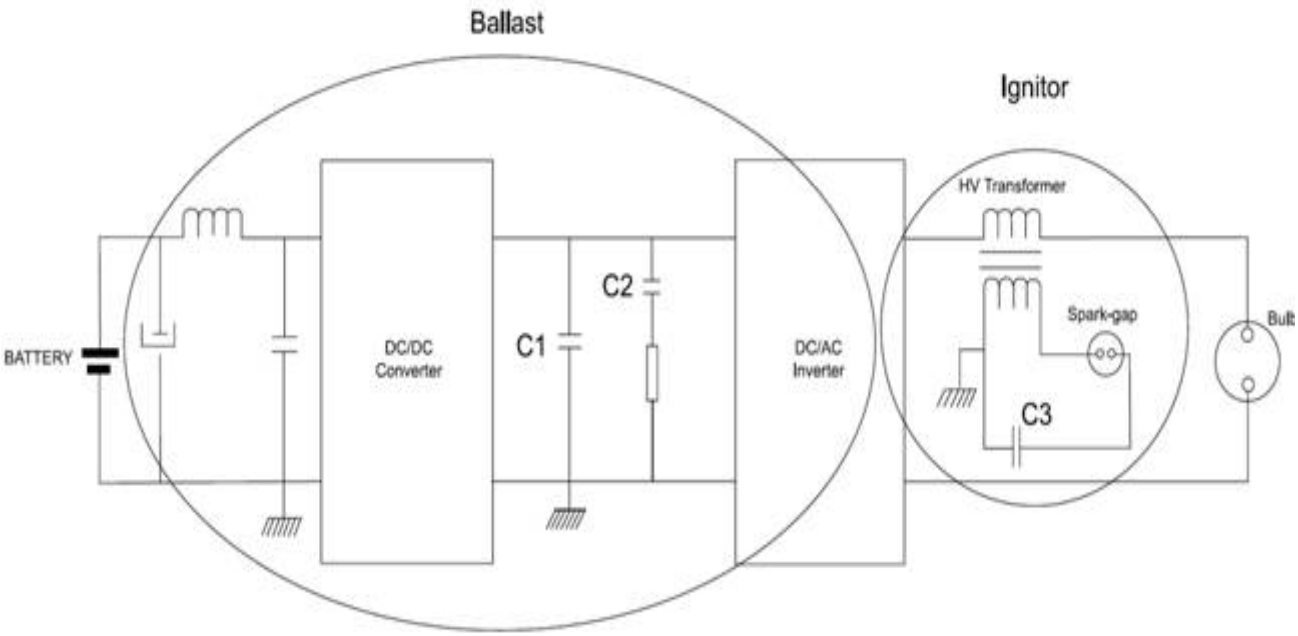


Figure 42: Schematic of the ballast and igniter circuits on high intensity discharge - (HID) - Xenon headlamps

2 - Igniter application: Design and performances of new naked stacked SMD PEN film capacitors

A dedicated Naked Stacked SMD capacitors range, for this special application, has been developed:

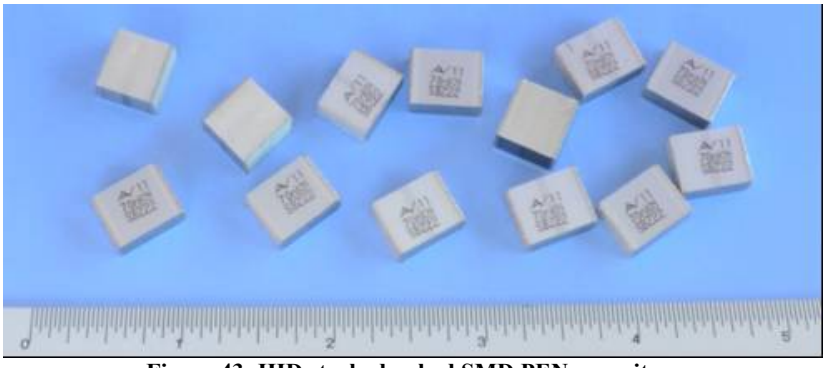


Figure 43: HID stacked naked SMD PEN capacitors

The capacitance range in the application is presently between 70 and 120 nF at 1.000 Vdc. In the Table 5 below the main igniter capacitor characteristics are listed:

Table 5: Main requirements of the igniter capacitor

Igniter capacitor electrical characteristics	
Capacitance value	70nF - 80nF - 120nF
Size	50.40 - 45.43
Max temperature of the reflow	245°C
Operating temperature (3000h)	-40 °C to +155 °C
Operating temperature (300h)	+155 °C to +170 °C
dv/dt	up to 8500 V/µs
Max allowed voltage during ignition	1250 Vdc
Number of ignitions	200.000
Damp heat 60 °C – 95 % R.H. 500h	Max $\Delta C = \pm 7$ %

Igniter capacitor needs to withstand high voltages, very high peak current (8.500 V/µs), high working temperature, a LF reflow process and critical humidity environment. Especially due to the very high peak current requirement, stacked technology has been chosen instead of wound technology. This for two main reasons:

- a stacked capacitor is built of several hundred independent layers (small capacitors) all put in parallel. If one layer disconnects because of high electric stress, the capacitance is slightly reduced, but the remaining layers' connections are safe. In a wound capacitor on the contrary, in case a layer disconnects, the capacitance value does not change, increasing the current through the remaining contacts (avalanche process) leading at the end to an open capacitor.
- thanks to the capacitance decrease in case total / partial disconnection of a layer in a stacked capacitor, it is quite easy to detect potentially weak capacitors during the electrical testing included in the manufacturing process or during the assembling / final testing in Customer's process.

Considering the requirement of the working temperature up to 170 °C, PEN has been chosen as dielectric.
In the following picture, both voltage and current waveforms applied on the igniter capacitors during the ignition are shown:

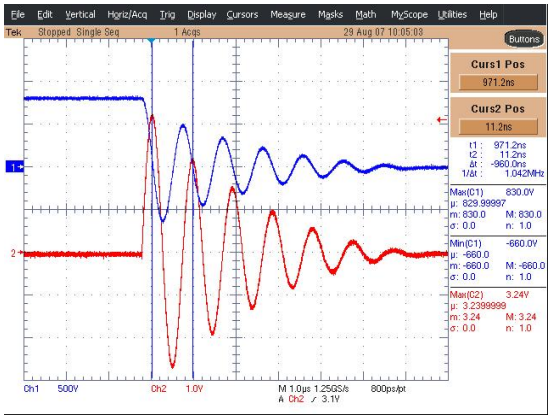


Figure 44: Voltage and current on igniter capacitor during the ignition of the Xenon lamp

The above graph demonstrates the great difference in terms of electrical stress between the ignition phase and steady working phase, after the lamp has been turned on. For this reason, the reliability of this capacitor is not measured in hours, but in ignition cycles. The typical requirement from the market is 100.000 to 200.000 cycles.

In the following graphs performance under high peak current stress is showed. It is important to underline that the current flows on a single metalized film capacitor instead of a double metalized one: this design choice has decreased the dimensions of the igniter capacitor:

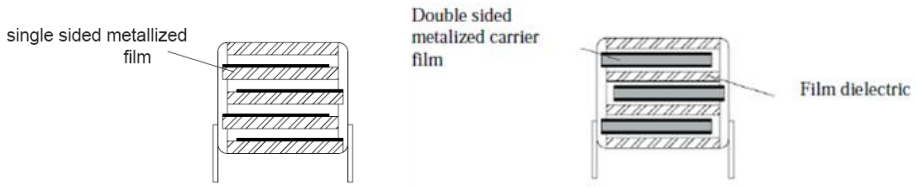


Figure 45: single and double metalized technologies

In order not to decrease the efficiency of the igniter circuit, high capacitance stability is required. In the Figure 46 distribution of the capacitance deviation is showed after 200k cycles with a voltage of 1000V and a peak current equivalent to 8500V/µs (600 A with a capacitance value of 70 nF):

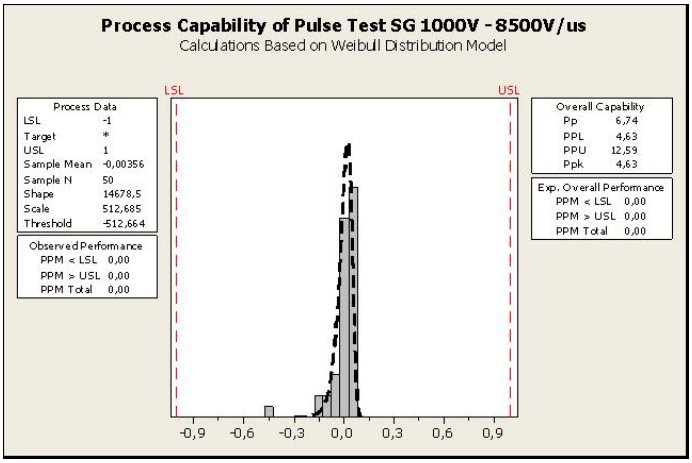


Figure 46: Distribution of the capacitance deviation after a charge/discarge test at 1000 V and 8500 V/µs

In order to check the trend of the capacitance deviation in relation to the number of ignition cycles, the following charge-discharge test has been performed with the same current value as in the preceding test (600 A on a capacitance value of 70 nF). According to Figure 47 the capacitance trend is quite linear in a semi-logarithm graph:

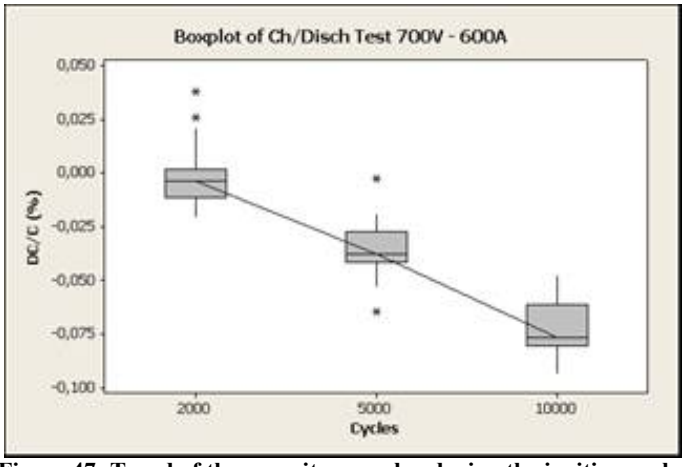


Figure 47: Trend of the capacitance value during the ignition cycles

As specified before, considering the harsh automotive environment (especially inside headlamps), several tests in severe humidity conditions have been carried out:

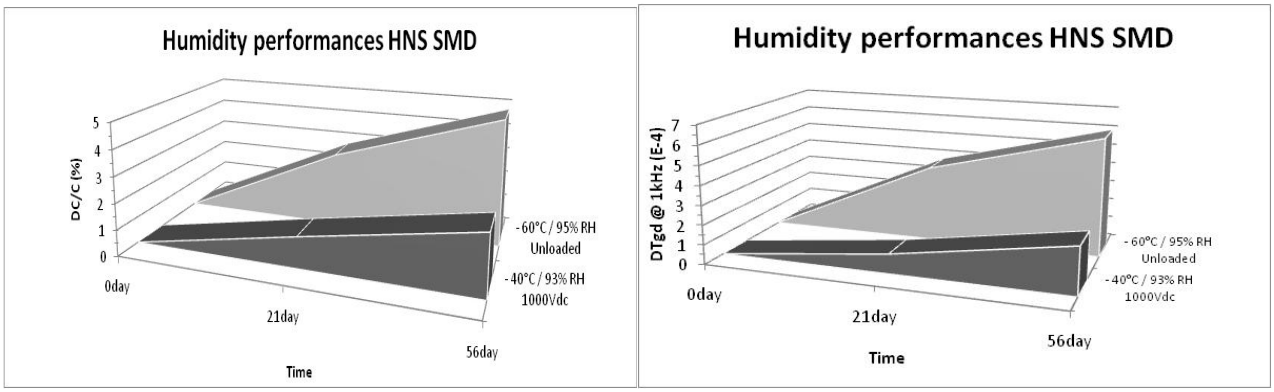


Figure 48 and 49: Humidity performances of the igniter capacitor (named HNS) in terms of capacitance and dissipation factor

As in the small DC link capacitor section graphs, no significant de-metallization effects, within 56 days, have been observed.

A critical parameter for the igniter capacitor is the voltage withstanding, especially after the LF reflow process. In order to monitor the igniter capacitor performance from this point of view, a voltage value is recorded to indicate the first occurrence of partial discharges when a constant voltage ramp-up is applied on the capacitor (this procedure is referred to as First Break Down Voltage - FBDV - test). What is measured in this way is not the real "break-down" of the dielectric, but only a partial discharge that, in some cases, can create only very small and brief current flow.

In the graphs in Figures 50 and 51, FBDV results have been recorded after reflow process with two different peak temperatures (233 °C and 245 °C). Considering that in the application the discharge voltage level of the spark gap is 800 Vdc with a tolerance of ± 20 %, the lower specification limit (LSL) inserted in the graph below, to evaluate the PPM performance, is 960 V. One of the excellent successes of this design is the negligible differences in terms of FBDV test performances after the reflow process with different peak temperatures:

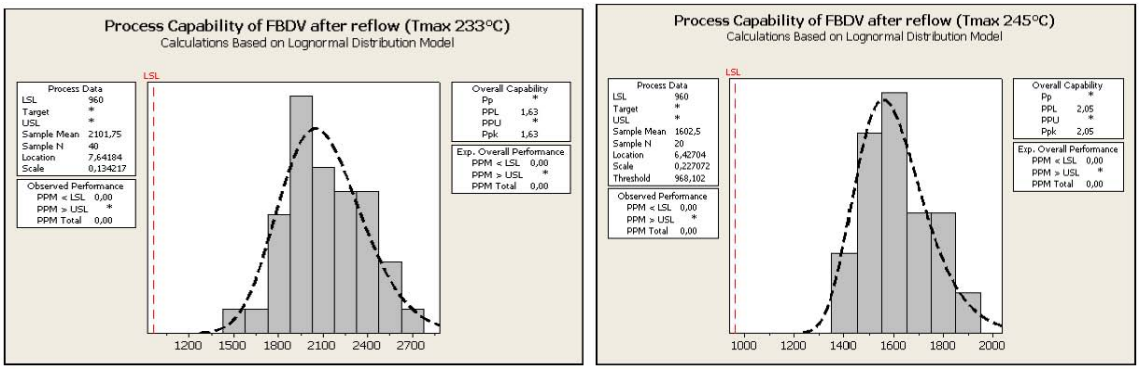


Figure 50 and 51: FBDV test on the igniter capacitor after a LF reflow process with different peak temperatures (233 °C and 245 °C)

3 - Boost application: Design and performances of new naked wound SMD PEN film capacitors

For the Ballast application, another dedicated naked SMD PEN capacitor family has been developed, focused on withstanding high voltage peaks during the ignition phase of the lamp. This capacitor family has rated voltage lower than peak voltage in the application. Therefore, it offers smaller dimensions with respect to the standard general purpose stacked naked SMD PEN capacitors family.

The size aspect was the biggest challenge for a successful design as the available space on the board is very limited due to the continuous miniaturization activities running on automotive appliances.

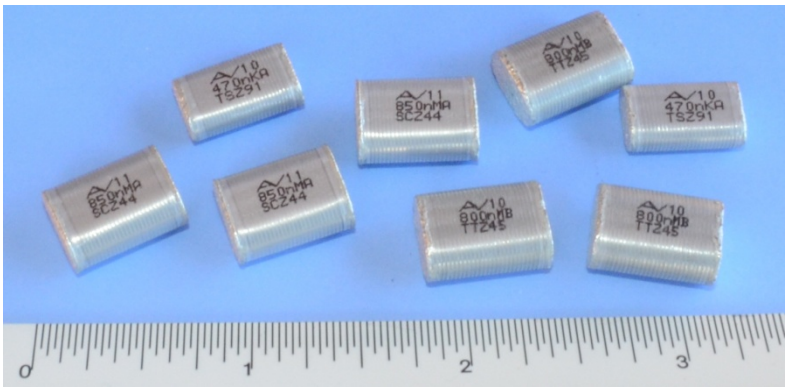


Figure 52: SMD wound naked capacitors in PEN

In the Table 6 below the main boost capacitor characteristics are listed:

Table 6: Main requirements of the boost capacitor

Boost capacitor electrical characteristics	
Capacitance value	270 nF - 1.200 nF
Size	50.40 - 60.40 - 60.54
Max temperature of the reflow	245 °C
Operating temperature range	-55 °C to 125 °C
Max allowed voltage during ignition (60 ms)	480 Vdc
Number of ignitions	Up to 500.000
Damp heat 60 °C – 95 % R.H. 500h	Max $\Delta C = \pm 7$ %

The main requirements are small dimensions, withstanding of voltage peaks, critical humidity environmental conditions and LF reflow process.

Wound technology was chosen, on this application, for its intrinsically good performances in withstanding voltage peaks. This intrinsic property is mainly explained by the fact that wound capacitors do not have a cutting surface as stacked capacitors. In this case, the peak current is not critical, and so the risk described in the igniter section is extremely limited (overloading of current on not detached layers in wound capacitors).

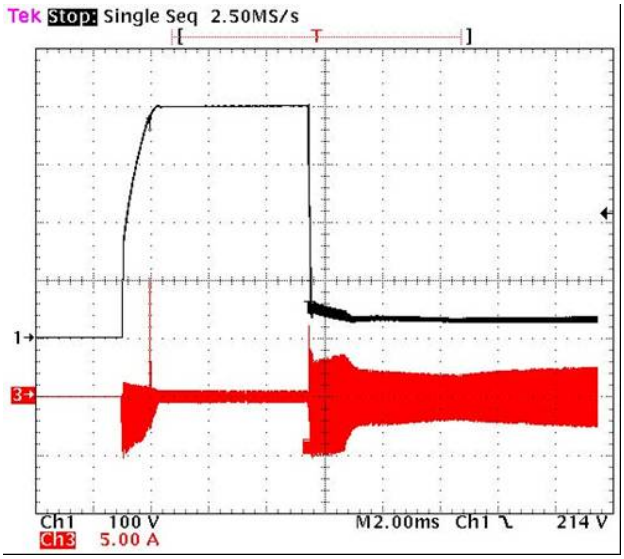


Figure 53: Voltage and current in the boost capacitor during the ignition of the Xenon lamp

Since the withstanding of voltage peaks and the dimensions were the main application requirements, R&D efforts have been focused on these characteristics, with the final result of reducing the film thickness by about 33% vs. the one used in the general purpose SMD naked stacked PEN capacitor family. This reduces therefore dramatically the volume of the capacitor.

This result has been obtained with R&D design activities in pre-treatment of film material, and in winding, pressing and thermal treatment manufacturing phases.

The simultaneous reduction of the volume shown in Figures 54 and 55 is highlighting the design improvements:

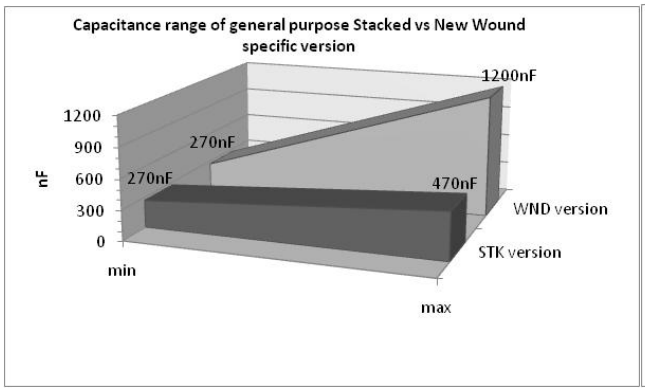


Figure 54: Increasing of the capacitance range in 60.54 size

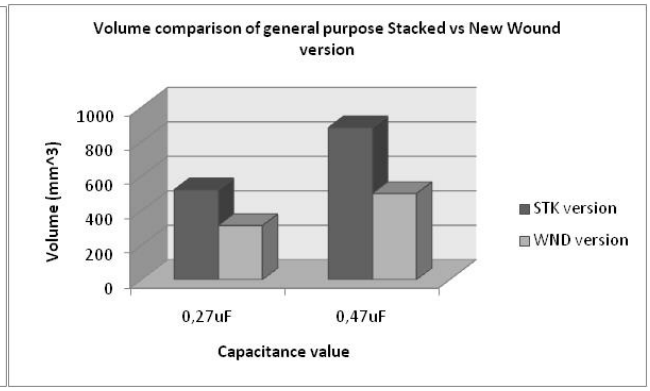
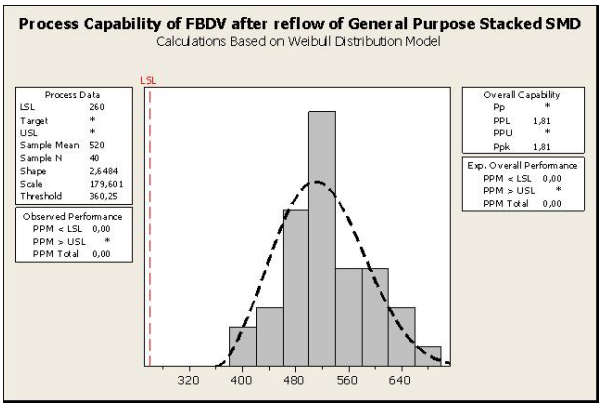


Figure 55: Volume comparison between stacked and wound

In order to increase safety vs. voltage withstanding, FBDV tests have been carried out, as was done for the igniter capacitor:



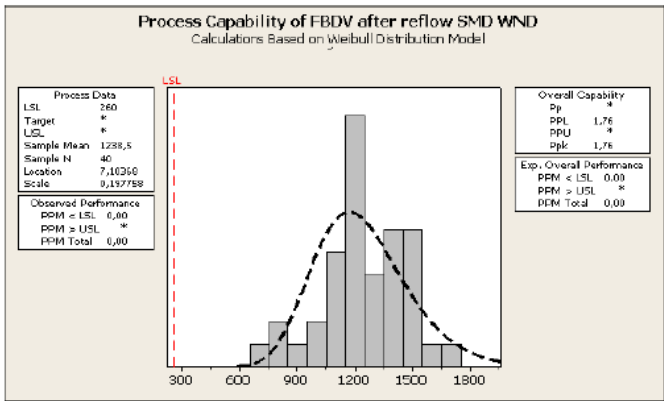


Figure 56 and 57: FBDV test on general purpose stacked PEN SMD version compared to the new wound PEN SMD version

The above comparison was made using the same film thickness (4µm) and therefore the same rated voltage (250 Vdc). According to Table 6, the peak voltage is up to 480 V. Therefore, from the graphs in Figures 56 and 57 it is evident that the general-purpose naked stacked SMD version, rated 250 Vdc, is not able to work in this application while the new wound release is.

The importance to have stable FBDV test performances, before and after a LF reflow process, amplifies the choice of PEN as dielectric.

As in the case of the igniter capacitor, the capability to work in critical humidity conditions is extremely important for the boost capacitor design:

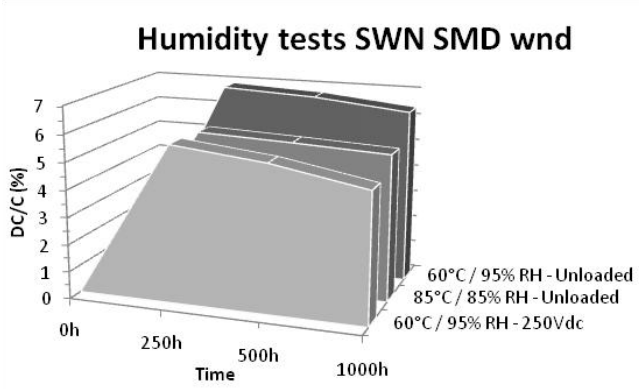


Figure 58: Humidity performance of the new naked wound SMD version (named SWN)

The boost capacitor's working temperature is currently up to 125 °C, but with the upcoming new 25 W version, the integration between the igniter and the ballast circuits might be an option. For this reason, the boost capacitor's working temperature can rise up to 150°C, validating even more the choice to use the PEN dielectric.

SUMMARY

Besides the standard film capacitors families, designed to be used in general purpose applications with general requirements, the high demand of miniaturization on new equipment and electronic concepts, even in harsh environments as automotive and marine, has increased the need to design dedicated components for particularly demanding applications, where the focus is to maximize the performance of specific electrical/physical parameters.

Naked components are usually the first choice when looking for miniaturized SMD film capacitors, but this means great efforts in the design of the capacitors' manufacturing process, starting from the selection of the film dielectric, then proceeding with the design of the most appropriate thermal treatment for the dielectric film material.

It has been shown in this paper how SMD naked film capacitors are now capable of working in severe environments and can withstand LF reflow processes keeping their renowned excellent electrical characteristics and their reliability. This is an important factor to be considered by Engineers when making their components selection.

For SMD film capacitors, when all manufacturing technologies/versions are an option (wound and stacked technology, naked and in-box versions, possibility to use all available films), the selection of the film dielectric and the manufacturing technology is generally made through the following steps:

1. LF reflow: PPS → PEN → PET. PPS and PEN are the films with the biggest safety margins vs. the LF reflow peak temperatures, while PET shows some restrictions vs. LF reflows
2. Mid power application (e.g. in parallel to a battery) → PET; PEN for medium-low power applications and high temperatures requirement (≥ 150 °C)
3. Working temperature: PET (Vdc ≤ 100 V), PEN (Vdc ≥ 250 V) up to 150°C; PEN from 150 °C up to 175 °C;
4. Precision capacitors: PPS (up to 175 °C)
5. Dimensions: Protected version (SMD in box), if the miniaturization requirement is not critical for the application, naked version otherwise
6. High current peaks → Stacked technology
7. High voltage peaks → Wound technology

Combined requirements (e.g. high voltage peaks and high current peaks) are to be analyzed case by case to create a specific design.

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