Streamlining PCB Assembly and Test NPI with Shared Component Libraries

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Abstract

PCB assembly designs become more complex year-on-year, yet early-stage form/fit compliance verification of all designed-in components to the intended manufacturing processes remains a challenge. So long as librarians at the design and manufacturing levels continue to maintain their own local standards for component representation, there is no common representation in the design-to-manufacturing phase of the product lifecycle that can provide the basis for transfer of manufacturing process rules to the design level. A comprehensive methodology must be implemented for all component types, not just the minority which happen to conform to formal packaging standards, to successfully left-shift assembly and test DFM analysis to the design level and thus compress NPI cycle times. The elements of such a solution include implementing de-facto standards for package and pin-type classifications, as well as DFM analysis rules that are associated with these classifications and the intended manufacturing processes. The resulting solution enables the transfer of DFM rules from the manufacturing process expert to the design and NPI engineers on the design side responsible for verifying manufacturing-process compliance of new product designs. This paper will demonstrate the technological components of the working solution: the logic for deriving repeatable and standardized package and pin classifications from a common source of component physical-model content, the method for associating DFA and DFT rules to those classifications, and the transfer of those rules to separate DFM and NPI analysis tools elsewhere in the design-through-manufacturing chain resulting in a consistent DFM process across multiple design and manufacturing organizations. Following establishment of a common source of component definitions and classifications, rules-based generation of assembly-level machine libraries is enabled from the same source that drove the DFM process, resulting in right-first-time launch of a new product into the manufacturing process.

Introduction

The principles of lean manufacturing, “getting it right first time”, minimizing waste and unnecessary manual interaction, are all familiar and generally accepted as contributing factors toward cost reduction and quality maximization. In that context, this paper will examine two specific engineering-process aspects of introducing a new PCB design into assembly manufacturing and the technical barriers to be overcome to make the processes as lean as possible. The two engineering processes to be discussed are:

1. Performing design-for-assembly (DFA) verification on a new product design, as early as possible in the product lifecycle, and in any case before transferring the design into manufacturing.
2. Preparing assembly-line machine library content for fast set-up.

Before getting into the technicalities of the two topics and how they are related, it is worth first considering the business environment of PCB manufacturing. It is now about 20 years since PCB assembly manufacturing began to be outsourced in a major way, with the resulting rapid growth of the now well-known EMS and contract manufacturers. Before the outsourcing revolution, when design and manufacturing operations were generally vertically integrated, it was common to see CAD/CAM engineering processes being set up and maintained by electronics OEMs, depending for their success on internally defined library standards, a specific and relatively narrow range of manufacturing processes, and plenty of in-house proprietary software to link it all together. By contrast, today’s challenge is to take full advantage of the outsourcing opportunity, the choice, the flexibility, and the cost-competitiveness, without losing the advantage through engineering-process inefficiencies related to discontinuities in CAD/CAM software, data flows, and libraries between the customer (the design organization) and the suppliers (the manufacturers). To make matters worse, the typical manufacturer of today will serve dozens, if not hundreds, of design-customers, and the design organization may use dozens of EMS providers. This many-to-many interface between design and manufacturing tends to drive engineering processes toward standardized “lowest common denominator” workflows that are relatively manual, error-prone, and slow. These workflows are certainly somewhat “standard”, but they are far from lean, in terms of minimizing waste and maximizing consistency through automation.

The two engineering processes described in this paper are specifically designed to enable a high degree of production-portability between a product’s design organization and multiple manufacturing facilities and processes.

Portability of DFA

Design for assembly DFA) refers to the dimensional analysis of a PCB design to check its compatibility with the intended manufacturing processes. Figure 1 shows illustrations of two specific DFA analysis checks: one checking the pin-to-pad distances against the rules of the reflow process, the second checking component-to-component spacing against the access-requirements of the rework process. The variety of rules typically scales with the range of intended assembly and test processes, as well as the number of component types or combinations of component types.

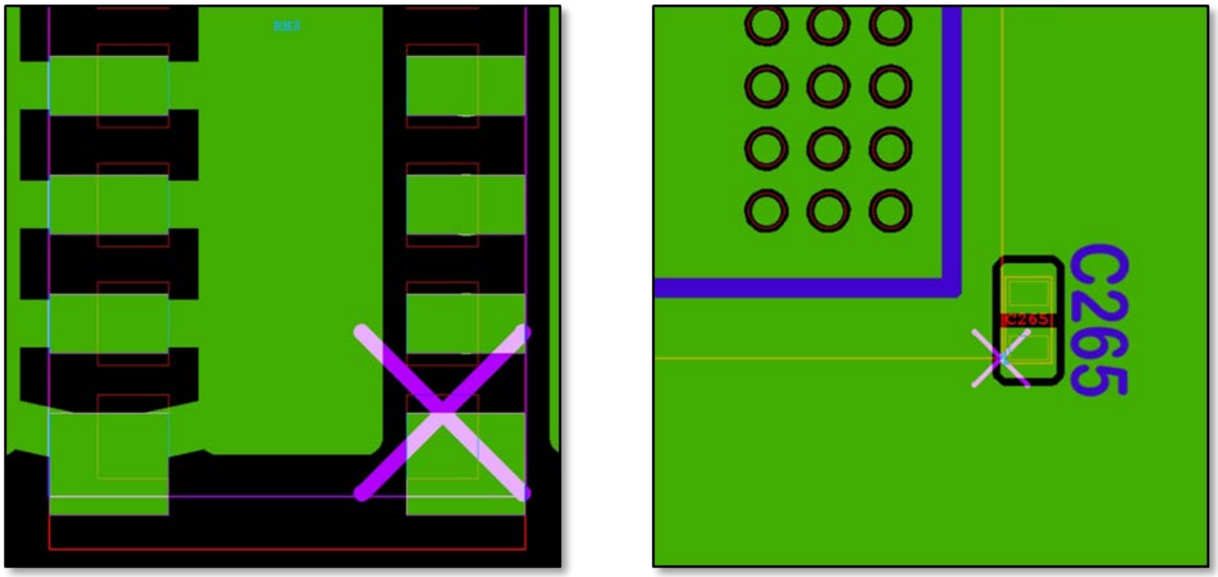


Figure 1: Two DFA checks: pin-to-pad analysis (left), and component-spacing analysis (right).

Now consider the DFA business process between a designer and a manufacturer, as illustrated in Figure 2. The designer has responsibility for the definition of the product, whereas the manufacturer is the owner of the manufacturing processes and the knowledge of their limitations relative to the characteristics of the products being manufactured.

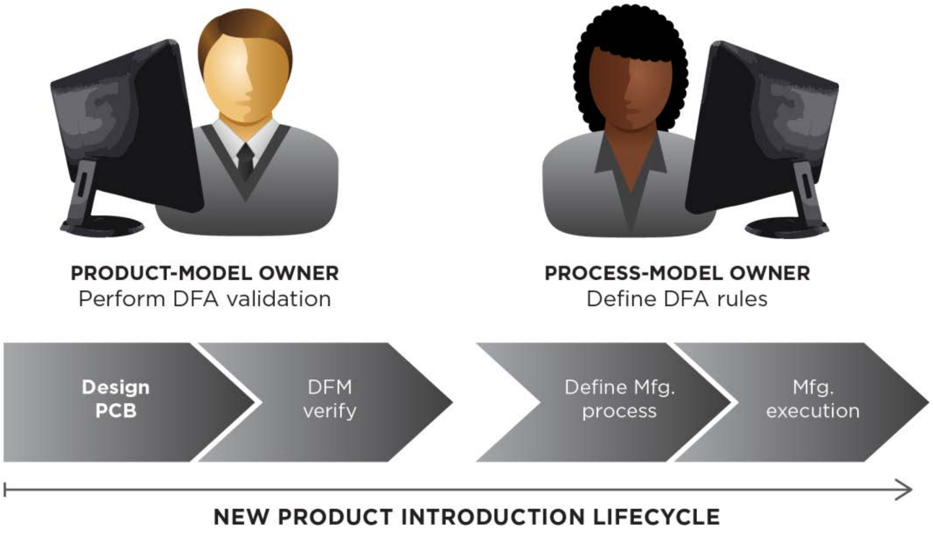


Figure 2: Outsourcing separation between design responsibility and manufacturing-process responsibility.

The designer's interest is to design the product so it is optimally manufacturable by the widest range of manufacturing suppliers. To be as lean as possible, the DFA validation process should be carried out in one place, on the design side, before handing the product to the manufacturers for production. But unless there is a formal common language for defining the product-model and the rules to be applied, the DFA process cannot be left-shifted from the manufacturing level into the design domain.

Figure 3 shows a simple real-life example of what happens when the designer is looking at the product with the design library, and the manufacturer is looking at the product with the manufacturing library. The component is the same, but its modeling is different. On the design side, the library sizes the pin of the component according to the pad it is standing on, whereas the manufacturing library sizes the pin according to the actual pin that is part of the component that will actually be placed on the board. Any communication between the designer and the manufacturer about what is an acceptable pin-spacing is meaningless unless a common modeling of the component is supporting the discussion. The same applies to the DFA rules themselves, unless the rules have the same meaning at both ends of the DFA process, the process will bring incorrect results and be of no value.

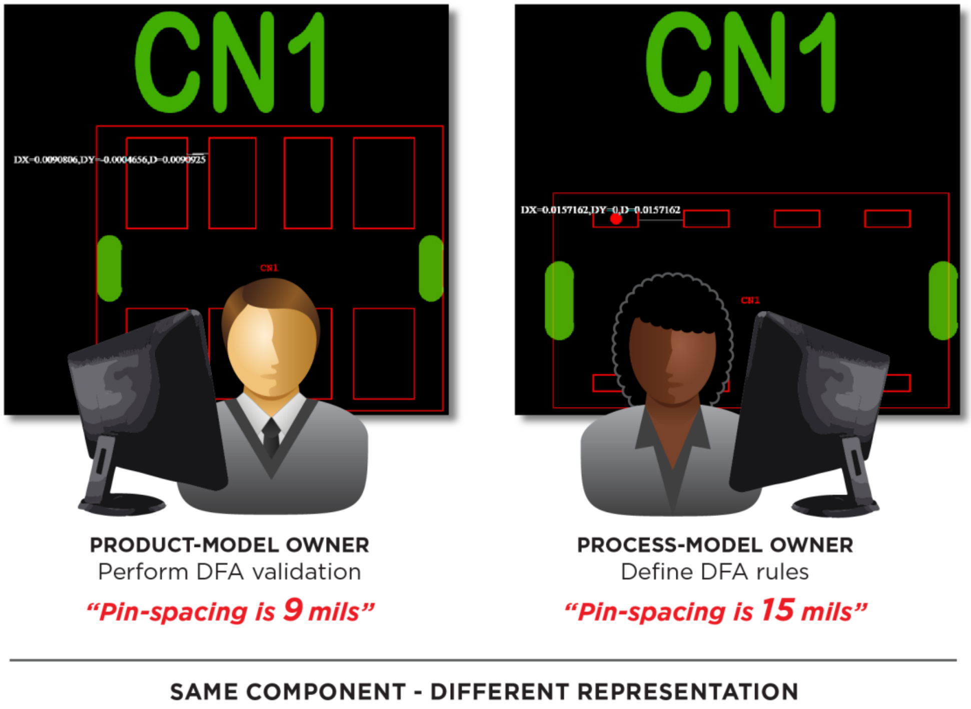


Figure 3: Outsourcing the need for a shared standard for component models.

First Requirement

The previous examples have shown how the models of the components must be standardized across the DFA workflow. The first assumption is that existing formal standards such as EIA, IPC, or JEDEC would meet the need. Assuming a reliable source of content could be found to deliver component models according to the standards, all mapped to their commercially purchasable part numbers, the standards approach would have had obvious benefits. However, we discovered, when examining the master parts lists of major DFA practitioners, barriers to a scalable solution based purely on the formal standards.

a) There are PCB-mounted components that do not conform to a standard of any kind. Figure 4 shows several examples of commercially available components that cannot be described by the JEDEC standard.

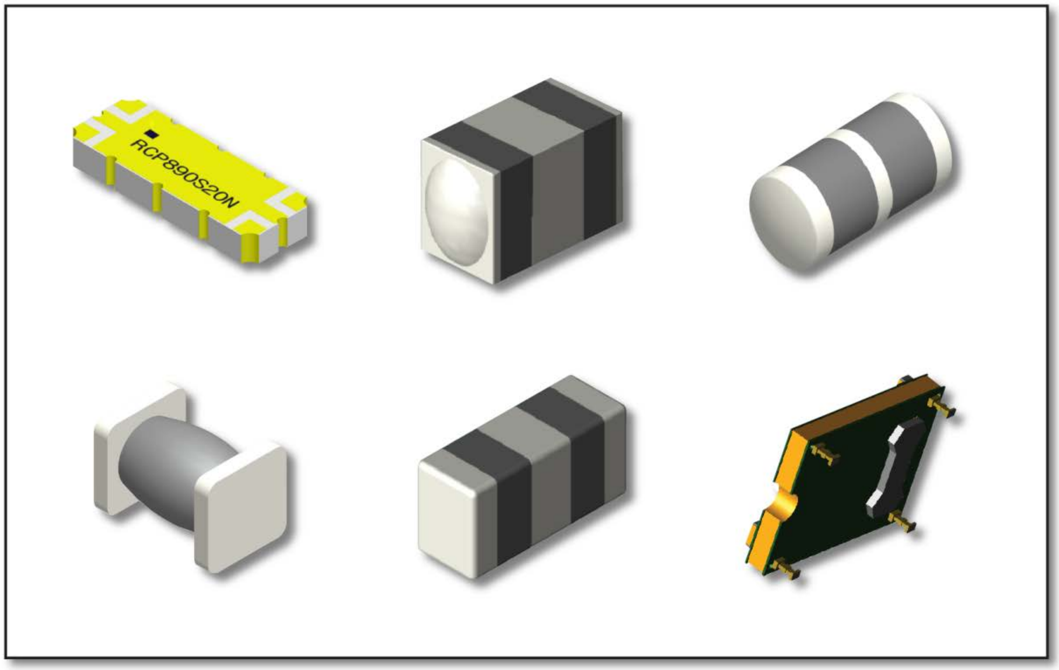
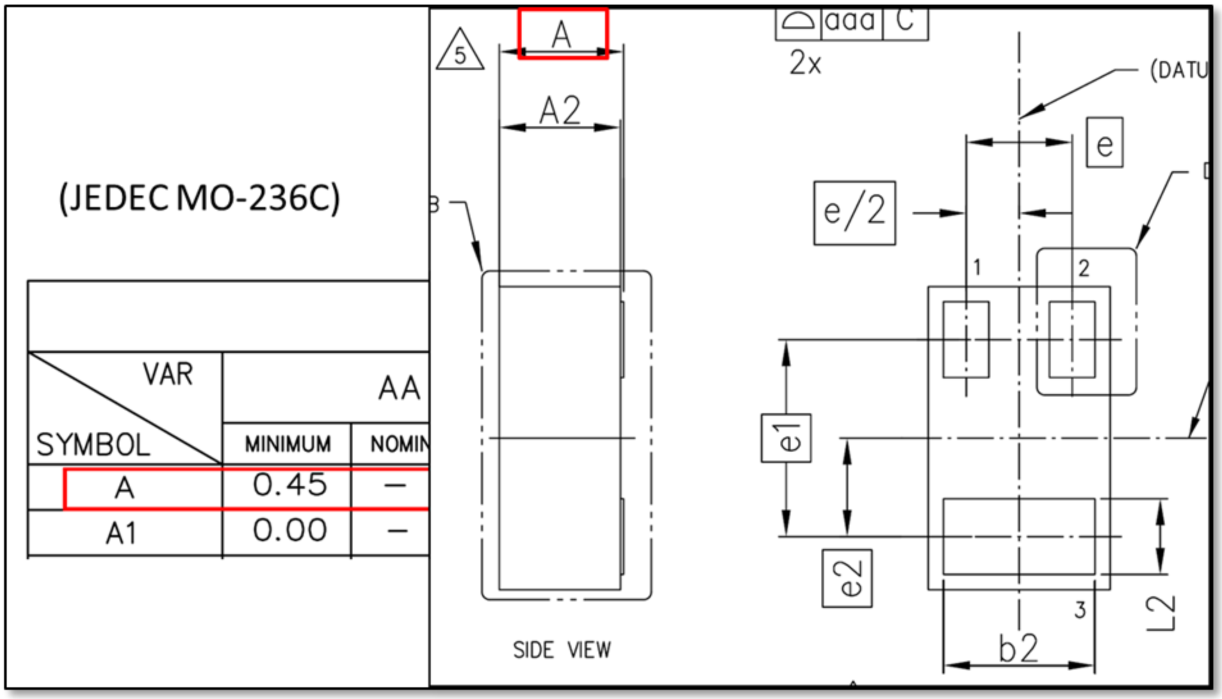


Figure 4: Formal component-modeling standards do not cover all purchasable parts.

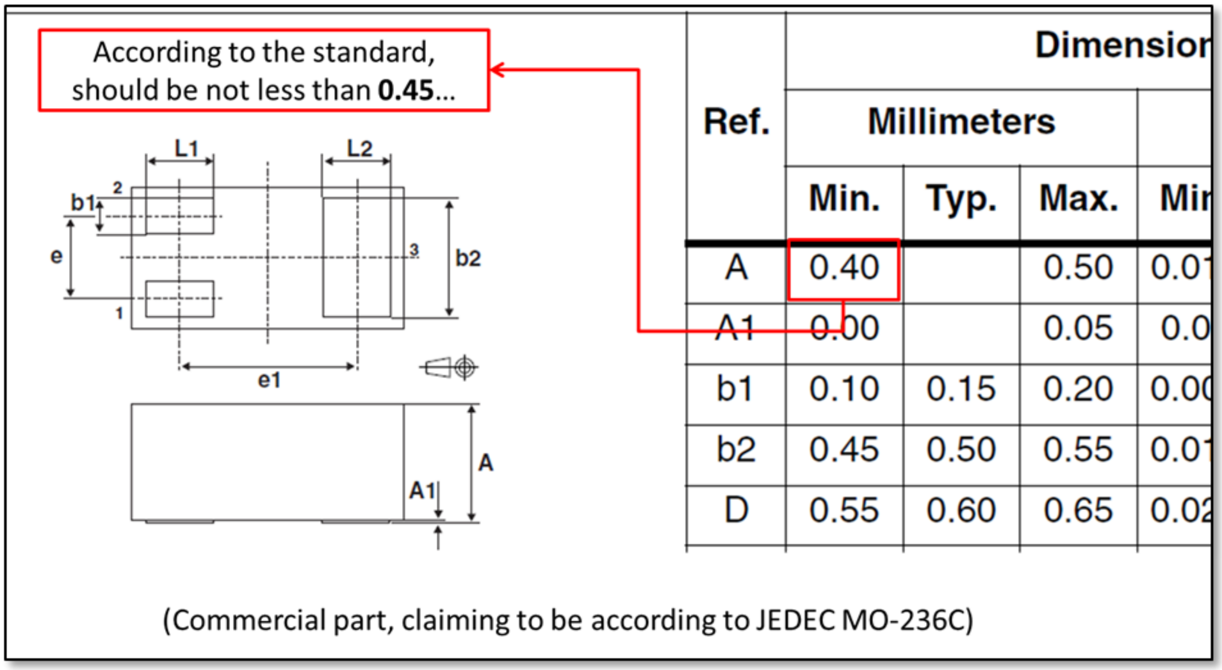
b) We found examples where the component manufacturer may declare that the component conforms to a standard, but in reality some of the dimensions are outside the tolerances set by the standard. Figure 5 shows one such example where some of the dimensions are outside the limits set by JEDEC. The size of the deviations may be small, but they could be enough to cause DFA violations to slip through into manufacturing; and in any case, a component is either within tolerance of not. We found that, from a sample of some 20,000 component package models of chip-style components that you would expect to be modeled by JEDEC in the "0402" or "0603" range of categories, approximately 20% were impossible to map correctly to the standard as defined. Therefore, the standards designation is not enough; a full graphical representation of the component and its pins is required.



(JEDEC MO-236C)

VAR SYMBOL	AA	
	MINIMUM	NOMIN
A	0.45	–
A1	0.00	–

Figure 5a: According to JEDEC MO-236C, minimum component body height is 0.45 mm.



According to the standard, should be not less than **0.45**...

Ref.	Dimension			
	Millimeters			
	Min.	Typ.	Max.	Mi
A	0.40		0.50	0.01
A1	0.00		0.05	0.0
b1	0.10	0.15	0.20	0.00
b2	0.45	0.50	0.55	0.01
D	0.55	0.60	0.65	0.02

(Commercial part, claiming to be according to JEDEC MO-236C)

Figure 5b: A commercial part, claiming to conform to JEDEC MO-236C, but actually does not conform.

The second prevailing assumption, especially in the design community, is that the library of the PCB layout system should be used for the purpose of DFA. From the standpoint of the designer, such an idea has obvious attractions. But the design library fails the suitability test for four reasons. Firstly, design library content is not systematically constructed according to any level of standardization that is recognizable outside the boundaries of a specific design organization. The rules and meaning of the design library content is defined and owned by the librarian, and it is highly likely to be inconsistent with the library content from a library in another organization that is under the control of a different librarian.

Secondly, the design library usually does not model the physical pin of the component at all, focusing instead on the component body outline and the related pad stacks; yet it is the relationship of the physical pin to the pads and solder mask openings that mainly determines the quality of the soldered joints that will be created in the manufacturing process.

Thirdly, the design library component model is usually an approximation based on all alternative purchasable parts that may be placed there (according to the master parts list or AVL), thus it cannot be said to support the DFA analysis of any specific part that may be used in production.

Fourthly, many design libraries contain multiple outlines for the component bodies, representing anything from the actual outline, to a "keep-out" box that will be used to enforce component spacing design rules. As a consequence, when the product model is output to manufacturing and especially in an outsourced manufacturing environment, it is not always clear what the component body outlines actually represent and thus which DFA rule-values to apply.

Therefore, and as part of developing a portable DFA process, a dedicated library format was defined that provides a shared standard for the participants in the DFA workflow. The approach taken was to use the JEDEC classification system, but with extensions to give the granularity required to support the full range of DFA rules to be applied. The essential structure of the library is shown in Figure 6, showing how the linking of the component manufacturer and purchasable part number(s) to the component model comprises a classified name linked to the graphics of that particular model. Examples of component models are shown; the principle being that, whenever a different graphical model is required to fully represent the detail published in the component manufacturer's datasheet, a new unique classified name is generated.

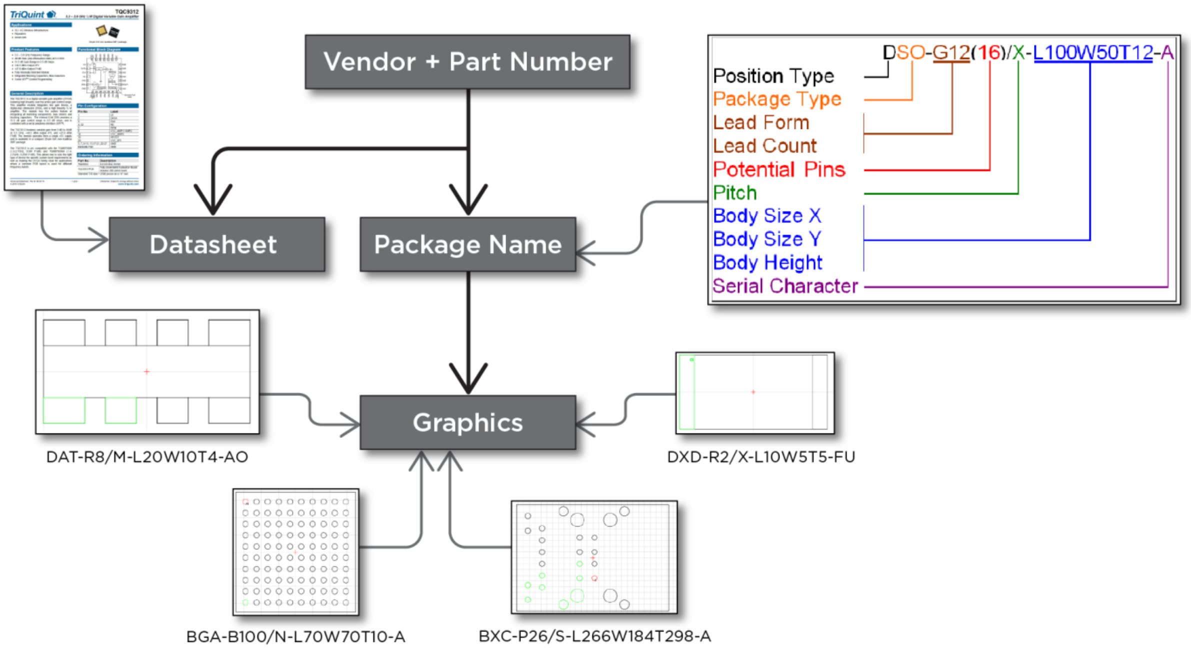


Figure 6: Cloud-based library structure linking purchasable parts to fixed-syntax graphical models.

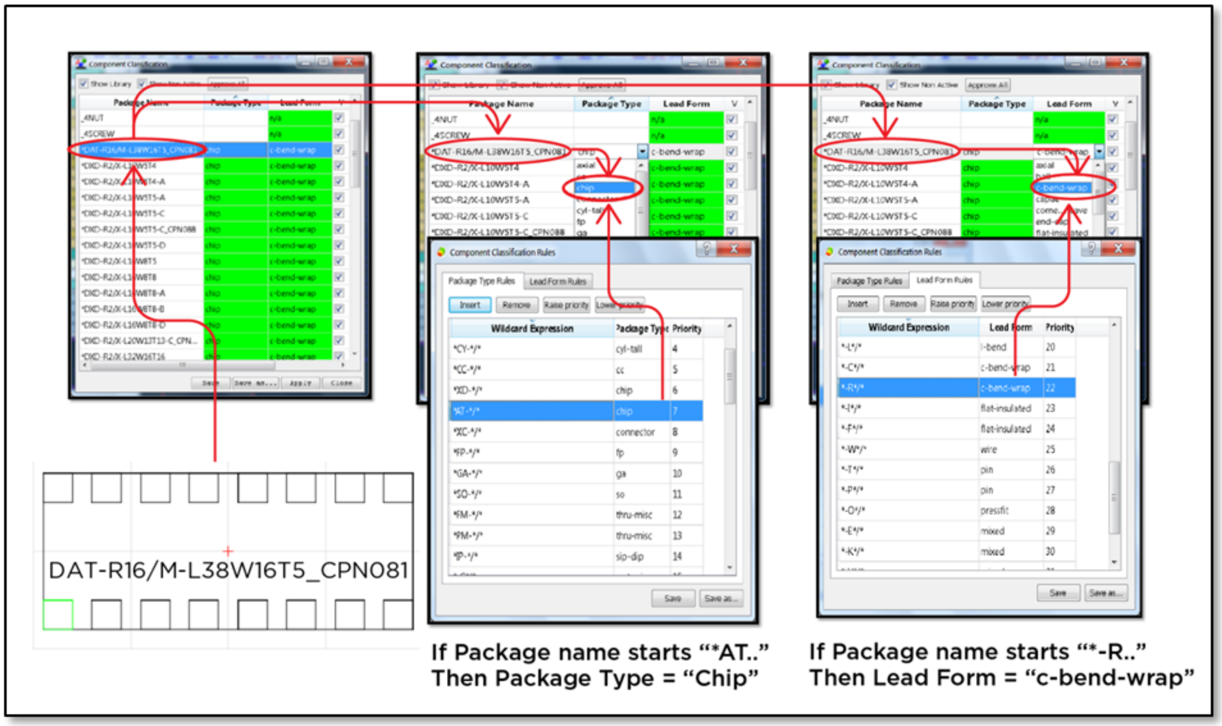
But it is not only the definition of the library structure and format that is essential to the solution, but also the availability of the content, as a service to the DFA engineers; the greater the extent to which the library can deliver the content for any particular PCB bill of materials (BOM), the greater the comprehensiveness of the DFA analysis that can be performed. After 15 years of building the content on behalf of DFA engineers around the world, there are now approximately 100,000 uniquely classified graphical models in the library mapped to upwards of 35 million purchasable part numbers. To date, there has not been a single instance of a PCB-mountable electronic component that cannot be modeled in the library for DFA purposes.

Second Requirement

The second major requirement to enable portability of the DFA process is to establish a standardized package- and pin-classification system in which the DFA analysis rules can be managed. The main challenge arises from the need for relevant spacing measurements between pairs of components of different classification. For example, the acceptable spacing between a small chip-resistor and an adjacent BGA will probably be different to the acceptable spacing between the BGA and a connector. Thus, the number of component-to-component rules can be proportional to the square of the number of different types of components in the library. Obviously, while it is necessary for the sake of DFA measurement accuracy to have available a number of unique component models on the order of 100,000 (as described in the previous section), to have 100,000 x 100,000 separate DFA rules to manage is obviously impracticable.

The approach we took was to consult people who are using DFA technology to determine the maximum granularity of component package types and lead form types needed to ensure that the DFA analysis measurements are appropriate to the combinations of components on the PCB. After many years of gathering feedback, we have 17 different package types and 23 different lead-form classifications, which result in a range of DFA rules measured in the hundreds, not the billions that would result from using the library-level classifications to define the distinction between DFA rules.

Figure 7 shows an example of a component model defined in the library as DAT-R16/M-L38W16T5_CPN081. This is the same syntax for unique definitions of the component models from the library definitions explained in the previous section. From this component model classification, the DFA software is able to automatically derive the package type as “chip” and the lead form as “c-bend-wrap”. The rules for defining these two type assignments are also shown in Figure 7.



Component Classification

☑ Show Library ☑ Show Non Active Approve All

Package Name	Package Type	Lead Form	V
_4NUT		n/a	☑
_4SCREW		n/a	☑
*DAT-R16/M-L38W16T5_CPN081	chip	c-bend-wrap	☑
*DXD-R2/X-L10W5T4	chip	c-bend-wrap	☑
*DXD-R2/X-L10W5T4-A	chip	c-bend-wrap	☑
*DXD-R2/X-L10W5T5-A	chip	c-bend-wrap	☑
*DXD-R2/X-L10W5T5-C	chip	c-bend-wrap	☑
*DXD-R2/X-L10W5T5-C_CPN088	chip	c-bend-wrap	☑
*DXD-R2/X-L10W5T5-D	chip	c-bend-wrap	☑
*DXD-R2/X-L10W8T5	chip	c-bend-wrap	☑
*DXD-R2/X-L10W8T8	chip	c-bend-wrap	☑
*DXD-R2/X-L10W8T8-A	chip	c-bend-wrap	☑
*DXD-R2/X-L16W8T8-B	chip	c-bend-wrap	☑
*DXD-R2/X-L16W8T8-D	chip	c-bend-wrap	☑
*DXD-R2/X-L20W13T13-C_CPN...	chip	c-bend-wrap	☑
*DXD-R2/X-L32W16T16	chip	c-bend-wrap	☑

DAT-R16/M-L38W16T5_CPN081

Component Classification Rules

Package Type Rules | Lead Form Rules

Wildcard Expression	Package Type	Priority
CY-/*	cyl-tall	4
CC-/*	cc	5
XD-/*	chip	6
AT-/*	chip	7
XC-/*	connector	8
FP-/*	fp	9
GA-/*	ga	10
SO-/*	so	11
FM-/*	thru-misc	12
PM-/*	thru-misc	13
P-/*	sip-dip	14

If Package name starts "*AT.."
Then Package Type = "Chip"

Component Classification Rules

Package Type Rules | Lead Form Rules

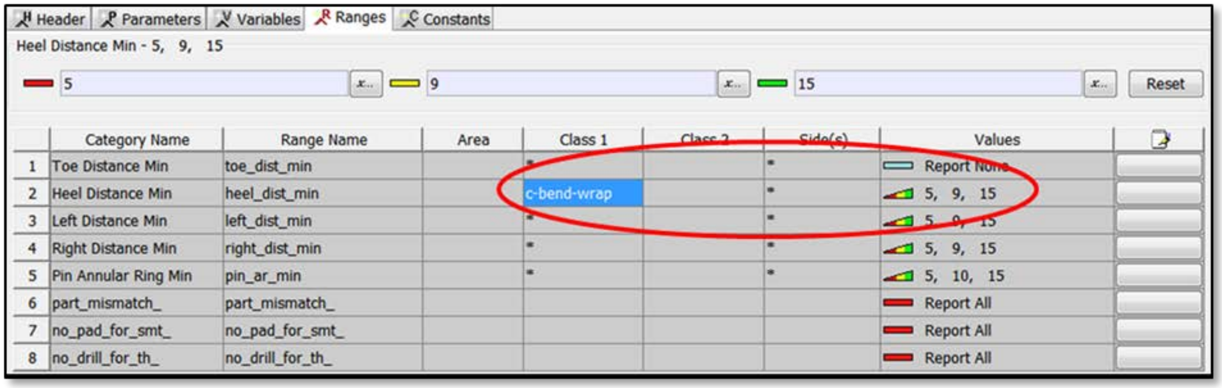
Wildcard Expression	Lead Form	Priority
-L/*	l-bend	20
-C/*	c-bend-wrap	21
-R/*	c-bend-wrap	22
-I/*	flat-insulated	23
-F/*	flat-insulated	24
-W/*	wire	25
-T/*	pin	26
-P/*	pin	27
-O/*	pressfit	28
-E/*	mixed	29
-K/*	mixed	30

If Package name starts "*-R.."
Then Lead Form = "c-bend-wrap"

Figure 7: Rules-based classification of package and lead form for DFA rules management.

The advantage of deriving the type assignments within the DFA software is that as the DFA requirements of the industry evolve, the method for deriving the type assignments, and the connection of those assignments to the rules themselves, can be released via software updates without disturbing the library content that is at the root of the process.

To illustrate the application of a DFA rule in the context of the type-assignments, Figure 8a shows a minimum heel-distance rule for components with lead forms of type "c-bend-wrap". The rule calls for a minimum spacing of 5 mils, with 9 mils being the target for best yield. Figure 8b then shows the result of applying this specific rule to the relevant components; in this case, the minimum heel distance is actually negative, thus calling for either an engineering change to the land pattern, of a change of components supplier on the master parts list, or maybe both.

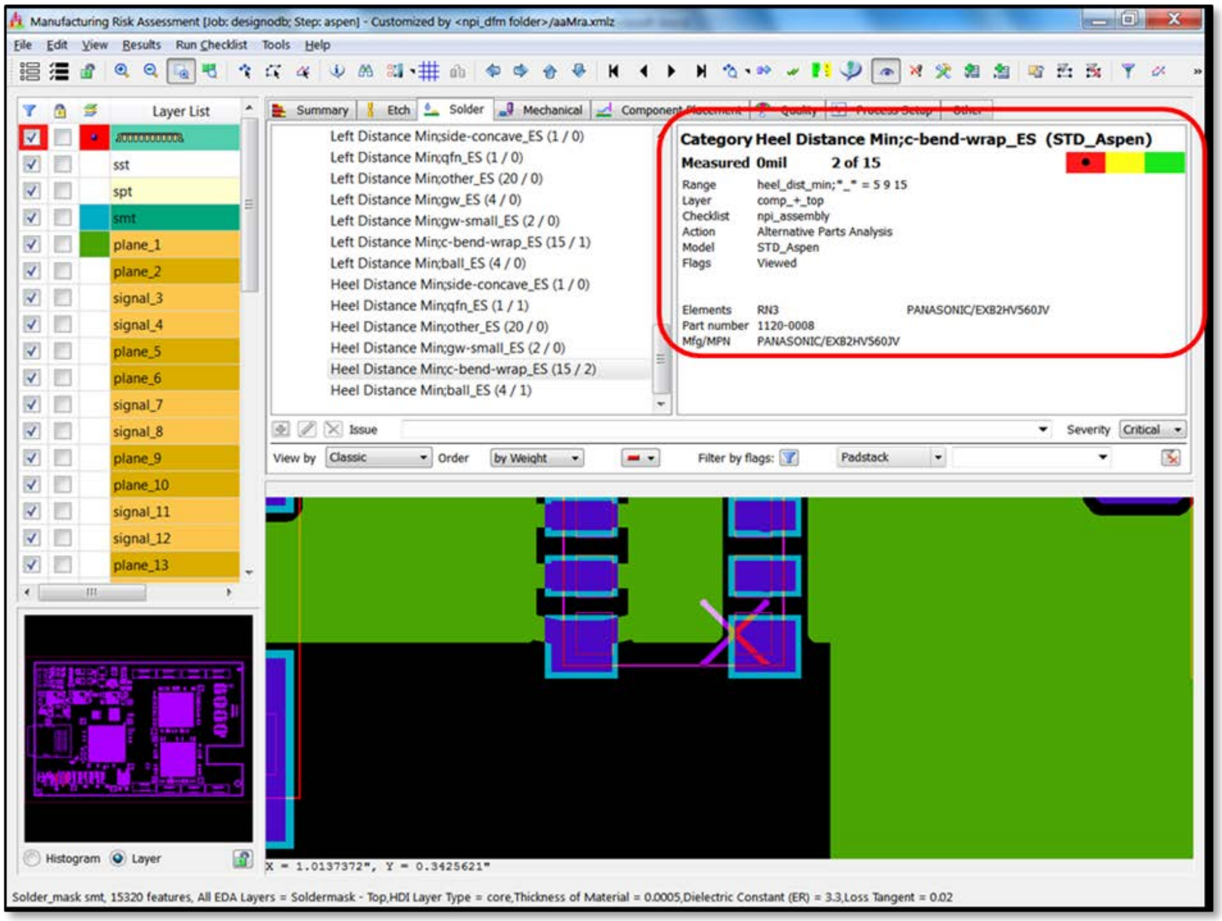


Heel Distance Min - 5, 9, 15

🟥 5 | 🟨 9 | 🟩 15

	Category Name	Range Name	Area	Class 1	Class 2	Side(s)	Values	
1	Toe Distance Min	toe_dist_min		*		*	Report None	
2	Heel Distance Min	heel_dist_min		c-bend-wrap		*	5, 9, 15	
3	Left Distance Min	left_dist_min		*		*	5, 9, 15	
4	Right Distance Min	right_dist_min		*		*	5, 9, 15	
5	Pin Annular Ring Min	pin_ar_min		*		*	5, 10, 15	
6	part_mismatch_	part_mismatch_					🟥 Report All	
7	no_pad_for_smt_	no_pad_for_smt_					🟥 Report All	
8	no_drill_for_th_	no_drill_for_th_					🟥 Report All	

Figure 8a: A DFA rule for minimum heel distance for a specific class of component.



Left Distance Min;side-concave_ES (1 / 0)
Left Distance Min;qfn_ES (1 / 0)
Left Distance Min;other_ES (20 / 0)
Left Distance Min;gw_ES (4 / 0)
Left Distance Min;gw-small_ES (2 / 0)
Left Distance Min;c-bend-wrap_ES (15 / 1)
Left Distance Min;ball_ES (4 / 0)
Heel Distance Min;side-concave_ES (1 / 0)
Heel Distance Min;qfn_ES (1 / 1)
Heel Distance Min;other_ES (20 / 0)
Heel Distance Min;gw-small_ES (2 / 0)
Heel Distance Min;c-bend-wrap_ES (15 / 2)
Heel Distance Min;ball_ES (4 / 1)

Category Heel Distance Min;c-bend-wrap_ES (STD_Aspen)
Measured 0mil 2 of 15

Range	heel_dist_min;*_* = 5 9 15	
Layer	comp_+_top	
Checklist	npi_assembly	
Action	Alternative Parts Analysis	
Model	STD_Aspen	
Flags	Viewed	
Elements	RN3	PANASONIC/EXB2HV560JV
Part number	1120-0008	
Mfg/MPN	PANASONIC/EXB2HV560JV	

Issue Severity Critical
View by Classic Order by Weight Filter by flags: Padstack

X = 1.0137372", Y = 0.3425621"

Solder_mask smt, 15320 features, All EDA Layers = Soldermask - Top,HDI Layer Type = core,Thickness of Material = 0.0005,Dielectric Constant (ER) = 3.3,Loss Tangent = 0.02

Figure 8b: Application of a minimum heel-distance rule to a PCB assembly model.

Third Requirement

The third element of the portable DFA solution is a documented language of rules that can be transferred between manufacturer and designer for application as early as possible in the design process. By exporting the DFA rules that are proven by the manufacturer to represent the constraints of the manufacturing processes, they can then be transmitted to the design organization to run the complete DFA analysis process while the design is still taking shape and the cost of finding and fixing the manufacturability problems is so much lower than if left until later in the NPI cycle.

In summary, Figure 9 illustrates how the portable DFA solution comprises the following multiple aspects that combine to make a working solution:

- A library of component models mapped to commercially purchasable part numbers. The library exists outside the internal networks of individual organizations, thus supporting the outsourced design-through-manufacturing flows of today.
- Availability of content in the library to describe the components listed in the bills-of-materials of the participating design and manufacturing organizations. Part-number coverage must run to the tens of millions, with rapid service to create missing content on demand to support scalable implementation by designers and manufacturers worldwide.
- DFA analysis software tools that can be used both in the context of design and manufacturing environments, with common functionality for the derivation of package and lead-form assignations, and a common DFA rules language.

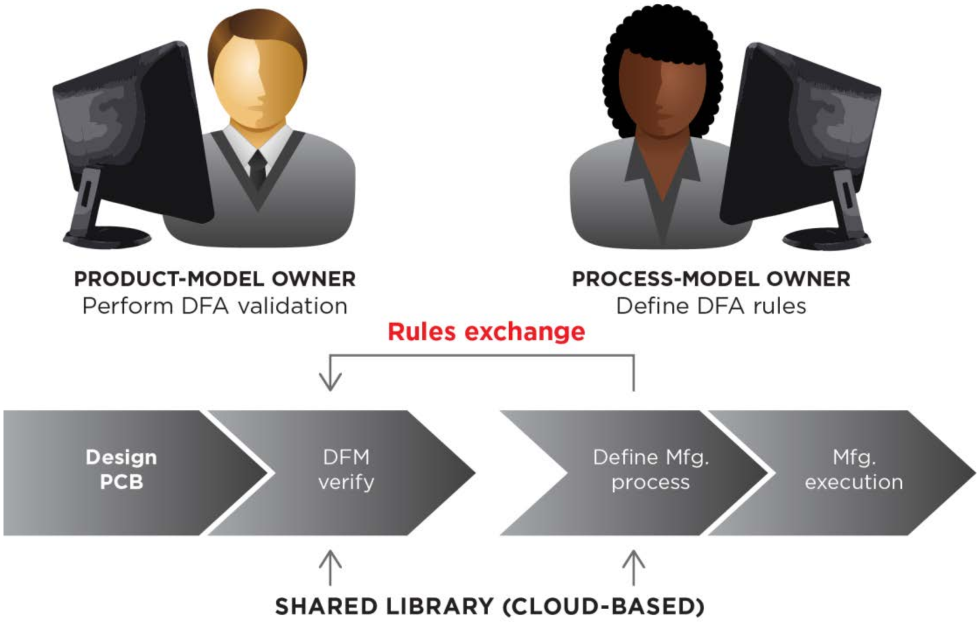


Figure 9: Shared library content, classifications, and rules enable portable DFA analysis.

Portability of Production between PCB Assembly Lines

In the context of PCB assembly operations, by portability, we mean the ability to easily move the assembly of a specific PCB design from one assembly line to another or from one factory to another or rapid switching on a specific assembly line between the production of different products. The business drivers behind this are:

- Reduction in working capital resulting from lean production techniques that call for small lots of PCB assemblies to be produced according to downstream inventory demand signals.
- Supply-chain discontinuities making it impossible to continue production of a certain product, requiring fast switching to production of another product.
- Supply-chain flexibility for the product-owner to switch rapidly from one manufacturing service provider to another.
- Maintaining high asset utilization of the assembly lines themselves. Typically, the machinery that comprises the assembly line ties up the majority of the fixed-asset capital of the manufacturer so, just as airlines need to keep their planes in the air to earn money, the assembly manufacturers need to maximize the time when the assembly lines are assembly products.

Assuming that component supply and machine availability are not limiting factors, the most important capability for addressing the above-mentioned business drivers is fast machine programming with all the data necessary to begin production of a new product. The primary burden here is the generation and management of the machine-level component libraries that determine how the different machines (placement, inspection, text) will treat each component on the PCB.

As shown by Figure10, each different machine has its own library, which must contain definitions of the parts it will handle. A single assembly line may have five to six different machines all with their own libraries; across a large factory, the number of separately maintained libraries can run to the hundreds. Just consider the time involved, per new part, per machine. An industry average is to spend 15 minutes, per new part, per machine type, preparing and testing out the part data. If there are 20 new parts in a PCB that is new to that assembly line, that is five machines in the line. It will take 1,500 minutes (more than two hours) of machine down-time to prepare the machine libraries for that particular product. In an environment of lean manufacturing with small lot sizes, such set-up overheads can mean that the manufacturer spends more time with his assembly lines down than up and running.

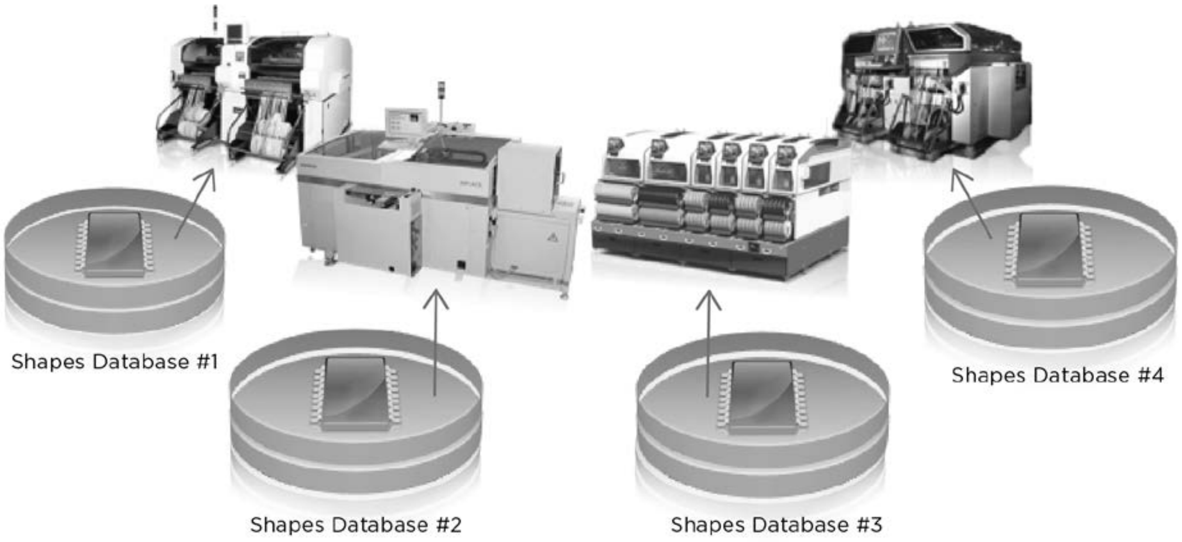
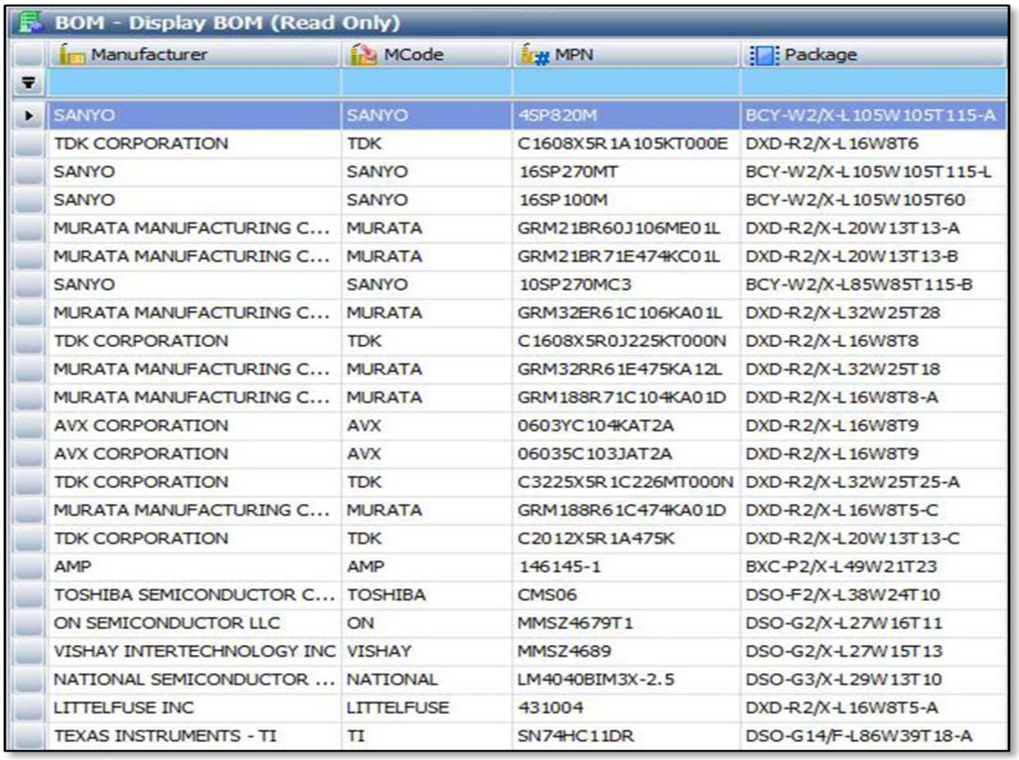


Figure 10: There are as many machine-library standards as there are types of machines in the world.

When we examined the nature of the parts data in the machine libraries we discovered that, with the exception of data that cannot be found in a component's datasheet such as color changes and markings that vary with lot code, the machine library content can all be derived from a standardized 2.5D model through the use of machine-dedicated rules. The flow for the solution, together with the requirements at each stage, is as follows.

First Requirement

The flow requires a source library for the component models that links back to the commercially purchasable part-numbers used in the supply chain. This enables transferability of a PCB product model between organizations and the use of a common component-model standard for deriving the machine-level library content for any assembly line or factory. Figure 11 shows links between component vendor name plus part number and the models in the same library as was described in the above discussion of portable DFA.



BOM - Display BOM (Read Only)

Manufacturer	MCode	MPN	Package
SANYO	SANYO	4SP820M	BCY-W2/X-L105W105T115-A
TDK CORPORATION	TDK	C1608X5R1A105KT000E	DXD-R2/X-L16W8T6
SANYO	SANYO	16SP270MT	BCY-W2/X-L105W105T115-L
SANYO	SANYO	16SP100M	BCY-W2/X-L105W105T60
MURATA MANUFACTURING C...	MURATA	GRM21BR60J106ME01L	DXD-R2/X-L20W13T13-A
MURATA MANUFACTURING C...	MURATA	GRM21BR71E474KC01L	DXD-R2/X-L20W13T13-B
SANYO	SANYO	10SP270MC3	BCY-W2/X-L85W85T115-B
MURATA MANUFACTURING C...	MURATA	GRM32ER61C106KA01L	DXD-R2/X-L32W25T28
TDK CORPORATION	TDK	C1608X5R0J225KT000N	DXD-R2/X-L16W8T8
MURATA MANUFACTURING C...	MURATA	GRM32RR61E475KA12L	DXD-R2/X-L32W25T18
MURATA MANUFACTURING C...	MURATA	GRM188R71C104KA01D	DXD-R2/X-L16W8T8-A
AVX CORPORATION	AVX	0603YC104KAT2A	DXD-R2/X-L16W8T9
AVX CORPORATION	AVX	06035C103JAT2A	DXD-R2/X-L16W8T9
TDK CORPORATION	TDK	C3225X5R1C226MT000N	DXD-R2/X-L32W25T25-A
MURATA MANUFACTURING C...	MURATA	GRM188R61C474KA01D	DXD-R2/X-L16W8T5-C
TDK CORPORATION	TDK	C2012X5R1A475K	DXD-R2/X-L20W13T13-C
AMP	AMP	146145-1	BXC-P2/X-L49W21T23
TOSHIBA SEMICONDUCTOR C...	TOSHIBA	CMS06	DSO-F2/X-L38W24T10
ON SEMICONDUCTOR LLC	ON	MMSZ4679T1	DSO-G2/X-L27W16T11
VISHAY INTERTECHNOLOGY INC	VISHAY	MMSZ4689	DSO-G2/X-L27W15T13
NATIONAL SEMICONDUCTOR ...	NATIONAL	LM4040BIM3X-2.5	DSO-G3/X-L29W13T10
LITTELFUSE INC	LITTELFUSE	431004	DXD-R2/X-L16W8T5-A
TEXAS INSTRUMENTS - TI	TI	SN74HC11DR	DSO-G14/F-L86W39T18-A

Figure 11: Mapping purchasable component part numbers in the BOM to shared library content.

The result is that, in the context of any assembly line or factory, the model of the product to be assembled will be identical. Figure 12 shows an example of the PCB product model, after identification of the parts and integration of their models from the cloud-based library. You see the exact outlines of the component bodies, their physical pin contacts on the PCB, of course also linked to the data that is embedded in the component-model name itself.

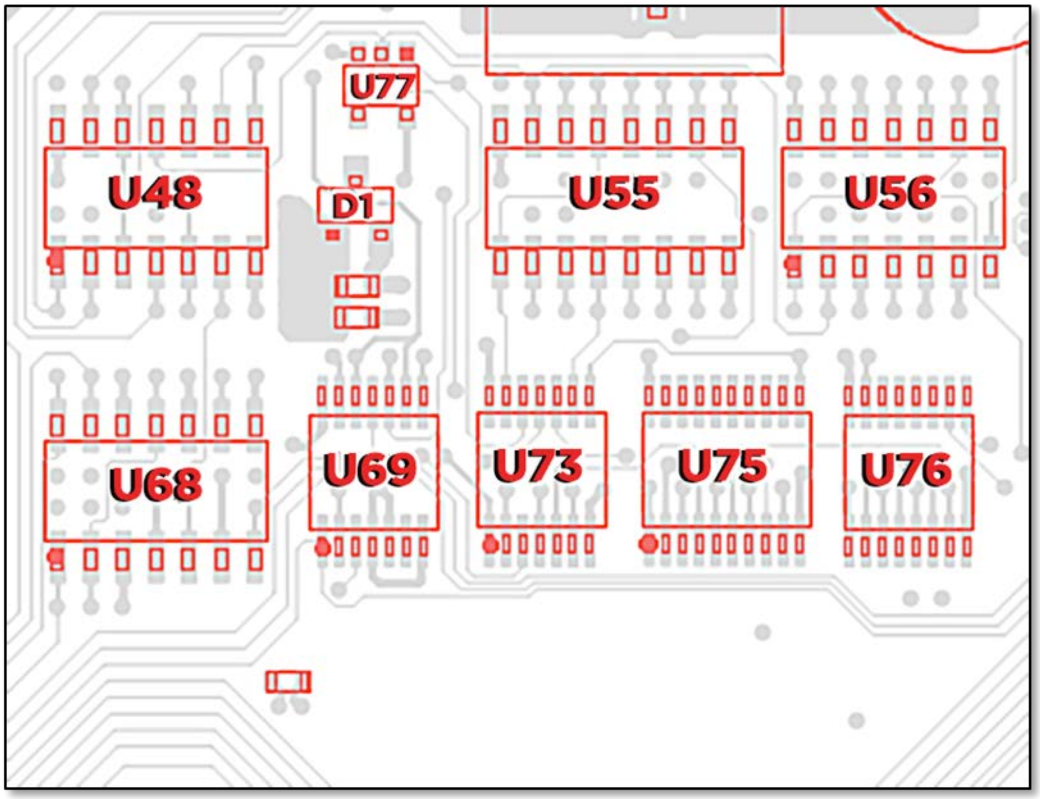
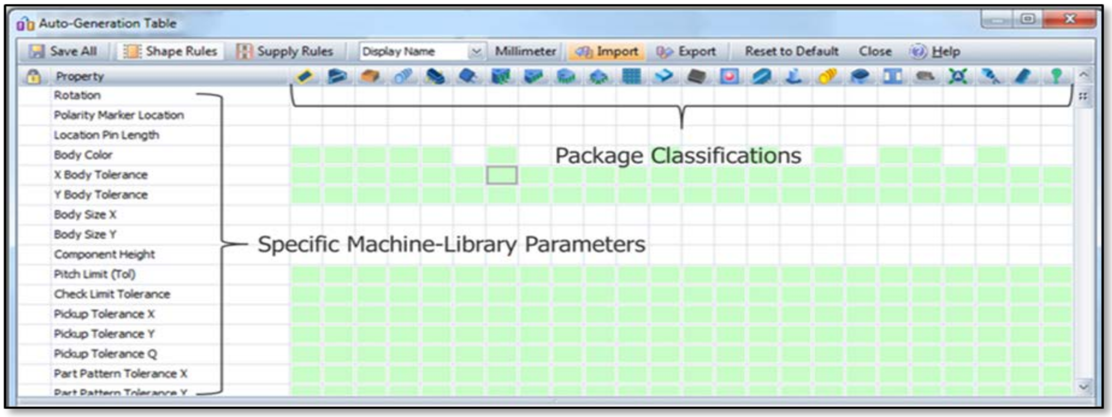


Figure 12: Component body and pin-contact models, integrated into the PCB product model.

Second Requirement

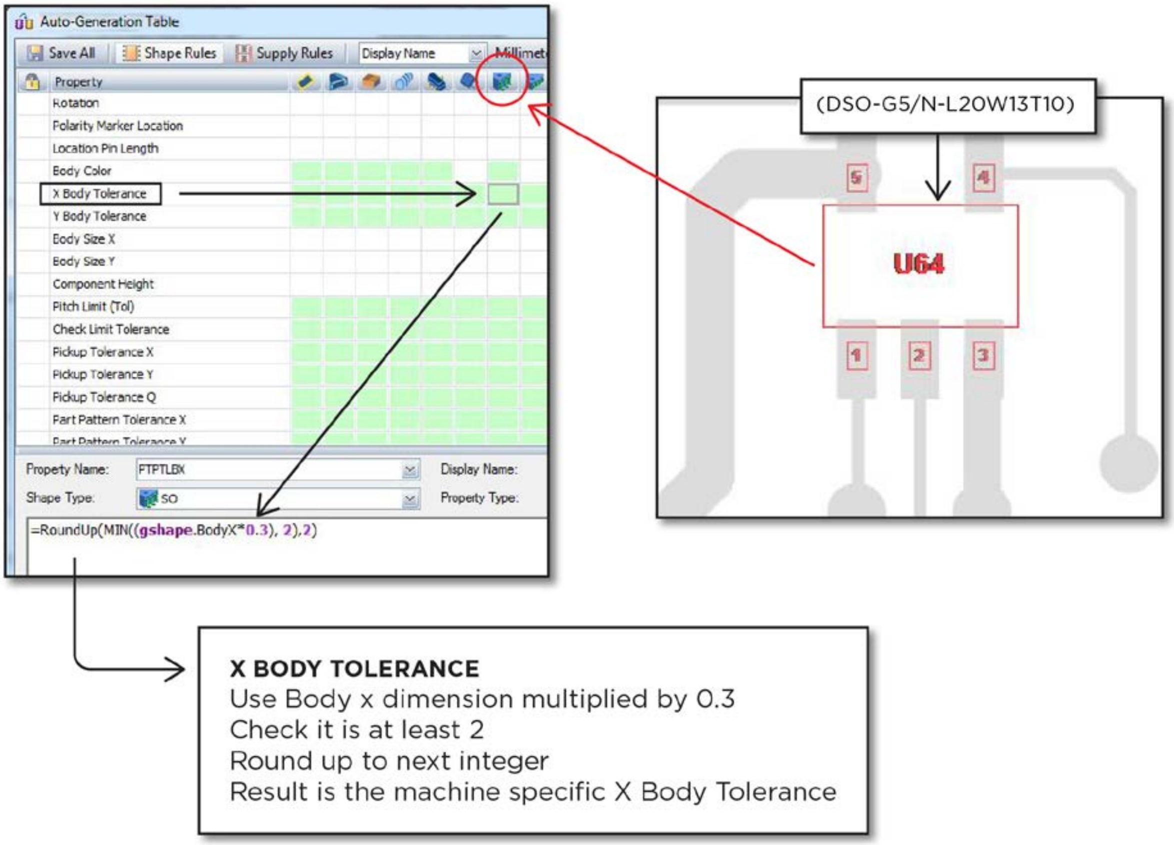
A classification system is required that can relate to any specific machine requirements to take the step from the general model of the part shown in the previous section to a machine-specific model of the part. After reviewing the libraries of the mainstream pick-and-place, AOI, AXI, and structural test machine vendors, we built a classification system as illustrated in Figure 13. From left to right, 24 component package classifications are shown for which machine-specific content can be derived. The rows in the table define the specific library content required by a particular widely used pick-and-place machine; the green cells are all instances where specific content is required for that machine to handle components of a particular classification. Thus, the purpose of the individual rows will vary according to the requirements of any particular machine, as will the definition of which classifications need each type of content (marked in green).



Property
Rotation
Polarity Marker Location
Location Pin Length
Body Color
X Body Tolerance
Y Body Tolerance
Body Size X
Body Size Y
Component Height
Pitch Limit (Tol)
Check Limit Tolerance
Pickup Tolerance X
Pickup Tolerance Y
Pickup Tolerance Q
Part Pattern Tolerance X
Part Pattern Tolerance Y

Figure 13: Matrix linking machine-library component classes to machine-library content rules.

Each green square in the matrix can have its own unique derivation rule(s) to be applied when generating the content for that specific machine. To illustrate, we can take the example of a simple five-pin gullwing component. The component is automatically classified as “SO”, which requires an X body tolerance for the specific machine we are preparing the library for. The rule for calculating the X body tolerance for this particular machine is shown in Figure 14, with a plain English version written underneath.



Property Name: FTPTLBX

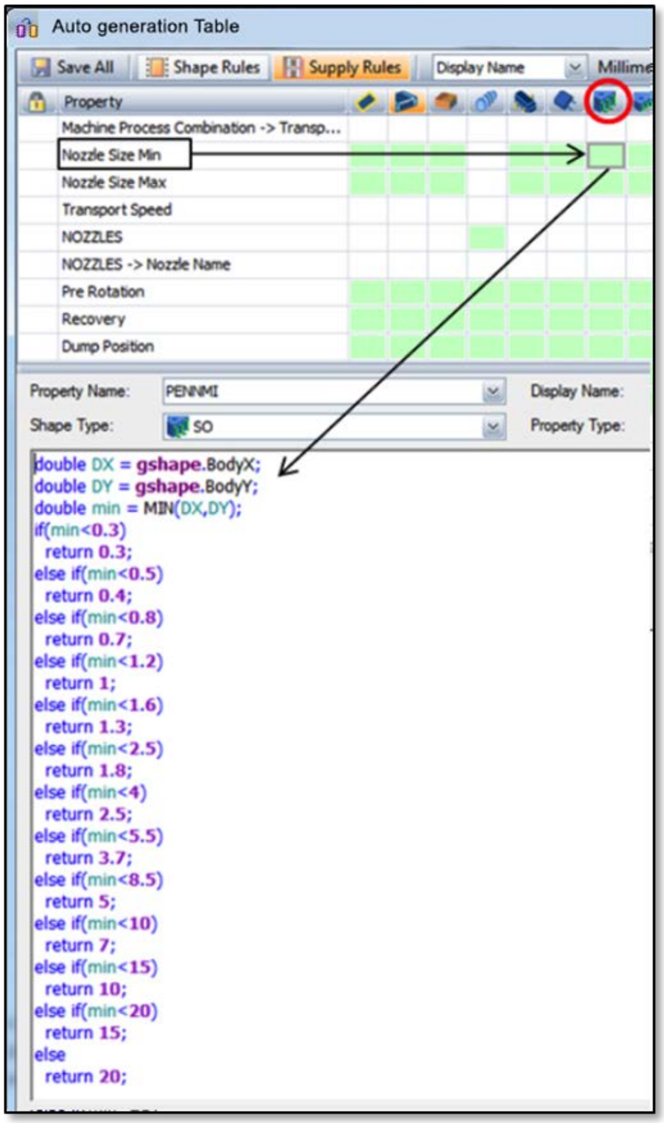
Shape Type: SO

```
=RoundUp(MIN((gshape.BodyX*0.3), 2),2)
```

X BODY TOLERANCE
Use Body x dimension multiplied by 0.3
Check it is at least 2
Round up to next integer
Result is the machine specific X Body Tolerance

Figure 14: Automatic derivation of machine-specific library content (X-body tolerance).

An example of a more complicated rule is shown in Figure 15 for the same component. In this example, the rule relates to the nozzle definition for the component. It illustrates the logic for selecting minimum nozzle size based on component body dimensions, for this particular machine.



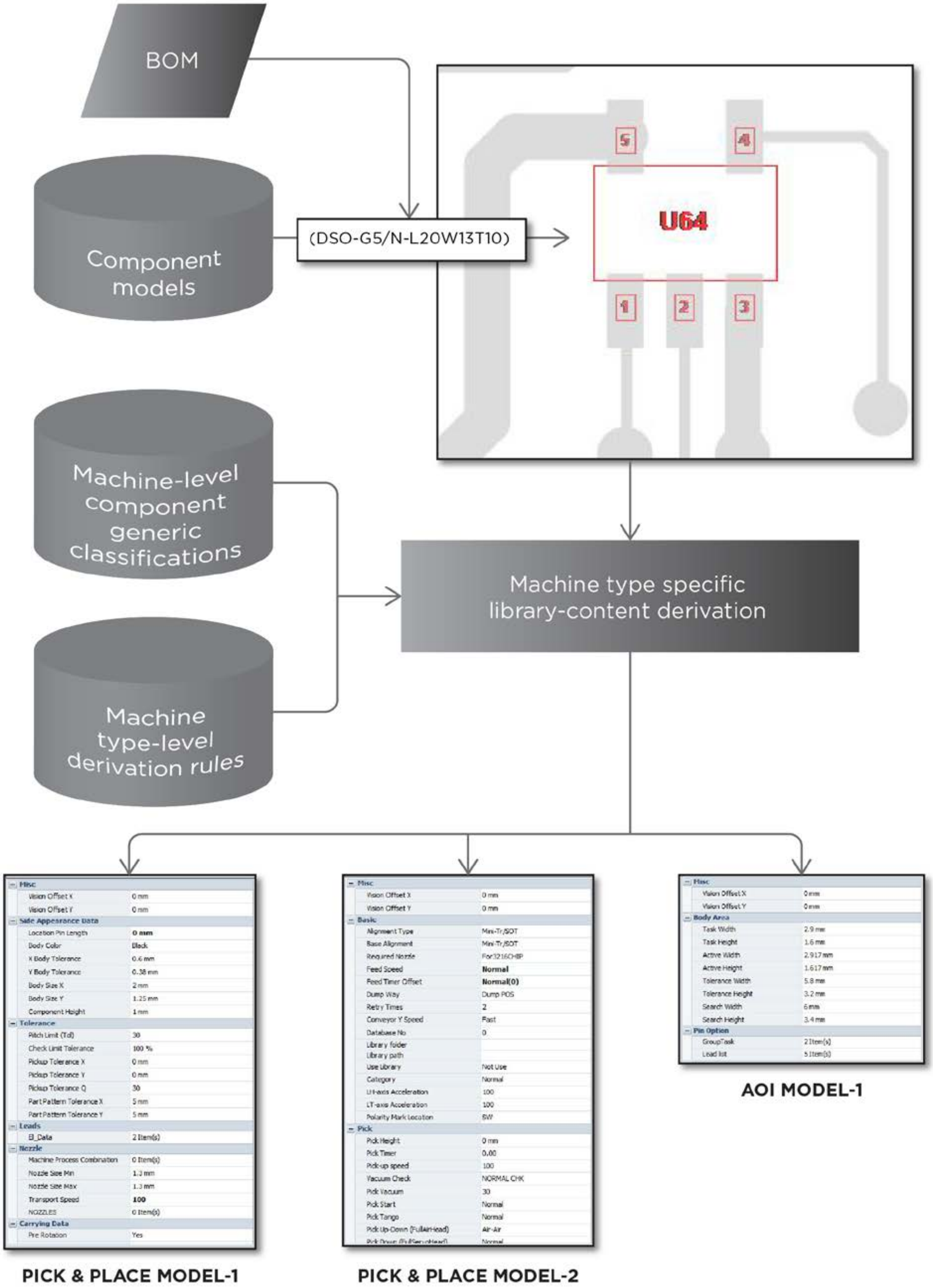
Machine Process Combination -> Transp...
Nozzle Size Min
Nozzle Size Max
Transport Speed
NOZZLES
NOZZLES -> Nozzle Name
Pre Rotation
Recovery
Dump Position

Property Name: PENNMI
Shape Type: SO
Display Name:
Property Type:

```
double DX = gshape.BodyX;
double DY = gshape.BodyY;
double min = MIN(DX,DY);
if(min<0.3)
  return 0.3;
else if(min<0.5)
  return 0.4;
else if(min<0.8)
  return 0.7;
else if(min<1.2)
  return 1;
else if(min<1.6)
  return 1.3;
else if(min<2.5)
  return 1.8;
else if(min<4)
  return 2.5;
else if(min<5.5)
  return 3.7;
else if(min<8.5)
  return 5;
else if(min<10)
  return 7;
else if(min<15)
  return 10;
else if(min<20)
  return 15;
else
  return 20;
```

Figure 15: Automatic derivation of machine-specific library content (nozzle diameter).

Thus, by a process of creating and proving the rules that relate to the library requirements of the models of pick-and-place, AOI, AXI, test machine in use across the industry, and all those who use the machines worldwide can expect right-first-time set-up of their machine libraries without having to create and fine-tune the data on the machine itself. By a combination of a single globally accessible source-model for the components, plus the classification system dedicated to the needs of machine-level libraries, and a library of rules at the machine-type level, a machine-library solution is created that can be applied at a level that runs above the individual machines, lines, and factories. Figure 16 shows the full flow of the solution, starting with BOM and model of the PCB assembly, through to the run-ready libraries at the individual machines.


BOM
Component models
(DSO-G5/N-L20W13T10)
5
4
U64
1
2
3
Machine-level component generic classifications
Machine type-level derivation rules
Machine type specific library-content derivation
PICK & PLACE MODEL-1
PICK & PLACE MODEL-2
AOI MODEL-1

Misc	
Vision Offset X	0 mm
Vision Offset Y	0 mm
Side Appearance Data	
Location Pin Length	**0 mm**
Body Color	Black
X Body Tolerance	0.6 mm
Y Body Tolerance	0.38 mm
Body Size X	2 mm
Body Size Y	1.25 mm
Component Height	1 mm
Tolerance	
Pitch Limit (Tol)	30
Check Limit Tolerance	100 %
Pickup Tolerance X	0 mm
Pickup Tolerance Y	0 mm
Pickup Tolerance Q	30
Part Pattern Tolerance X	5 mm
Part Pattern Tolerance Y	5 mm
Leads	
El_Data	2 Item(s)
Nozzle	
Machine Process Combination	0 Item(s)
Nozzle Size Min	1.3 mm
Nozzle Size Max	1.3 mm
Transport Speed	**100**
NOZZLES	0 Item(s)
Carrying Data	
Pre Rotation	Yes

Misc	
Vision Offset X	0 mm
Vision Offset Y	0 mm
Basic	
Alignment Type	Mini-Tr./SOT
Base Alignment	Mini-Tr./SOT
Required Nozzle	For3216CHIP
Feed Speed	**Normal**
Feed Timer Offset	**Normal(0)**
Dump Way	Dump POS
Retry Times	2
Conveyor Y Speed	Fast
Database No	0
Library folder	
Library path	
Use Library	Not Use
Category	Normal
UI-axis Acceleration	100
LT-axis Acceleration	100
Polarity Mark Location	SW
Pick	
Pick Height	0 mm
Pick Timer	0.00
Pick-up speed	100
Vacuum Check	NORMAL CHK
Pick Vacuum	30
Pick Start	Normal
Pick Tango	Normal
Pick Up-Down (FullAirHead)	Air-Air
Pick Down (FullServoHead)	Normal

Misc	
Vision Offset X	0 mm
Vision Offset Y	0 mm
Body Area	
Task Width	2.9 mm
Task Height	1.6 mm
Active Width	2.917 mm
Active Height	1.617 mm
Tolerance Width	5.8 mm
Tolerance Height	3.2 mm
Search Width	6 mm
Search Height	3.4 mm
Pin Option	
GroupTask	2 Item(s)
Lead list	5 Item(s)

Figure 16: Automatic library content-generation from one source, for multiple machine types.

In effect, a unified on-demand library content service for any SMT assembly, inspection, and test line, worldwide. Production of a specific PCB assembly can be switched between lines of any machine combination within a matter of minutes, bringing high flexibility in asset utilization and the opportunity to reduce production lot-sizes and thus levels of working capital. It opens the way for the full application of lean manufacturing in the supply-chain sense.

Summary

This paper describes a technological implementation of component libraries, classification systems, and rules that support DFA and assembly-line setup portability. The development has taken time because of a number of factors related to investment, time to gather and verify industry requirements, and the time required to establish library content of sufficient critical mass to meet the needs of the industry in general (tens of millions of parts). To be a working solution, multiple pieces of a puzzle had to be developed in parallel, including:

1. A globally available library that meets the requirements for DFA analysis and assembly line machines, loaded with content to match the many millions of parts in use by the design and manufacturing organizations.
2. A component classification system that meets the needs of DFA analysis.
3. A set of rules for DFA analysis, matched to the classification system, the values for which can be maintained by process engineers.
4. A component classification system that meets the needs of PCB assembly-line machine-library generation.
5. A set of rules for machine-level library generation that matches the classification system, which can be extended as new machines and component types emerge.
6. The software infrastructure and tools to realize the solution in the hands of PCB designers and manufacturers in thousands of locations worldwide, together with its on-going maintenance and upgrading according to developing industry processes and requirements.

The forward roadmap is to continue the development of all the aspects described above, in parallel and according to industry requirements, and also to support additional PCB-related engineering processes that can take advantage of the same source library content so as to further reduce the per-task cost.

Streamlining PCB Assembly and Test NPI With Shared Component Libraries

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Mentor Graphics, Valor Division
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Contents

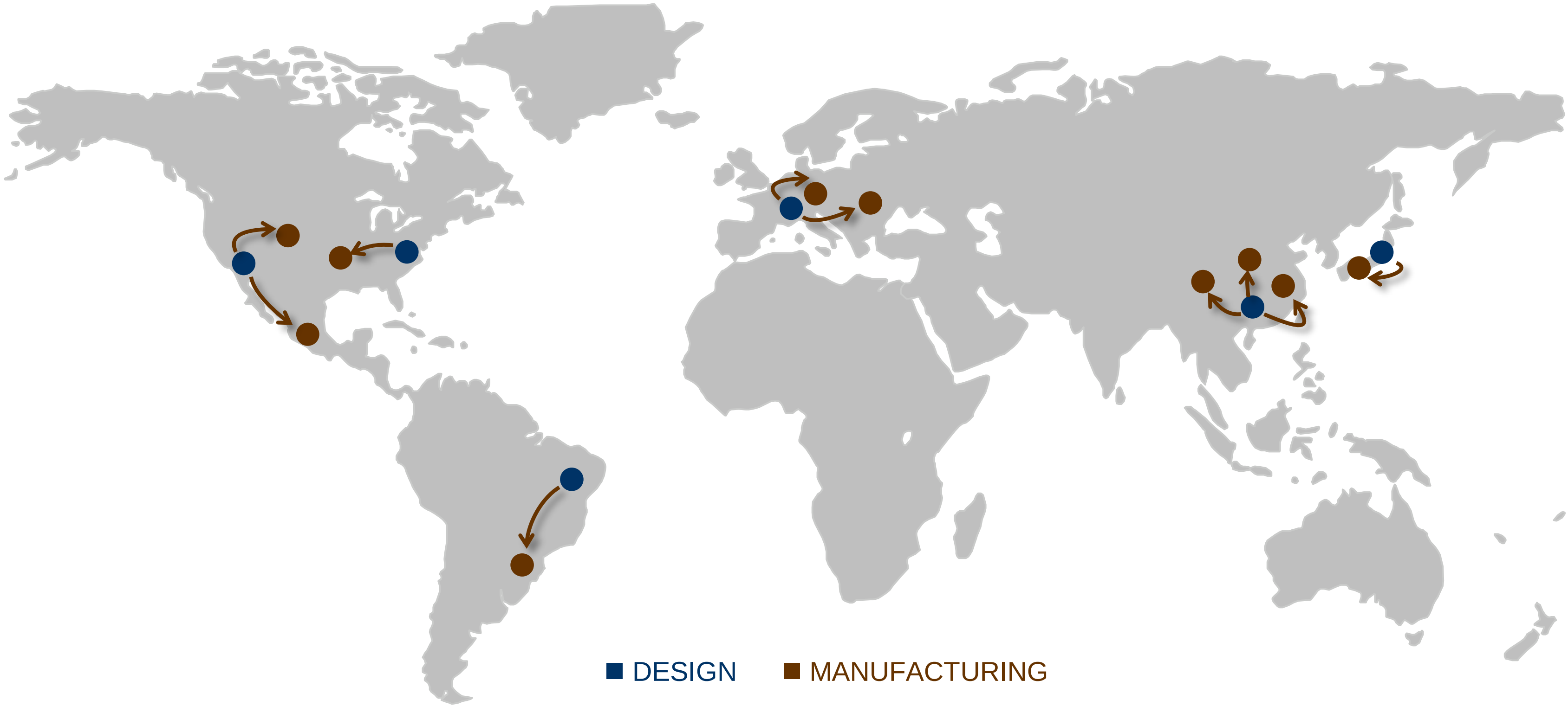
- Outsourcing, effect on libraries
- Focus on portability of two processes

  1. The portability problem:- DFA
     - DFA solution
  2. The portability problem:- Assembly-line libraries
     - The assembly-line libraries solution

- Summary

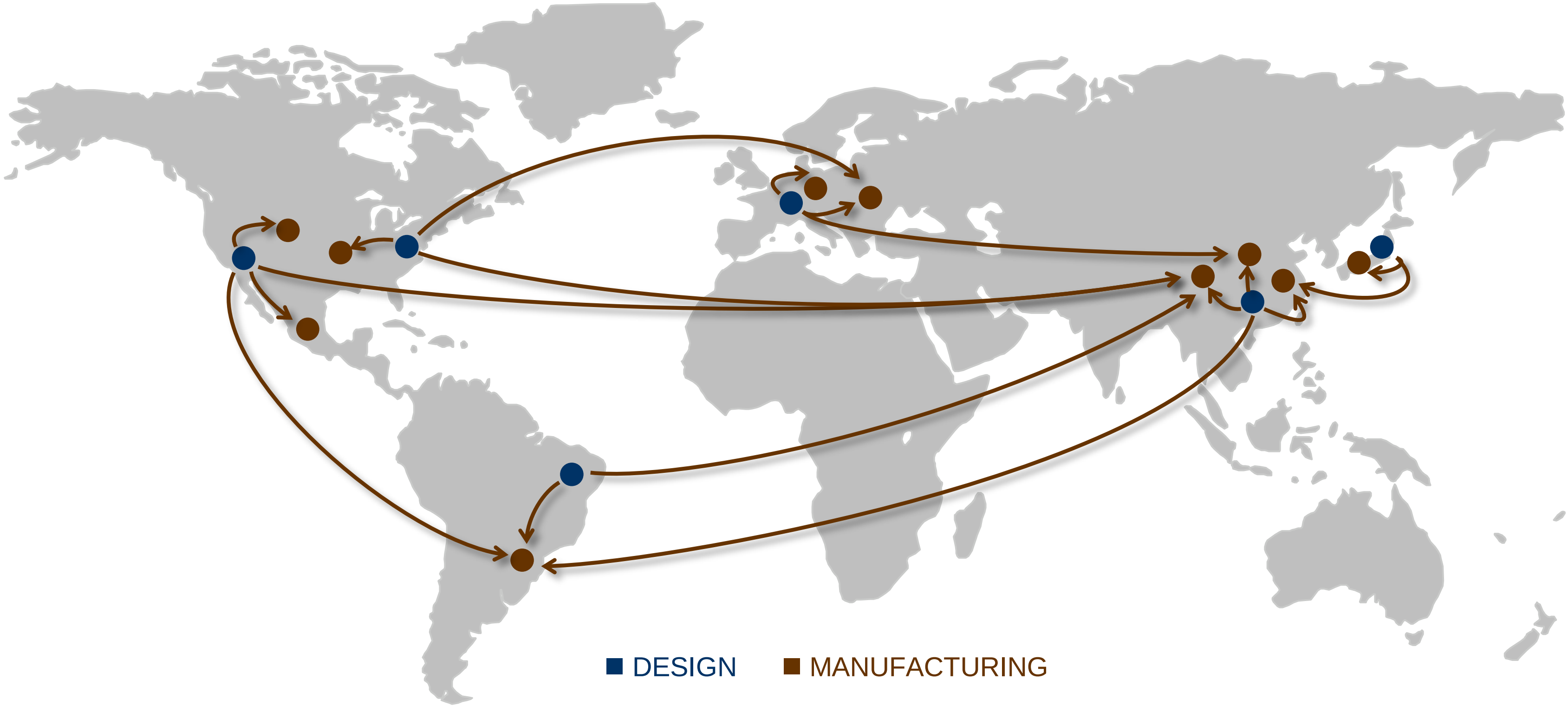
Traditional (localized) manufacturing

One to One or a Few to a Few
Company-specific standards for engineering processes



Modern manufacturing: Globalized

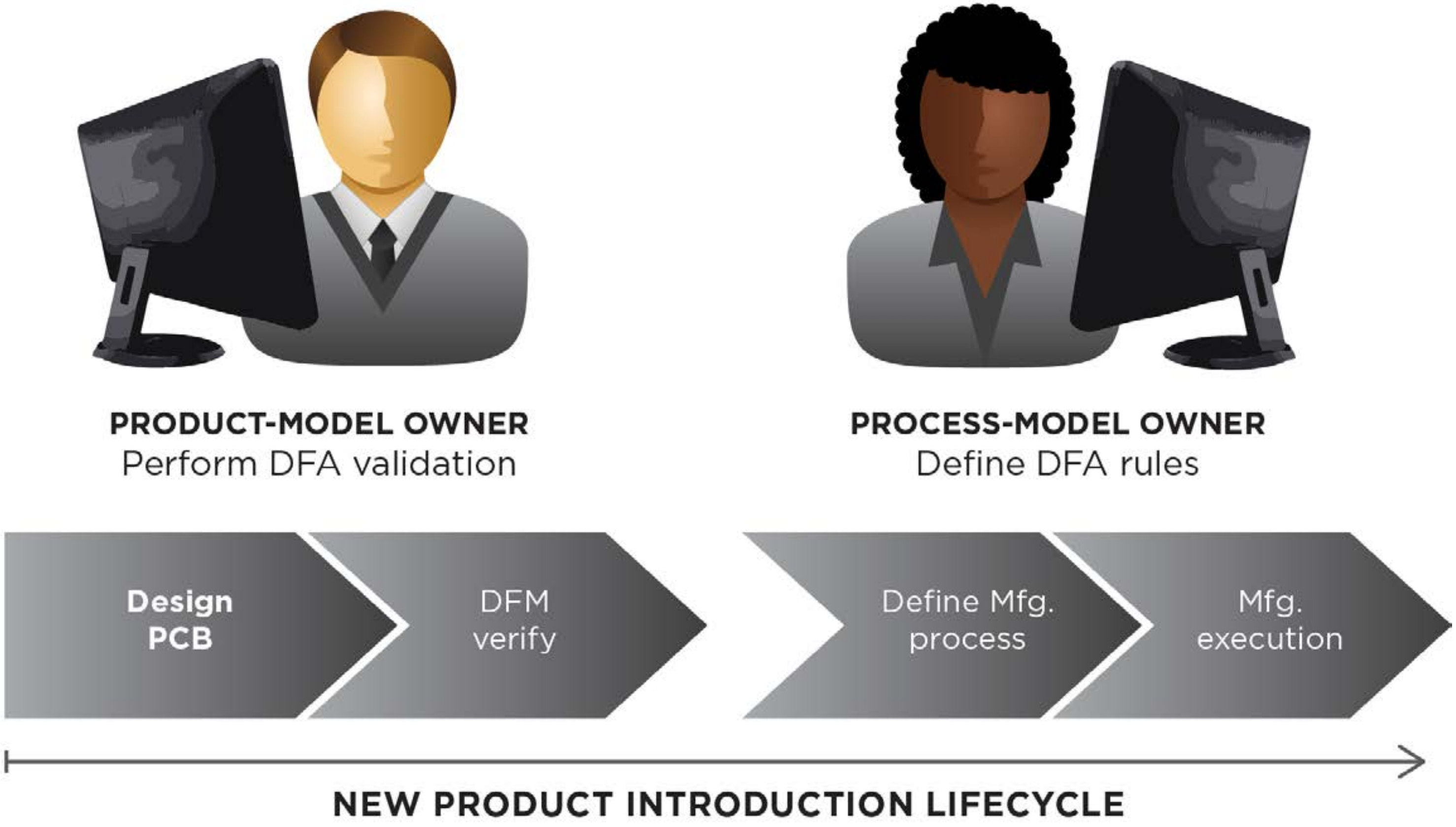
Many-to-Many relationship between designers and manufacturers
Consequence:- Engineering processes conform to the lowest common denominator

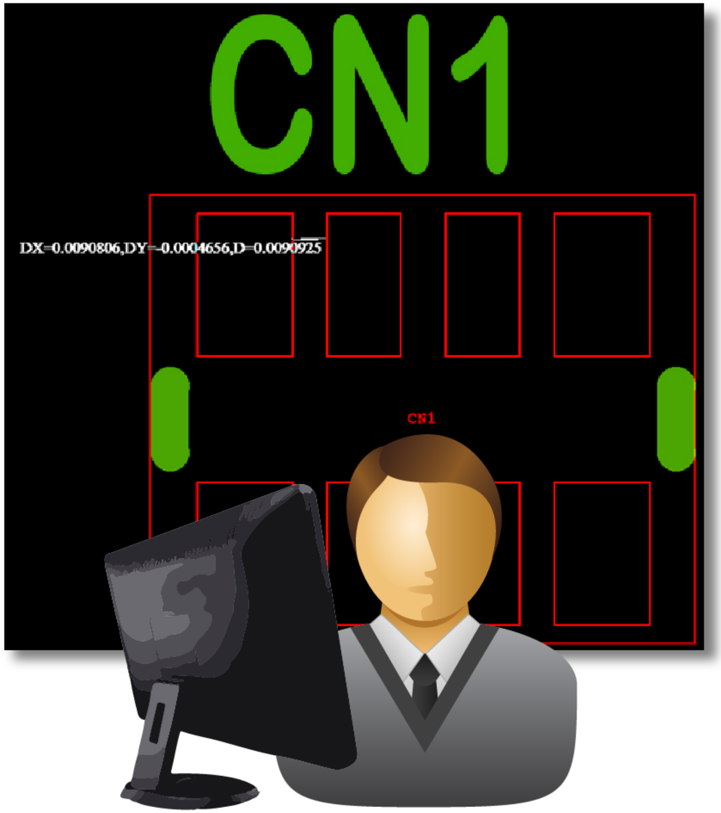


Focus: Libraries for DFA and the assembly & test process

The DFA portability problem

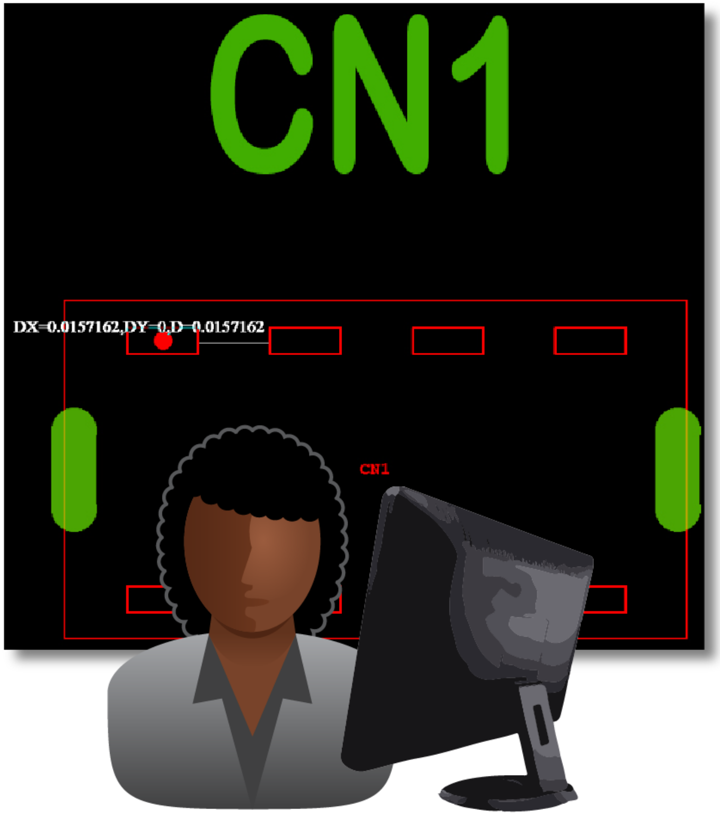
Ideal "lean" scenario:





PRODUCT-MODEL OWNER
Perform DFA validation

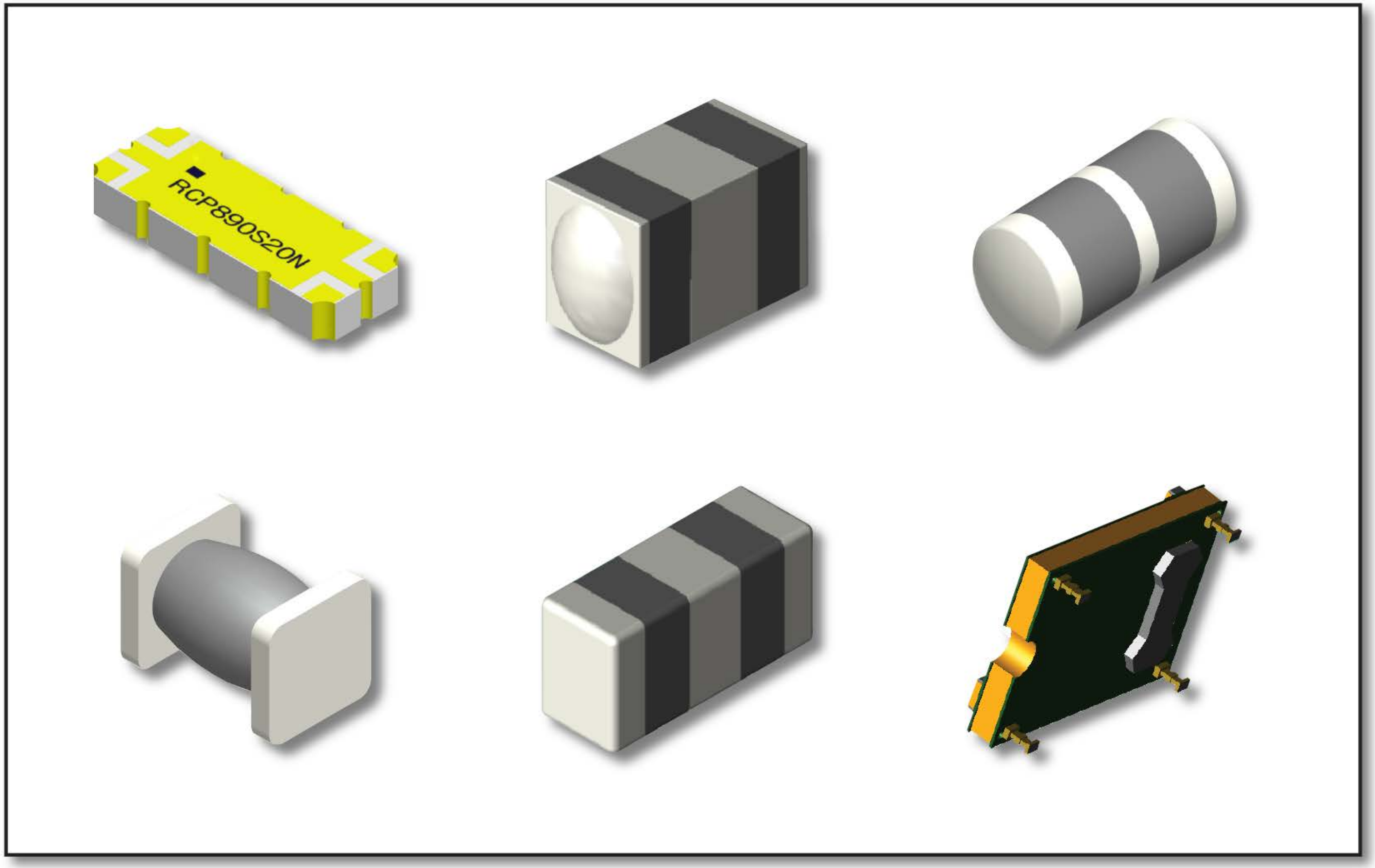
"Pin-spacing is 9 mils"



PROCESS-MODEL OWNER
Define DFA rules

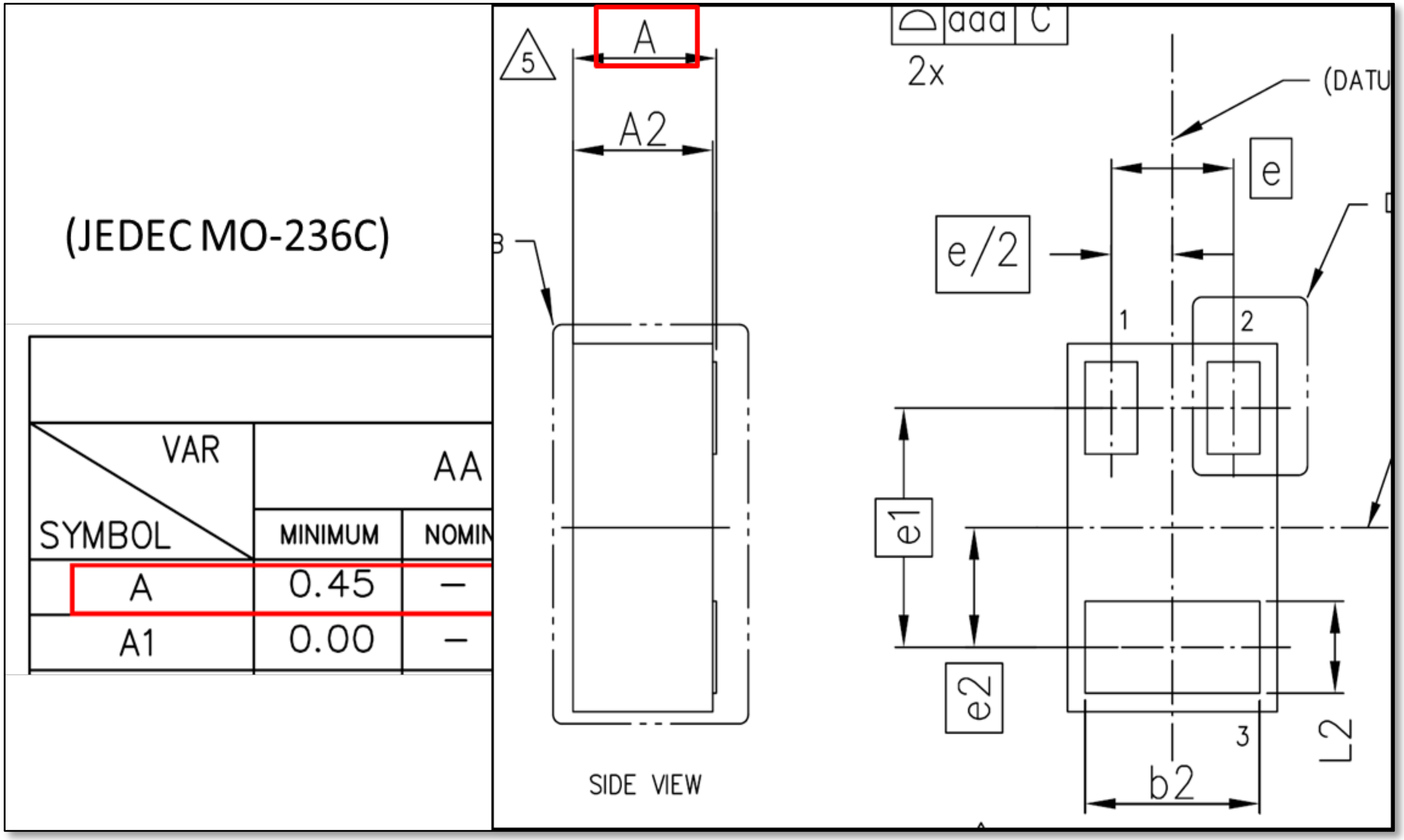
"Pin-spacing is 15 mils"

SAME COMPONENT - DIFFERENT REPRESENTATION



A selection of component
package types not covered
by JEDEC

Commercial parts conforming to JEDEC

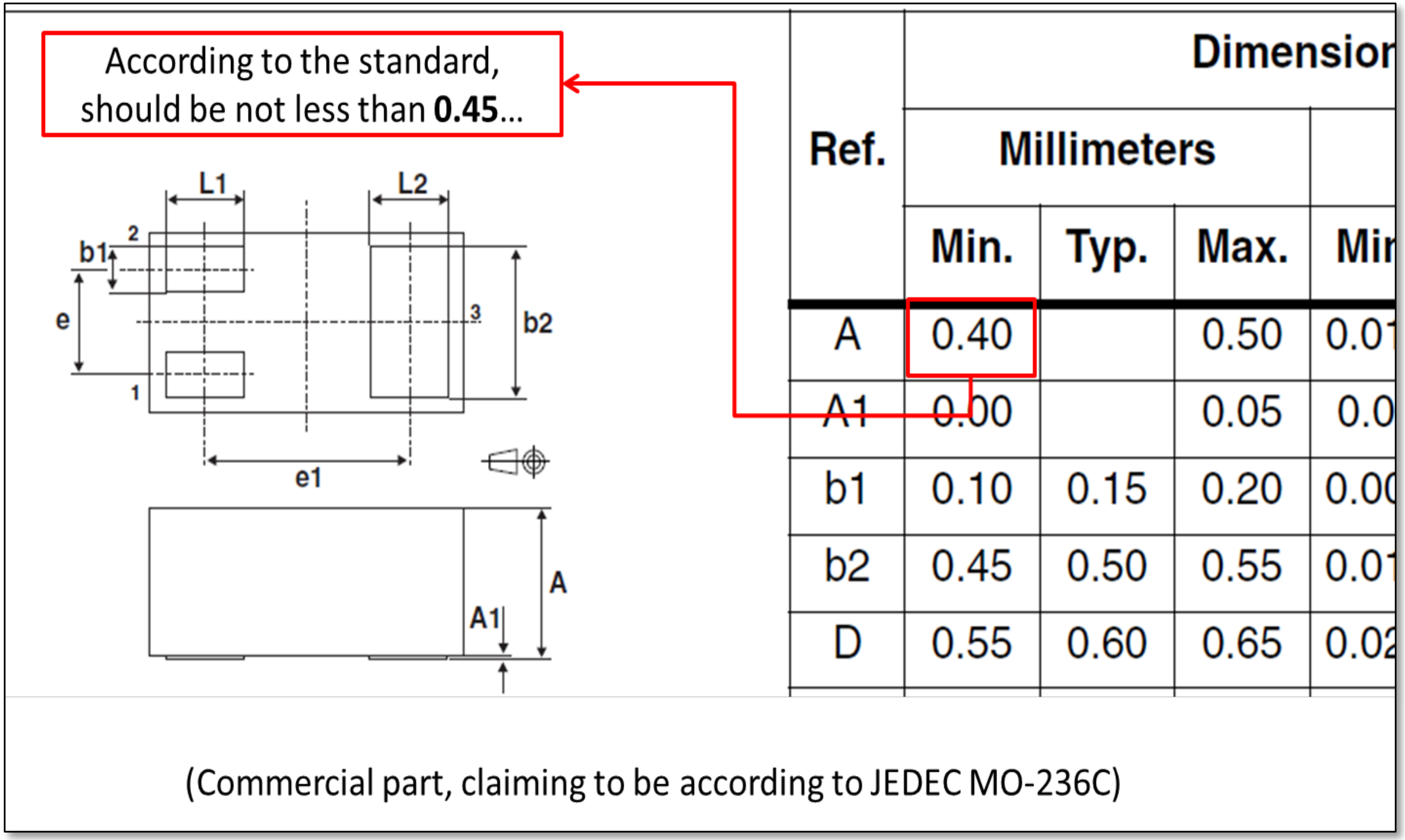


(JEDEC MO-236C)

VAR SYMBOL	AA	
	MINIMUM	NOMIN
A	0.45	–
A1	0.00	–

JEDEC minimum dimension example

Commercial parts conforming to JEDEC

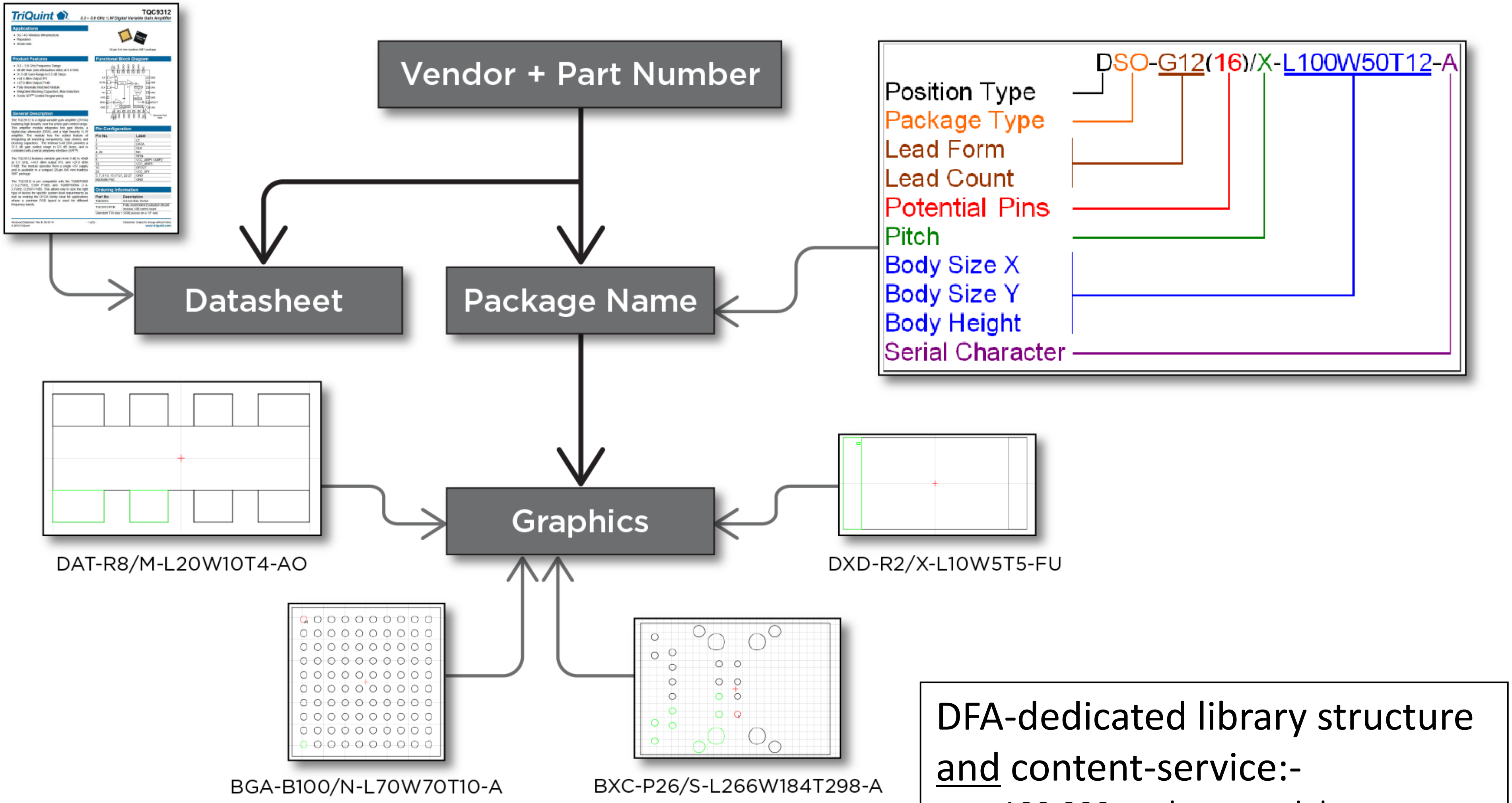


According to the standard, should be not less than **0.45**...

Ref.	Dimension			
	Millimeters			
	Min.	Typ.	Max.	Mi
A	0.40		0.50	0.01
A1	0.00		0.05	0.0
b1	0.10	0.15	0.20	0.00
b2	0.45	0.50	0.55	0.01
D	0.55	0.60	0.65	0.02

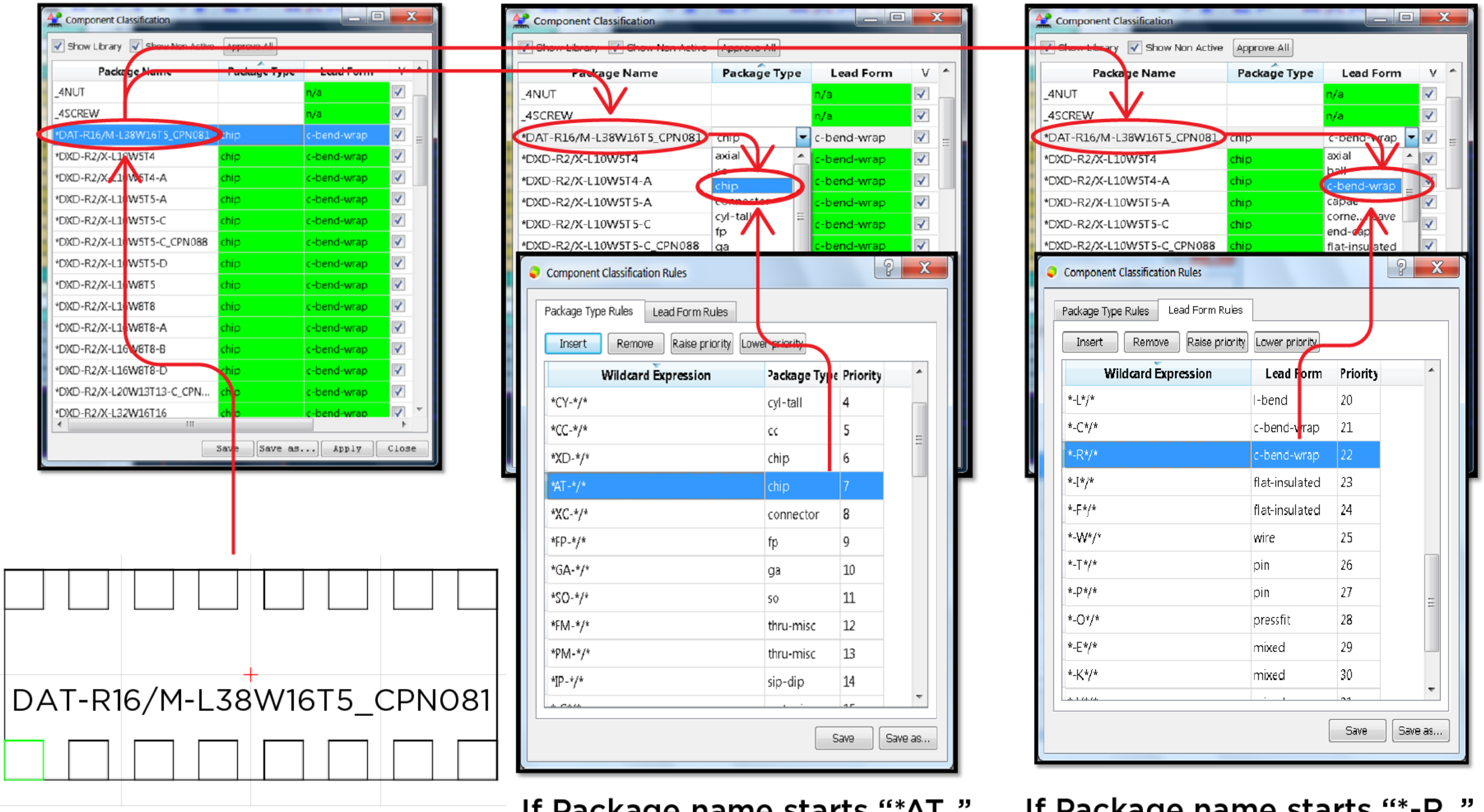
(Commercial part, claiming to be according to JEDEC MO-236C)

(Should be not less than 0.45mm…..)



DFA-dedicated library structure and content-service:-

- ~100,000 package models
- Can describe any purchasable part



Component Classification

☑ Show Library ☑ Show Non Active Approve All

Package Name	Package Type	Lead Form	V
_4NUT		n/a	☑
_4SCREW		n/a	☑
*DAT-R16/M-L38W16T5_CPN081	chip	c-bend-wrap	☑
*DXD-R2/X-L10W5T4	chip	c-bend-wrap	☑
*DXD-R2/X-L10W5T4-A	chip	c-bend-wrap	☑
*DXD-R2/X-L10W5T5-A	chip	c-bend-wrap	☑
*DXD-R2/X-L10W5T5-C	chip	c-bend-wrap	☑
*DXD-R2/X-L10W5T5-C_CPN088	chip	c-bend-wrap	☑
*DXD-R2/X-L10W5T5-D	chip	c-bend-wrap	☑
*DXD-R2/X-L16W8T5	chip	c-bend-wrap	☑
*DXD-R2/X-L16W8T8	chip	c-bend-wrap	☑
*DXD-R2/X-L16W8T8-A	chip	c-bend-wrap	☑
*DXD-R2/X-L16W8T8-B	chip	c-bend-wrap	☑
*DXD-R2/X-L16W8T8-D	chip	c-bend-wrap	☑
*DXD-R2/X-L20W13T13-C_CPN...	chip	c-bend-wrap	☑
*DXD-R2/X-L32W16T16	chip	c-bend-wrap	☑

Save | Save as... | Apply | Close

Component Classification

☑ Show Library ☑ Show Non Active Approve All

Package Name	Package Type	Lead Form	V
_4NUT		n/a	☑
_4SCREW		n/a	☑
*DAT-R16/M-L38W16T5_CPN081	chip	c-bend-wrap	☑
*DXD-R2/X-L10W5T4	axial	c-bend-wrap	☑
*DXD-R2/X-L10W5T4-A	chip	c-bend-wrap	☑
*DXD-R2/X-L10W5T5-A	connector	c-bend-wrap	☑
*DXD-R2/X-L10W5T5-C	cyl-tall fp	c-bend-wrap	☑
*DXD-R2/X-L10W5T5-C_CPN088	ga	c-bend-wrap	☑

Component Classification Rules

Package Type Rules | Lead Form Rules

Insert | Remove | Raise priority | Lower priority

Wildcard Expression	Package Type	Priority
CY-/*	cyl-tall	4
CC-/*	cc	5
XD-/*	chip	6
AT-/*	chip	7
XC-/*	connector	8
FP-/*	fp	9
GA-/*	ga	10
SO-/*	so	11
FM-/*	thru-misc	12
PM-/*	thru-misc	13
IP-/*	sip-dip	14
-C/*		15

Save | Save as...

Component Classification

☑ Show Library ☑ Show Non Active Approve All

Package Name	Package Type	Lead Form	V
_4NUT		n/a	☑
_4SCREW		n/a	☑
*DAT-R16/M-L38W16T5_CPN081	chip	c-bend-wrap	☑
*DXD-R2/X-L10W5T4	chip	axial ball	☑
*DXD-R2/X-L10W5T4-A	chip	c-bend-wrap	☑
*DXD-R2/X-L10W5T5-A	chip	capac	☑
*DXD-R2/X-L10W5T5-C	chip	corne...ave end-cap	☑
*DXD-R2/X-L10W5T5-C_CPN088	chip	flat-insulated	☑

Component Classification Rules

Package Type Rules | Lead Form Rules

Insert | Remove | Raise priority | Lower priority

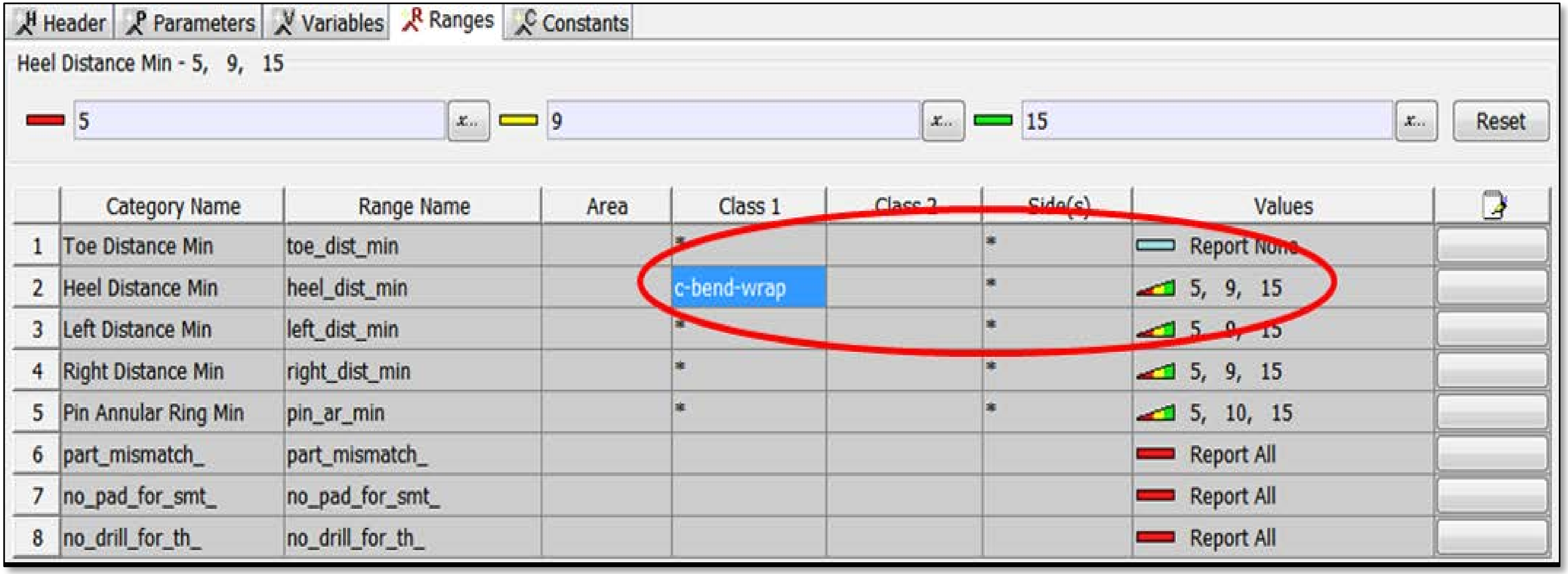
Wildcard Expression	Lead Form	Priority
-L/*	l-bend	20
-C/*	c-bend-wrap	21
-R/*	c-bend-wrap	22
-I/*	flat-insulated	23
-F/*	flat-insulated	24
-W/*	wire	25
-T/*	pin	26
-P/*	pin	27
-O/*	pressfit	28
-E/*	mixed	29
-K/*	mixed	30
		31

Save | Save as...

If Package name starts "*AT.." Then Package Type = "Chip"

If Package name starts "*-R.." Then Lead Form = "c-bend-wrap"

Rules-driven package-type and lead-form derivation

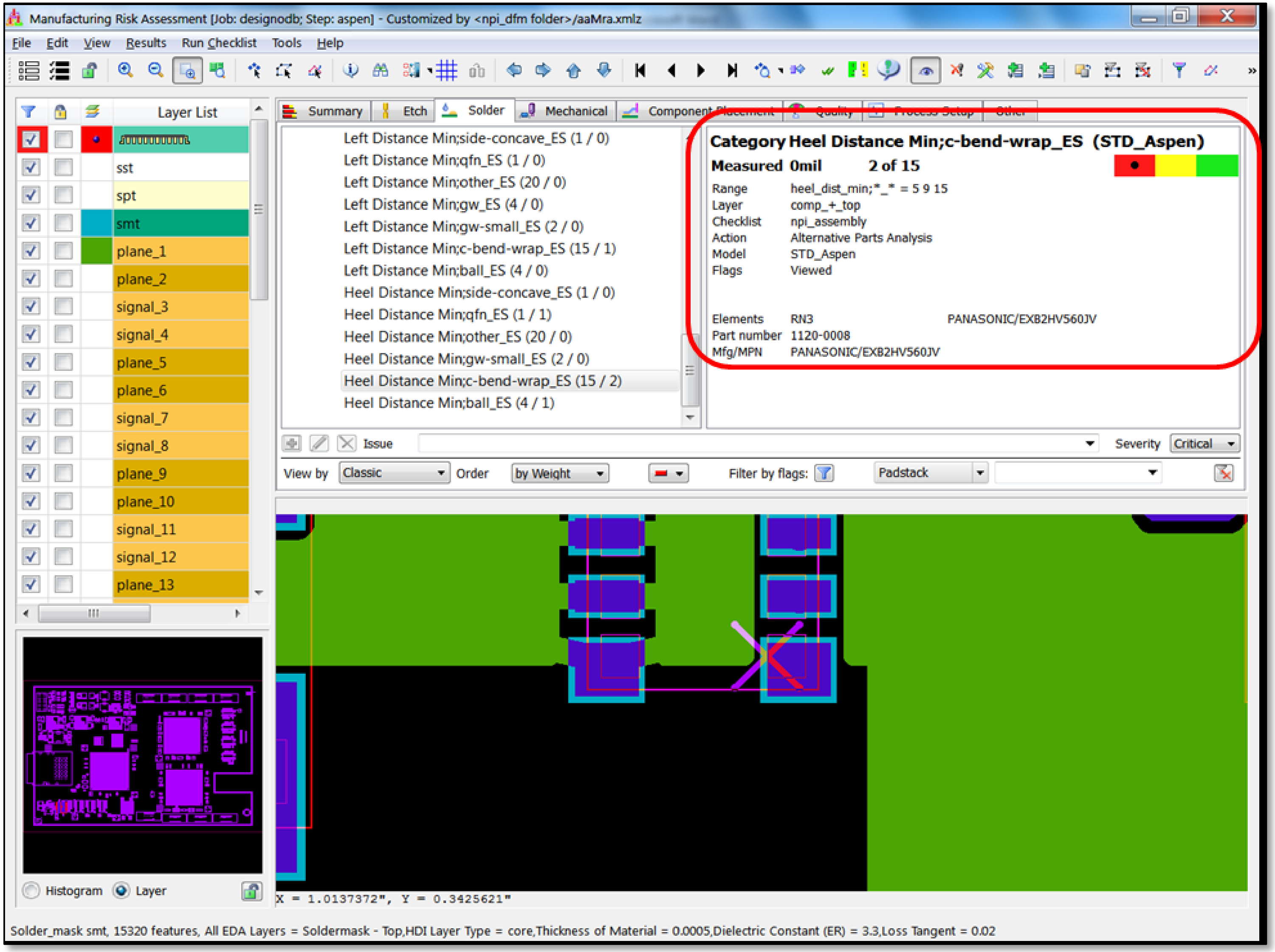


Heel Distance Min - 5, 9, 15

🟥 5 x... 🟨 9 x... 🟩 15 x... Reset

	Category Name	Range Name	Area	Class 1	Class 2	Side(s)	Values	
1	Toe Distance Min	toe_dist_min		*		*	Report None	
2	Heel Distance Min	heel_dist_min		c-bend-wrap		*	5, 9, 15	
3	Left Distance Min	left_dist_min		*		*	5, 9, 15	
4	Right Distance Min	right_dist_min		*		*	5, 9, 15	
5	Pin Annular Ring Min	pin_ar_min		*		*	5, 10, 15	
6	part_mismatch_	part_mismatch_					🟥 Report All	
7	no_pad_for_smt_	no_pad_for_smt_					🟥 Report All	
8	no_drill_for_th_	no_drill_for_th_					🟥 Report All	

Example of DFA rule, according to classifications



Manufacturing Risk Assessment [Job: designodb; Step: aspen] - Customized by <npi_dfm folder>/aaMra.xmlz

☑	□	[illegible]
☑	□	sst
☑	□	spt
☑	□	smt
☑	□	plane_1
☑	□	plane_2
☑	□	signal_3
☑	□	signal_4
☑	□	plane_5
☑	□	plane_6
☑	□	signal_7
☑	□	signal_8
☑	□	plane_9
☑	□	plane_10
☑	□	signal_11
☑	□	signal_12
☑	□	plane_13

Left Distance Min;side-concave_ES (1 / 0)
Left Distance Min;qfn_ES (1 / 0)
Left Distance Min;other_ES (20 / 0)
Left Distance Min;gw_ES (4 / 0)
Left Distance Min;gw-small_ES (2 / 0)
Left Distance Min;c-bend-wrap_ES (15 / 1)
Left Distance Min;ball_ES (4 / 0)
Heel Distance Min;side-concave_ES (1 / 0)
Heel Distance Min;qfn_ES (1 / 1)
Heel Distance Min;other_ES (20 / 0)
Heel Distance Min;gw-small_ES (2 / 0)
Heel Distance Min;c-bend-wrap_ES (15 / 2)
Heel Distance Min;ball_ES (4 / 1)

Category Heel Distance Min;c-bend-wrap_ES (STD_Aspen)
Measured 0mil 2 of 15

Range	heel_dist_min;*_* = 5 9 15
Layer	comp_+_top
Checklist	npi_assembly
Action	Alternative Parts Analysis
Model	STD_Aspen
Flags	Viewed
Elements	RN3 PANASONIC/EXB2HV560JV
Part number	1120-0008
Mfg/MPN	PANASONIC/EXB2HV560JV

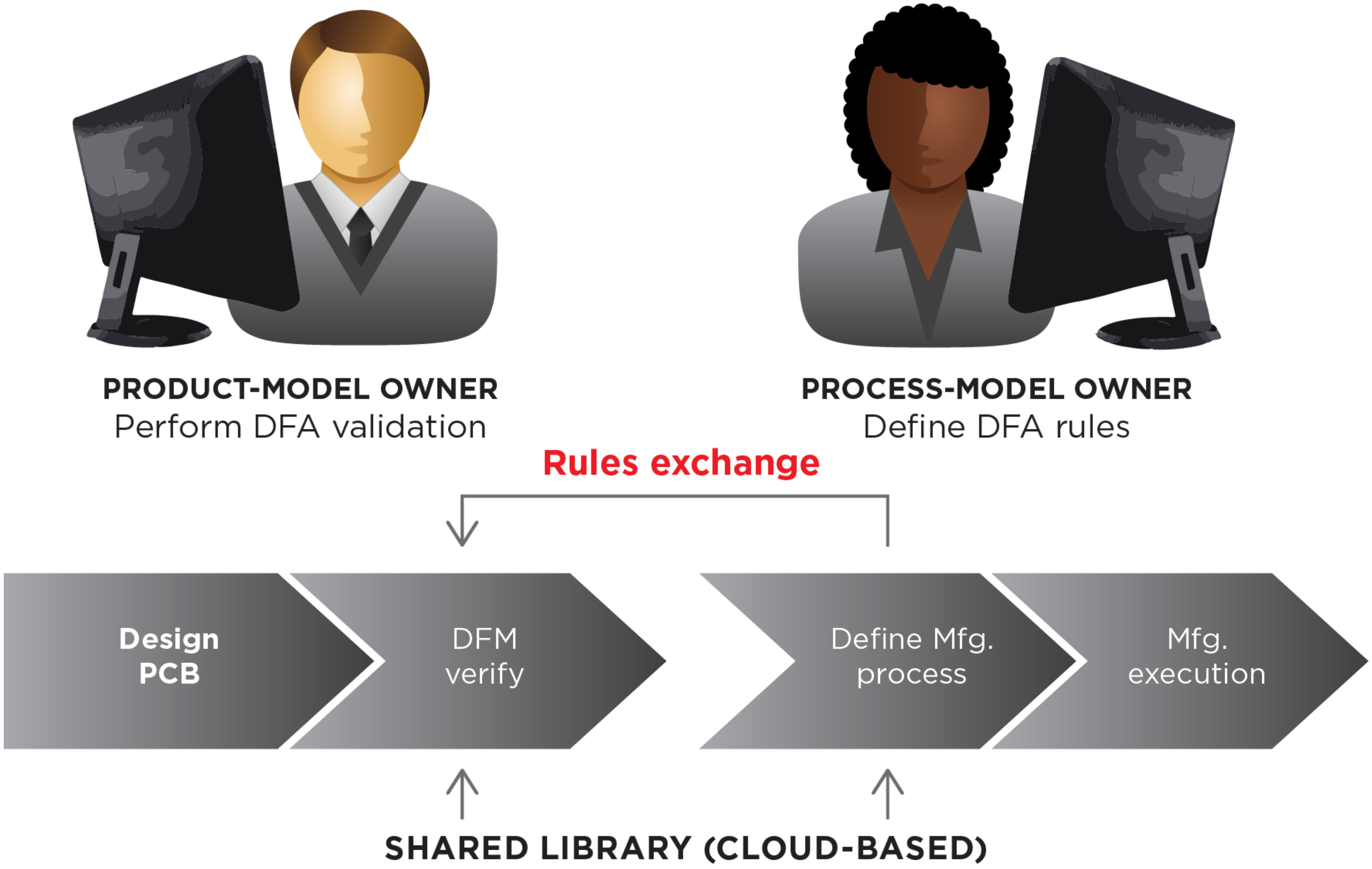
Issue
Severity: Critical
View by: Classic
Order: by Weight
Filter by flags:
Padstack

○ Histogram ● Layer

X = 1.0137372", Y = 0.3425621"

Solder_mask smt, 15320 features, All EDA Layers = Soldermask - Top,HDI Layer Type = core,Thickness of Material = 0.0005,Dielectric Constant (ER) = 3.3,Loss Tangent = 0.02

Example of applying a DFA rule, according to component classification



PRODUCT-MODEL OWNER
Perform DFA validation

PROCESS-MODEL OWNER
Define DFA rules

Rules exchange

Design PCB

DFM verify

Define Mfg. process

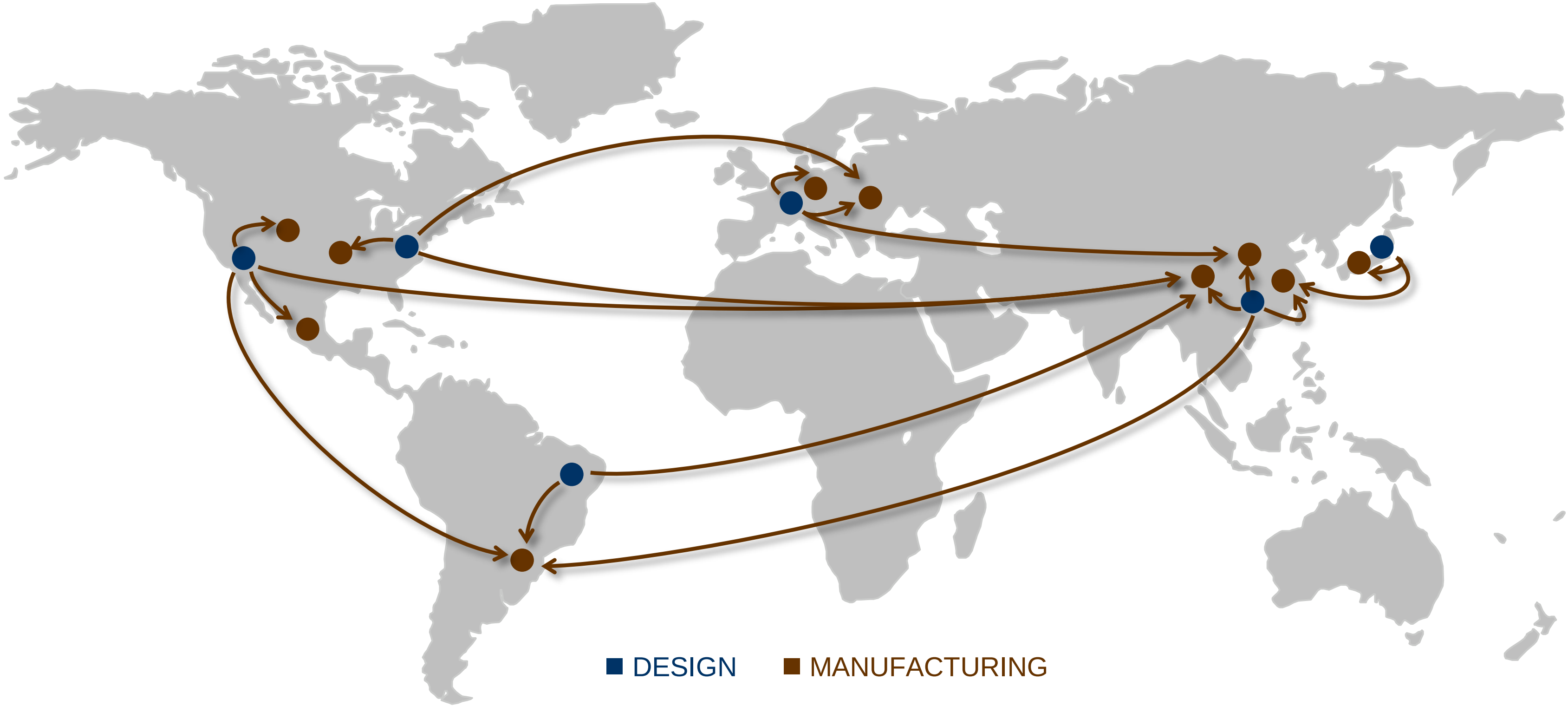
Mfg. execution

SHARED LIBRARY (CLOUD-BASED)

Shared library, classifications and rules enabling portability of DFA

Modern manufacturing: Globalized

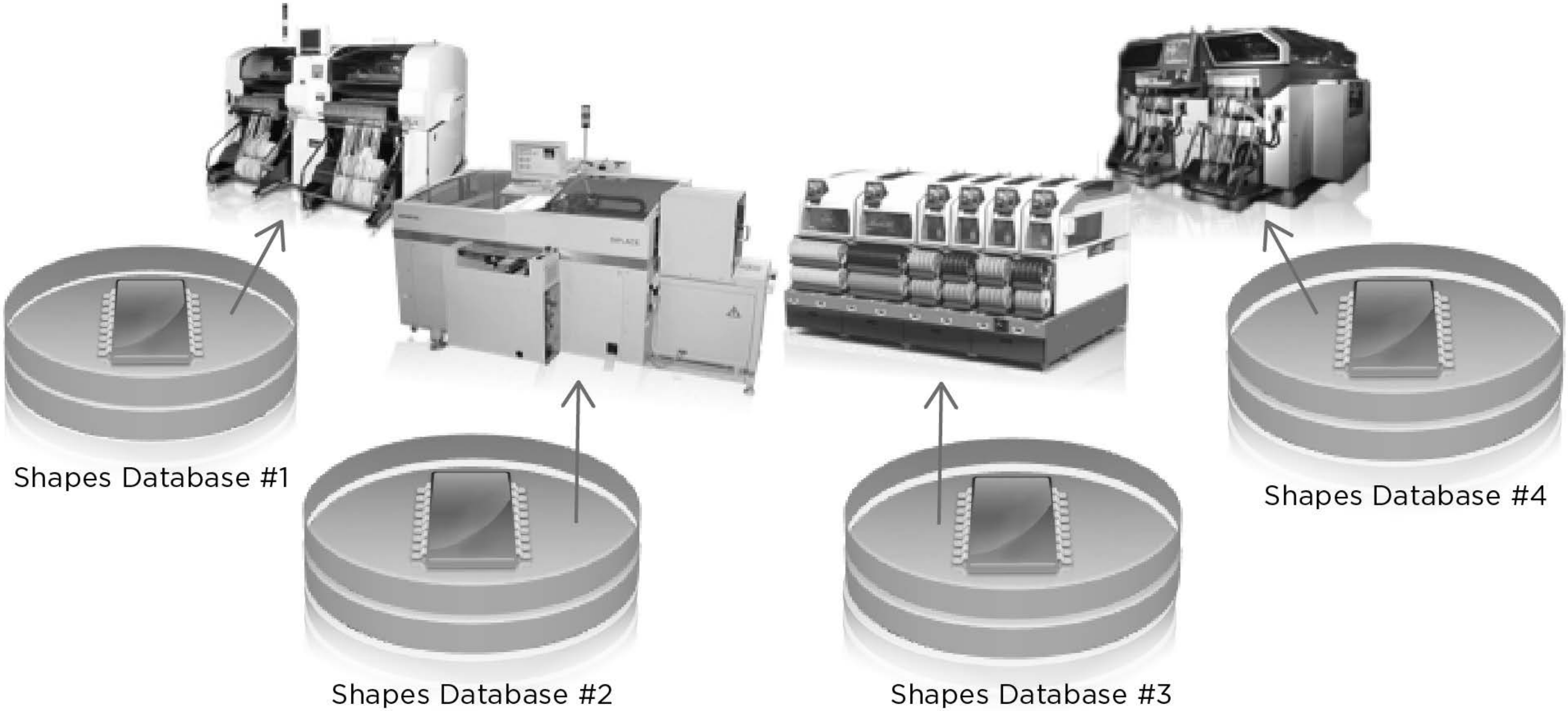
Many-to-Many relationship between designers and manufacturers
Consequence:- Engineering processes conform to the lowest common denominator

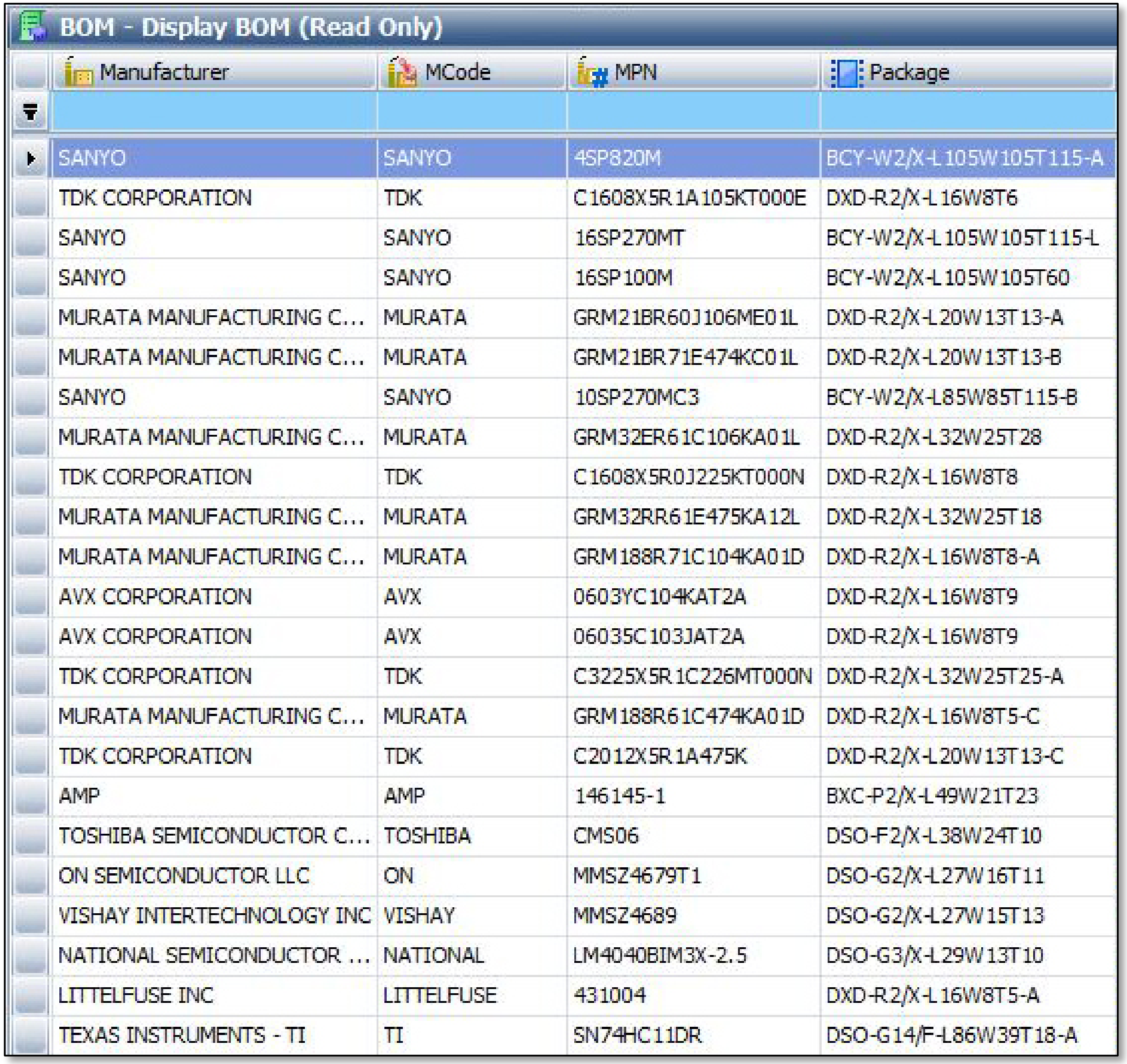


Focus: Libraries for DFA and the assembly & test process

The machine-library problem

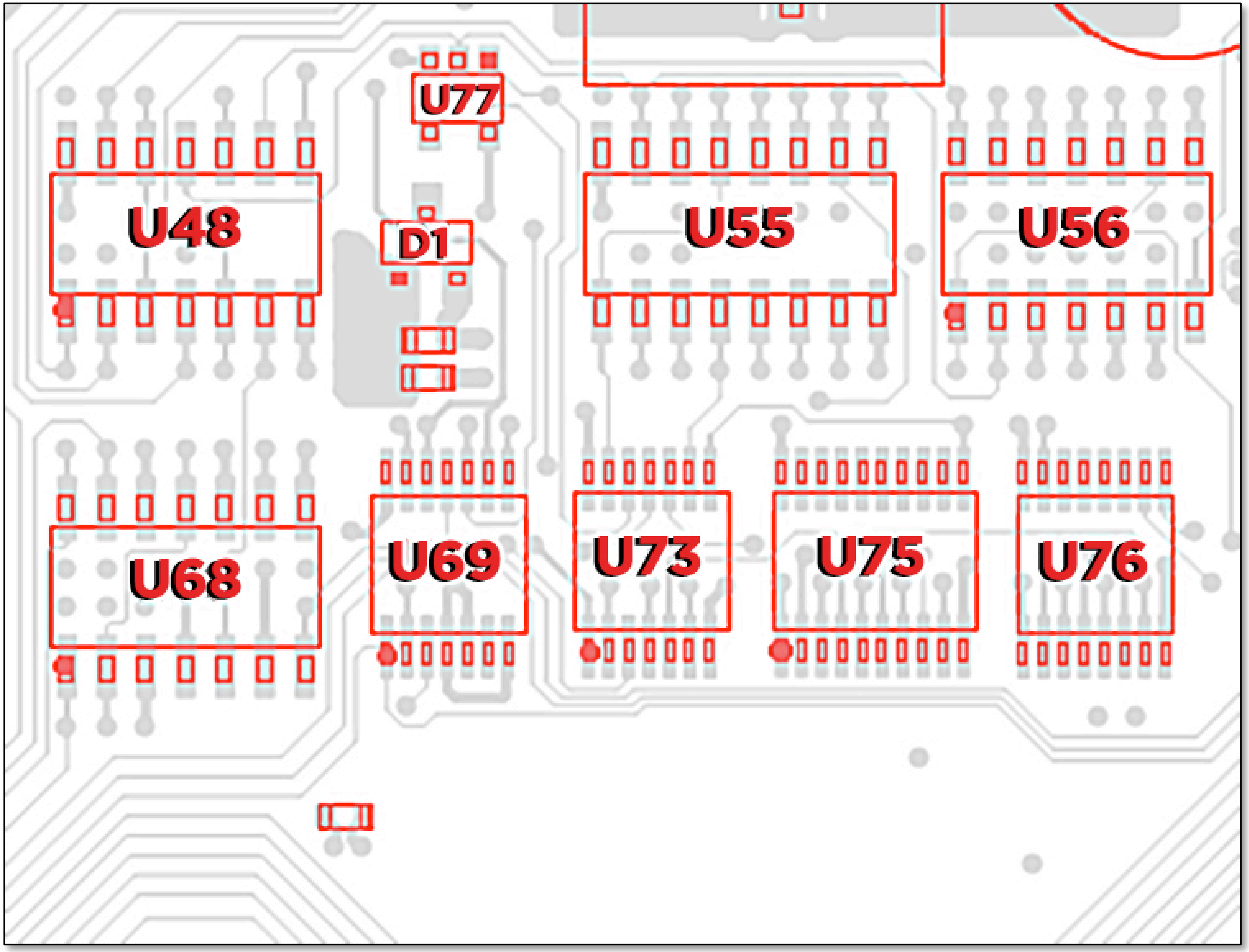
Multiple repeated tasks for the same parts:

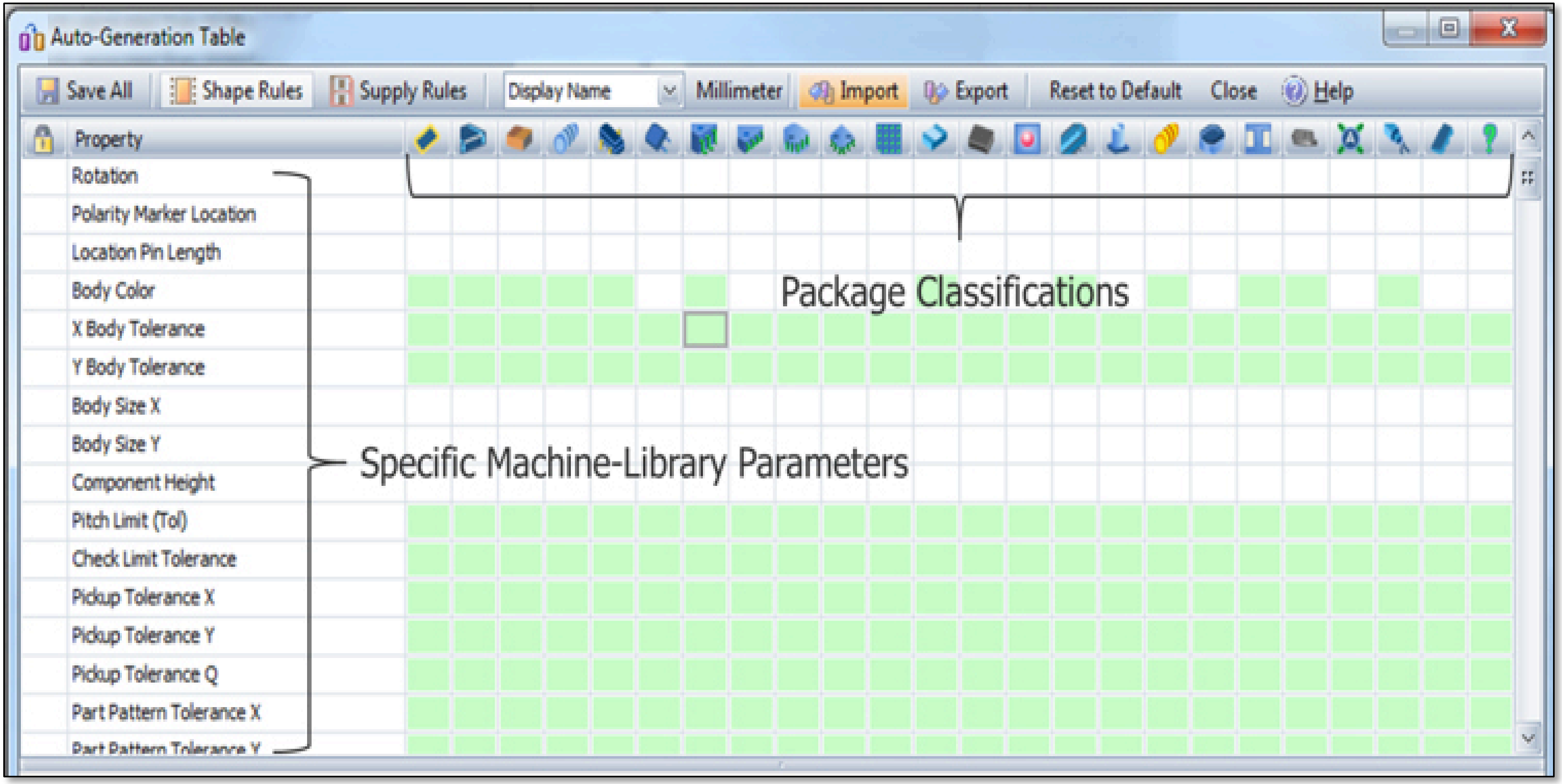




BOM - Display BOM (Read Only)

Manufacturer	MCode	MPN	Package
SANYO	SANYO	4SP820M	BCY-W2/X-L105W105T115-A
TDK CORPORATION	TDK	C1608X5R1A105KT000E	DXD-R2/X-L16W8T6
SANYO	SANYO	16SP270MT	BCY-W2/X-L105W105T115-L
SANYO	SANYO	16SP100M	BCY-W2/X-L105W105T60
MURATA MANUFACTURING C...	MURATA	GRM21BR60J106ME01L	DXD-R2/X-L20W13T13-A
MURATA MANUFACTURING C...	MURATA	GRM21BR71E474KC01L	DXD-R2/X-L20W13T13-B
SANYO	SANYO	10SP270MC3	BCY-W2/X-L85W85T115-B
MURATA MANUFACTURING C...	MURATA	GRM32ER61C106KA01L	DXD-R2/X-L32W25T28
TDK CORPORATION	TDK	C1608X5R0J225KT000N	DXD-R2/X-L16W8T8
MURATA MANUFACTURING C...	MURATA	GRM32RR61E475KA12L	DXD-R2/X-L32W25T18
MURATA MANUFACTURING C...	MURATA	GRM188R71C104KA01D	DXD-R2/X-L16W8T8-A
AVX CORPORATION	AVX	0603YC104KAT2A	DXD-R2/X-L16W8T9
AVX CORPORATION	AVX	06035C103JAT2A	DXD-R2/X-L16W8T9
TDK CORPORATION	TDK	C3225X5R1C226MT000N	DXD-R2/X-L32W25T25-A
MURATA MANUFACTURING C...	MURATA	GRM188R61C474KA01D	DXD-R2/X-L16W8T5-C
TDK CORPORATION	TDK	C2012X5R1A475K	DXD-R2/X-L20W13T13-C
AMP	AMP	146145-1	BXC-P2/X-L49W21T23
TOSHIBA SEMICONDUCTOR C...	TOSHIBA	CMS06	DSO-F2/X-L38W24T10
ON SEMICONDUCTOR LLC	ON	MMSZ4679T1	DSO-G2/X-L27W16T11
VISHAY INTERTECHNOLOGY INC	VISHAY	MMSZ4689	DSO-G2/X-L27W15T13
NATIONAL SEMICONDUCTOR ...	NATIONAL	LM4040BIM3X-2.5	DSO-G3/X-L29W13T10
LITTELFUSE INC	LITTELFUSE	431004	DXD-R2/X-L16W8T5-A
TEXAS INSTRUMENTS - TI	TI	SN74HC11DR	DSO-G14/F-L86W39T18-A

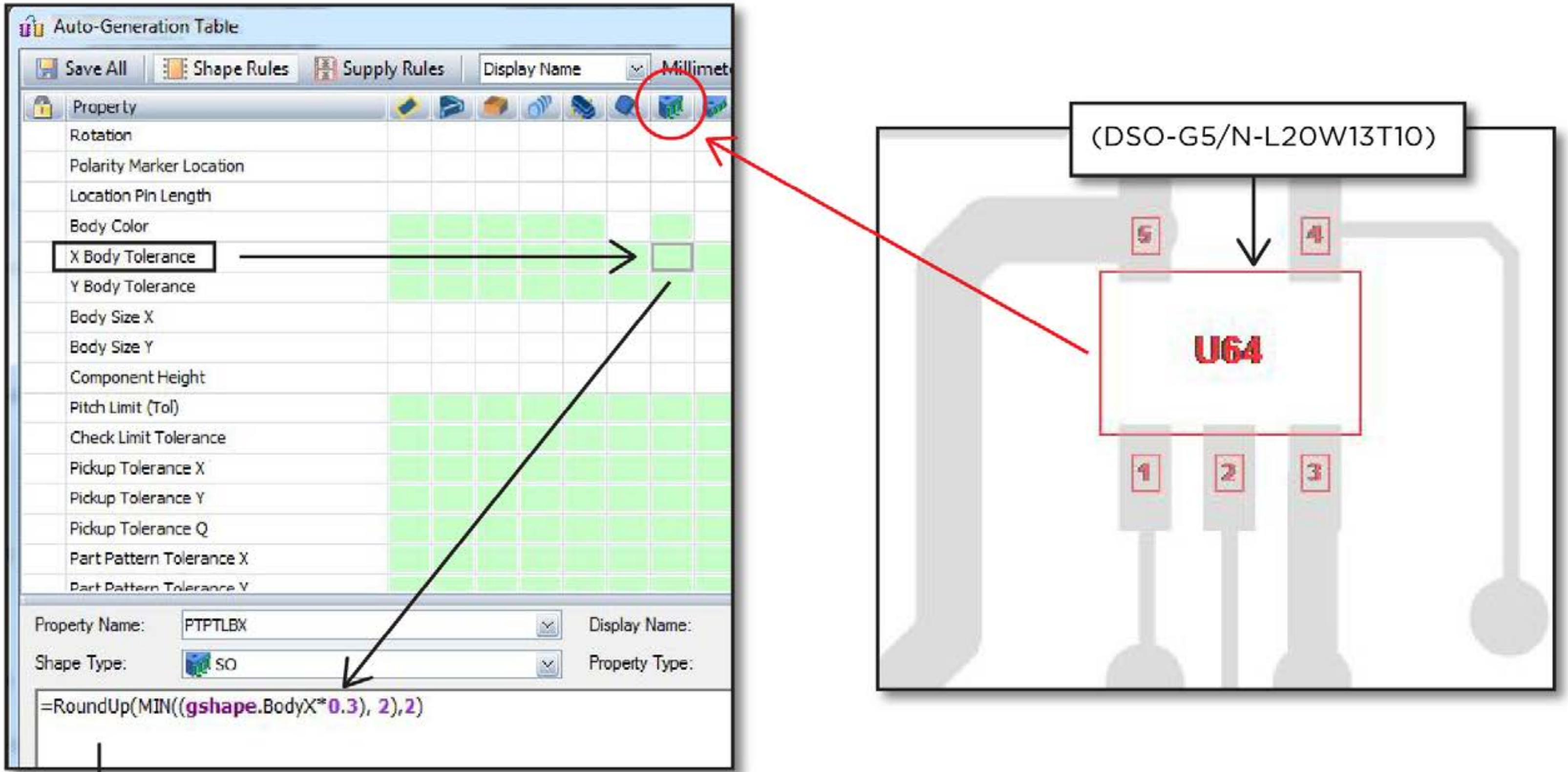

U77
U48
D1
U55
U56
U68
U69
U73
U75
U76



Property																								
Rotation																								
Polarity Marker Location																								
Location Pin Length																								
Body Color	🟩	🟩	🟩	🟩	🟩		🟩										🟩		🟩	🟩		🟩		
X Body Tolerance	🟩	🟩	🟩	🟩	🟩	🟩	🟩	🟩	🟩	🟩	🟩	🟩	🟩	🟩	🟩	🟩	🟩	🟩	🟩	🟩	🟩	🟩	🟩	🟩
Y Body Tolerance	🟩	🟩	🟩	🟩	🟩	🟩	🟩	🟩	🟩	🟩	🟩	🟩	🟩	🟩	🟩	🟩	🟩	🟩	🟩	🟩	🟩	🟩	🟩	🟩
Body Size X																								
Body Size Y																								
Component Height																								
Pitch Limit (Tol)	🟩	🟩	🟩	🟩	🟩	🟩	🟩	🟩	🟩	🟩	🟩	🟩	🟩	🟩	🟩	🟩	🟩	🟩	🟩	🟩	🟩	🟩	🟩	🟩
Check Limit Tolerance	🟩	🟩	🟩	🟩	🟩	🟩	🟩	🟩	🟩	🟩	🟩	🟩	🟩	🟩	🟩	🟩	🟩	🟩	🟩	🟩	🟩	🟩	🟩	🟩
Pickup Tolerance X	🟩	🟩	🟩	🟩	🟩	🟩	🟩	🟩	🟩	🟩	🟩	🟩	🟩	🟩	🟩	🟩	🟩	🟩	🟩	🟩	🟩	🟩	🟩	🟩
Pickup Tolerance Y	🟩	🟩	🟩	🟩	🟩	🟩	🟩	🟩	🟩	🟩	🟩	🟩	🟩	🟩	🟩	🟩	🟩	🟩	🟩	🟩	🟩	🟩	🟩	🟩
Pickup Tolerance Q	🟩	🟩	🟩	🟩	🟩	🟩	🟩	🟩	🟩	🟩	🟩	🟩	🟩	🟩	🟩	🟩	🟩	🟩	🟩	🟩	🟩	🟩	🟩	🟩
Part Pattern Tolerance X	🟩	🟩	🟩	🟩	🟩	🟩	🟩	🟩	🟩	🟩	🟩	🟩	🟩	🟩	🟩	🟩	🟩	🟩	🟩	🟩	🟩	🟩	🟩	🟩
Part Pattern Tolerance Y	🟩	🟩	🟩	🟩	🟩	🟩	🟩	🟩	🟩	🟩	🟩	🟩	🟩	🟩	🟩	🟩	🟩	🟩	🟩	🟩	🟩	🟩	🟩	🟩

Package Classifications

Specific Machine-Library Parameters



Auto-Generation Table

Save All | Shape Rules | Supply Rules | Display Name | Millimet

Property
- Rotation
- Polarity Marker Location
- Location Pin Length
- Body Color
- X Body Tolerance
- Y Body Tolerance
- Body Size X
- Body Size Y
- Component Height
- Pitch Limit (Tol)
- Check Limit Tolerance
- Pickup Tolerance X
- Pickup Tolerance Y
- Pickup Tolerance Q
- Part Pattern Tolerance X
- Part Pattern Tolerance Y

Property Name: PTPTLBX

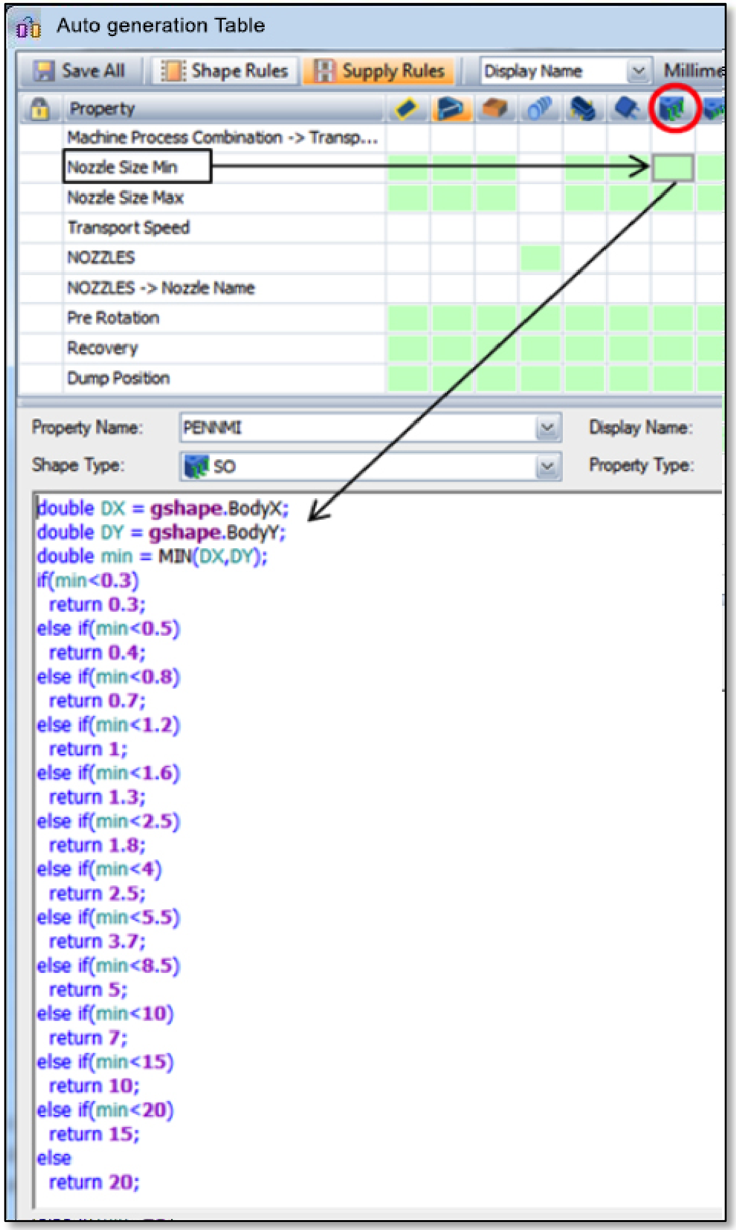
Display Name:

Shape Type: SO

Property Type:

```
=RoundUp(MIN((gshape.BodyX*0.3), 2),2)
```

X BODY TOLERANCE
Use Body x dimension multiplied by 0.3
Check it is at least 2
Round up to next integer
Result is the machine specific X Body Tolerance

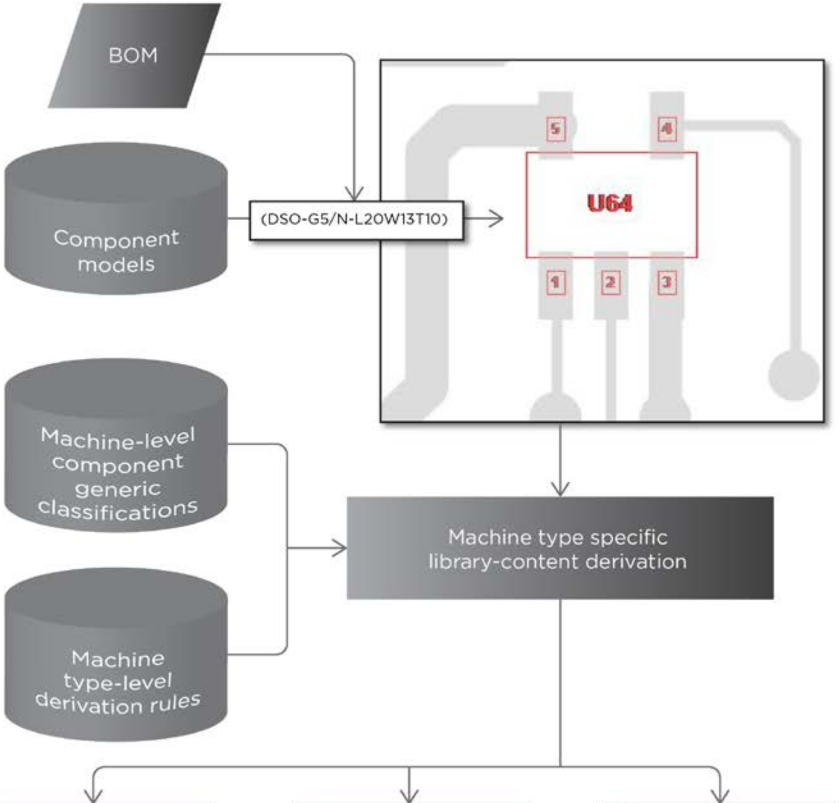


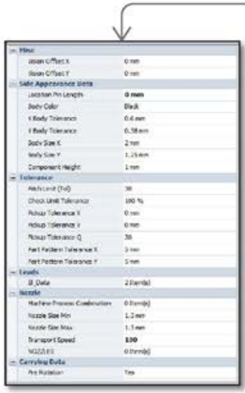
Display Name

Property								
Machine Process Combination -> Transp...								
Nozzle Size Min	🟩	🟩	🟩		🟩	🟩	🟩	🟩
Nozzle Size Max	🟩	🟩	🟩		🟩	🟩	🟩	🟩
Transport Speed								
NOZZLES				🟩				
NOZZLES -> Nozzle Name								
Pre Rotation	🟩	🟩	🟩	🟩	🟩	🟩	🟩	🟩
Recovery	🟩	🟩	🟩	🟩	🟩	🟩	🟩	🟩
Dump Position	🟩	🟩	🟩	🟩	🟩	🟩	🟩	🟩

Property Name: PENNMI
Display Name:
Shape Type: SO
Property Type:

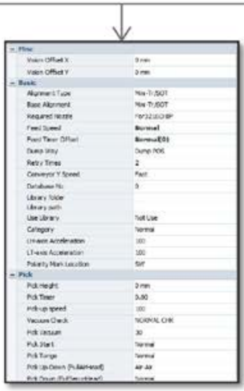
```
double DX = gshape.BodyX;
double DY = gshape.BodyY;
double min = MIN(DX,DY);
if(min<0.3)
  return 0.3;
else if(min<0.5)
  return 0.4;
else if(min<0.8)
  return 0.7;
else if(min<1.2)
  return 1;
else if(min<1.6)
  return 1.3;
else if(min<2.5)
  return 1.8;
else if(min<4)
  return 2.5;
else if(min<5.5)
  return 3.7;
else if(min<8.5)
  return 5;
else if(min<10)
  return 7;
else if(min<15)
  return 10;
else if(min<20)
  return 15;
else
  return 20;
```


BOM
Component models
(DSO-G5/N-L20W13T10)
5
4
U64
1
2
3
Machine-level component generic classifications
Machine type-level derivation rules
Machine type specific library-content derivation



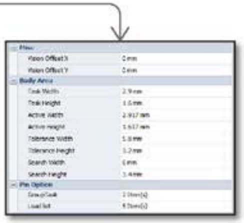
Misc	
Vision Offset X	0 mm
Vision Offset Y	0 mm
Side Appearance Data	
Location Pin Length	0 mm
Body Color	Black
X Body Tolerance	0.4 mm
Y Body Tolerance	0.38 mm
Body Size X	2 mm
Body Size Y	1.25 mm
Component Height	1 mm
Tolerance	
Pitch Limit (Tol)	30
Check Limit Tolerance	100 %
Pickup Tolerance X	0 mm
Pickup Tolerance Y	0 mm
Pickup Tolerance Q	30
Part Pattern Tolerance X	3 mm
Part Pattern Tolerance Y	5 mm
Leads	
B_Data	2 Item(s)
Nozzle	
Machine Process Combination	0 Item(s)
Nozzle Size Min	1.3 mm
Nozzle Size Max	1.3 mm
Transport Speed	100
NOZZLES	0 Item(s)
Carrying Data	
Pre Rotation	Yes

PICK & PLACE MODEL-1



Misc	
Vision Offset X	0 mm
Vision Offset Y	0 mm
Basic	
Alignment Type	Mini-Tr,SOT
Base Alignment	Mini-Tr,SOT
Required Nozzle	[illegible]
Feed Speed	Normal
Feed Timer Offset	Normal(0)
Dump Way	Dump POS
Retry Times	2
Conveyor Y Speed	Fast
Database No	0
Library Folder	
Library path	
Use Library	Not Use
Category	Normal
LH-axis Acceleration	100
LT-axis Acceleration	100
Polarity Mark Location	SW
Pick	
Pick Height	0 mm
Pick Timer	0.00
Pick-up speed	100
Vacuum Check	NORMAL CHK
Pick Vacuum	30
Pick Start	Normal
Pick Torque	Normal
Pick Up Down (PulseHead)	Air Air
Pick Down (FullServoHead)	Normal

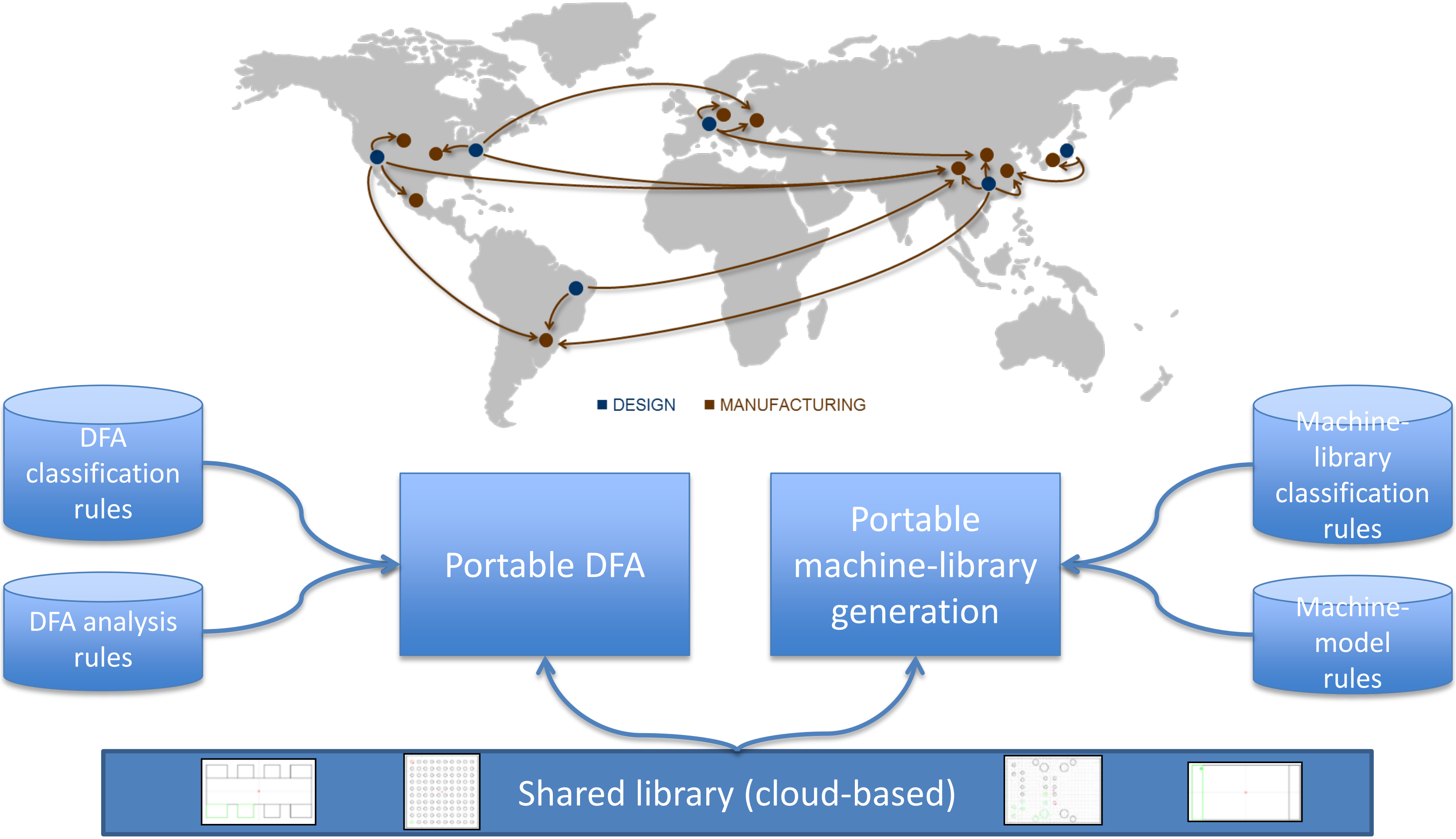
PICK & PLACE MODEL-2



Misc	
Vision Offset X	0 mm
Vision Offset Y	0 mm
Body Area	
Task Width	2.9 mm
Task Height	1.6 mm
Active Width	2.917 mm
Active Height	1.617 mm
Tolerance Width	1.0 mm
Tolerance Height	1.2 mm
Search Width	0 mm
Search Height	1.4 mm
Pin Option	
Group Task	2 Item(s)
Load list	8 Item(s)

AOI MODEL-1

Combined solution overview



DFA classification rules

DFA analysis rules

Portable DFA

Portable machine-library generation

Machine-library classification rules

Machine-model rules

Shared library (cloud-based)