Large Thin Organic PTFE Substrates for Multichip Applications

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Abstract

Very high performance computer applications have created a demand for large organic substrates capable of interconnecting one or a few ASIC semiconductor devices with packaged memory devices. The electrical advantages offered by the use of a thin PTFE composite substrate were coupled with intrinsic mechanical advantages to create very high performance applications. The application development required interactions of design, fabrication, and new manufacturing technology to obtain rapid prototype production and allow a successful ensuing manufacturing ramp. One such package application involved using a 0.47mm thick PTFE substrate in a 65mm size format, having 8 memory devices surrounding a central ASIC, with numerous capacitors, in double-sided format. The application was developed as a pluggable module by using SMT attached pin/socket, and has a heatspreader which is in thermal contact with all devices and further provides flatness control once attached using thermal and electrically conductive adhesives. Assembly procedures to successfully handle the thin flexible substrate in volume were developed. Other applications are being developed in both pinned and BGA connection formats, and will have similar characteristics.

This advanced packaging technology allows the ASIC devices to rapidly communicate with the memory devices through the use of low-k materials in conjunction with the substrate's stripline format. This avoids the need for PWB complexity, and provides for a very compact, lightweight application. The composite substrate also includes low thermal expansion layer materials to provide for high reliability to the die, the memory devices, and the interconnection. Because of the attractive packaging characteristics, applications in high performance military dataprocessors as well as commercial telecom switches are being qualified for high volume production and assembly, with more than one application currently in high volume ramp. The integrated design, fab, and assembly facilities at Endicott Interconnect Technology allowed several large multichip applications to go from paper concept to ramp in approximately one year, showing that synergistic use of proven, existing substrate technology in new complex applications can be very successful.

Multichip Applications with Dense Component Layout

The relentless drive toward miniaturization of electronics systems, in part to obtain better performance, has created a need for system in package (SIP) utilizing the high speed PTFE based laminates. This is referred to as a PTFE-SIP laminate. The high-speed nature of the PTFE based laminate material, having a dielectric constant of 2.7, provides for signal propagation much faster than a typical motherboard. Since an SIP configuration avoids a signal path through the BGA, a primary source of filtering, higher overall system speeds can be realized by keeping memory and processor on the same high speed chip package. The compliant PTFE based laminate was originally designed to utilize optimized laminate properties for overall system performance and extreme reliability – for a single die [1-6]. It is available in single-chip, stiffener format to 55mm size with I/O count of over 2700 BGA at 1mm pitch, currently supporting large lead-reduced applications. This paper describes the adaptation of that PTFE laminate usage from single chip package format towards multiple chip format, to enable high performance SIP applications. An example of a multi chip format application [7] is shown in Figure 1.

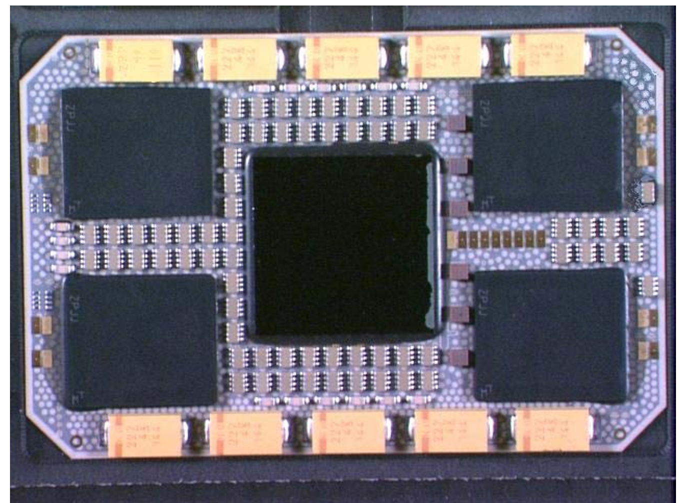

Figure 1. PTFE laminate in SIP format, showing topside components (lid removed) including ASIC die, 4 SRAM devices, multiple formats of passive components. Package length is 65mm.

The main differences are related to allocation of laminate real estate. For each package format, it was desirable to maintain a common laminate cross section. PTFE-SIP laminate has a fairly thin section, 0.47 mm thick. It also utilizes compliant materials, so as to avoid high stress to the attached components. For the single-chip application, significant laminate real estate was devoted to flatness control of this thin section, through the use of an adhesively bonded stiffener. For example, a common ASIC die size of 14mm would have an ‘unsupported’ region in the die cavity of no more than 20mm square. To keep this unsupported region flat, the remainder of the laminate was covered with a stiffener, save for a few passive openings. The stiffener was CTE-matched to the laminate to provide flatness control through reflow temperature ranges, for successful die assembly reflow processes. Several examples of stiffener

configurations are shown in Figure 2, for single-chip package formats.

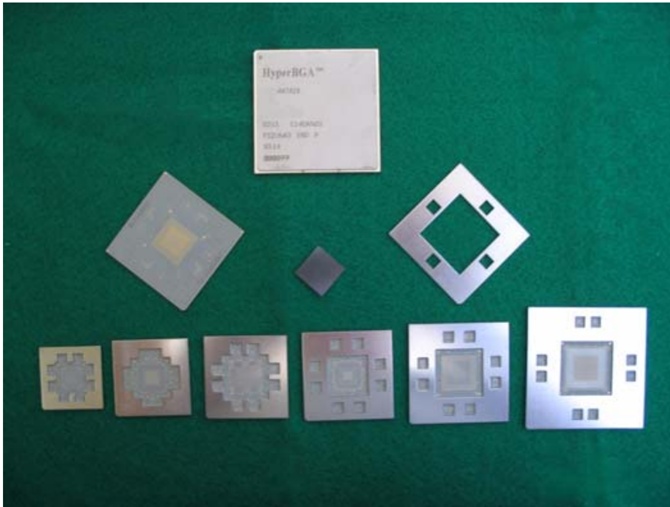

Figure 2. PTFE based laminates in various single-chip stiffener formats. Bottom row, left to right: PTFE based laminates with stiffener, size range from 31 to 52.5mm. Middle row, 42.5mm laminate, an ASIC die, and corresponding stiffener. Top, a completed 52.5mm package.

In order to allow for more die, memory, and passive placement, high performance SIP configurations had essentially no real estate budgeted for a traditional perimeter stiffener. This had profound effects on assembly process and associated tooling needs. At least one SIP application that is currently in production has a fairly large size, 65mm. This meant the 'unsupported' laminate area would increase from 20mm square (remainder having a perimeter stiffener) to 65mm (no stiffener), utilizing the same thin laminate section - more than tripling the unsupported laminate aspect ratio. Also, applications with a small package (40mm) were demonstrated with very large die (26mm) leaving little or no room for a perimeter stiffener. Even smaller package sizes (19x25mm) were produced in multi chip format. Several examples of PTFE-SIP package components are shown as a group in Figure 3, for relative size comparisons. A close up of the largest area package is shown in Figure 4.

It was obvious that, without a stiffener, the package lid would now provide the majority of flatness control to the finished PTFE-SIP package. Now serving a double role as "stiffener plus lid", this structural function was further combined with it's thermal function. For one PTFE-SIP application, the lid also became part of the actuation system, as a surface mount technology (SMT) pin/pluggable approach was chosen instead of ball grid array (BGA). The lid was used to apply loading to actuate and deactuate the package system. This drove the lid design to have sufficient bending stiffness and strength to avoid high localized stresses and possible debonding from the components. In another PTFE-SIP application, the lid was further electrically grounded to selected portions of the laminate, providing yet another combined function and further complicating the assembly process with multiple adhesives.

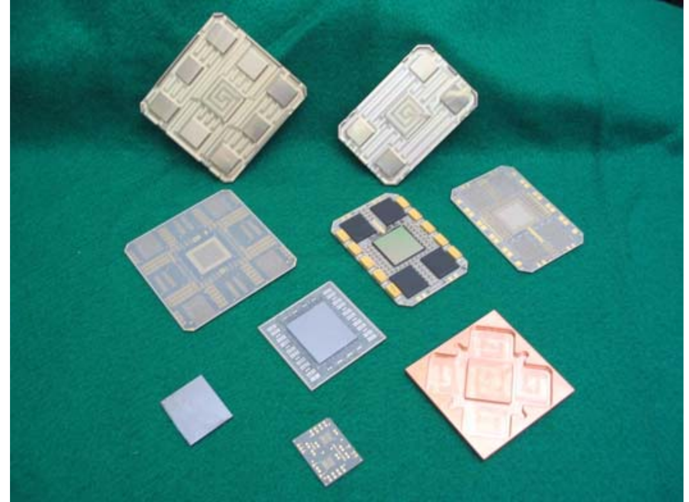

Figure 3, Examples of various PTFE-SIP packages and components. Top row is a bottom view of heatspreaders, shown flipped from corresponding PTFE-SIP laminates. The largest laminate (top left) is 68x65mm laminate to interconnect a die, 8 memory devices, and multiple passives. The smallest laminate (bottom center) is 25x19mm size, designed for 2 die, plus passives. Below is shown a 26mm ASIC, mounted on/off a laminate. Bottom right is shown an example of a milled copper lid of stepped height design.

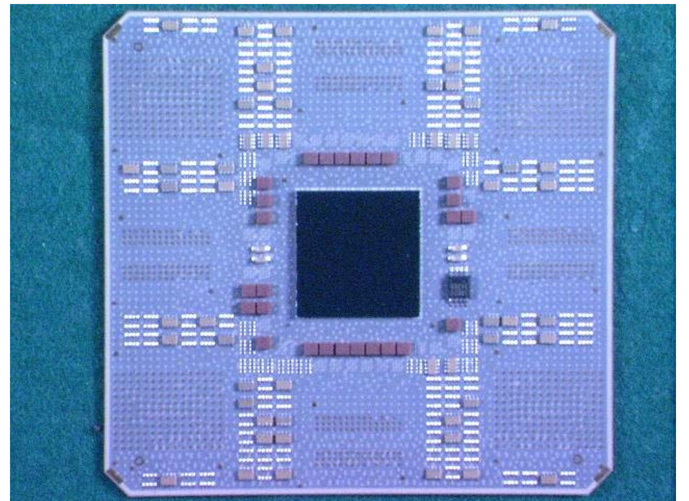

Figure 4. PTFE-SIP in MCM format, 68x65mm size. Shown partially assembled with 17mm ASIC and selected passives attached, designed to accommodate up to 8 additional memory devices and backside passives (not shown).

All of these factors led to the need for a balanced development and design process that equally considered and solved problems posed by the component assembly process, system requirements, subsrate characteristics, component attributes, and component manufacturing needs.

Substrate Design Considerations

The design phase for these types of applications are often highly underestimated from a routing and performance perspective. The customer may often have very specific electrical criteria for impedance, noise, and other parasitics as well as a requirement for a low inductance power distribution network. All of these play hand in hand throughout the design phase. Coupled with a need to dissipate a great amount of heat from the device and maintain a 10 year field application reliability grade that is at least equivalent to current applications today will coerce the application and design team to fully comprehend the structural, mechanical, electrical, and environmental needs of each specific application.

One of the largest concerns with the initial design phase of these high performance substrates is often centered around the initial component layout and the wireability demands between these components. This is a hallmark of SIP applications also known as FCAMP, flip chip and memory package, where applications have a central ASIC device and are closely surrounded by high speed memory devices as well as a litany of decoupling capacitors and terminating resistors. It will be advantageous for the SIP design team to initially focus on the wireability to ensure that the demands of the interconnects between the component as well as the I/O of the package is achievable. Assembly processes can also play a role, but with careful planning and design, highly packed PTFE-SIPs can readily be designed and fabricated.

With most organic packages, the best design starting point is to evaluate the escape from the central ASIC or processor. This is done to determine if the wiring demand from the device to the peripheral units can be achieved. Making necessary adjustments is an area that truly demands a "system level" approach to optimize the SIP layout. Simply put, the simplicity of the final substrate design solution hinges on the need for the silicon design team to locate their I/O on the die in such a pattern that truly minimizes the crossovers within the SIP package physical design layout. In other words, the goal for the physical layout of the ASIC I/O, if at all possible, should be to ensure that the majority of the interconnections are in rough proximity. For example, it is desirable for I/O residing in the northwest quadrant of the ASIC to route to the memory and peripheral devices in the very same northwest quadrant of the substrate, as shown in Figure 5. What is the majority of the wiring ? Upwards of 90% of the wiring in this specific quadrant should be segregated to the interconnections to the devices within this very same quadrant in order to ensure a simple, straightforward approach to the physical design layout for the substrate can be achieved. If the design teams can not achieve this optimal rule of thumb layout, the result is more often than not a 2 to 3 times higher price point for a 30 or 40 layer multilayer thin film ceramic substrate when compared to a high performance PTFE-SIP substrate. In addition, the PTFE-SIP substrate fabrication cycle is most often considerably less than a comparable ceramic substrate.

Other design options are available to enhance the wiring density of PTFE-SIP substrates. Close evaluation of the voltage and ground flip chip ball assignments on the silicon may allow the designer to buss adjacent power C4 bumps together on one of the upper layers in the x-section, and drop a single via for two or more common power flip chip bumps. This technique can be used for common ground bumps, and can have the effect of opening up valuable wiring channels in the signal layers beneath the power C4 that have been bussed. A further advantage is reduction of the overall via count in the design, which will reduce the price. Of course, this technique is often criticized for adding to the overall inductance in the power distribution network; this is a key electrical factor when the ASIC has a high percentage of drivers that are switching on and off simultaneously. The point here is, in reaching an optimized design, all parties in the design process must come to agreement and possibly some compromise. The engineering process which keeps focused on a balance of optimized performance, price, and manufacturability will provide the best overall value to the customer. Every diligent package design engineer strives to keep price sensitivity, and the ability to enhance product yield in the back of his mind. At the same time, and what chip designer does not demand the best performing platform from silicon? But commence to look at a comparable ceramic SIP design, especially those that utilize a mesh voltage or ground plane for power distribution, and factor in the point that the ceramic substrate will be 3 to 5 times as thick as your PTFE-SIP alternative; then quantify the electrical performance difference. Most likely, bussing a few dozen voltage bumps provides minimal overall impact on the inductance in the power path. Additional bussing may alleviate the need to drive down to design groundrule minimums for line width and space (as a result of fewer thru vias), so overall the design team will produce a design point that is simply a better yielding application. Other up and coming high performance organic solutions are delving further into the high end of the high end SIP application space and will shortly offer up true organic alternatives to 30 to 50 layer count ceramic MCM's.

"Monday morning quarterbacks" will soon realize that an already released product will very rarely be redesigned into SIP format, unless it enables a new form factor for the product or extreme cost reduction, or extreme performance enhancement. This may be a result after component sweep into an ASIC, wherein some of the peripheral components in an existing design have been swept into the ASIC, truly allowing additional real estate gains on the PWB.

Other gains by packaging in a high performance organic solution may also include reduced weight of the system; an organic solution will typically offer a significant reduction over ceramic counterparts. This can have a distinct advantage in certain military application spaces – even land-based systems which may be highly dense. The total interconnect length, total parasitic capacitance, critical net wiring delay , and even noise performance will be enhanced in PTFE-SIP environment. These factors can further be realized with higher component reliability due to lower operating temperatures, since the thin form factor of a PTFE-SIP typically allows more vertical space allocation to heatspreaders (thicker material for better heat spreading) or air-cooling solutions (offering larger heatsinks/more airflow).

These few design factors mentioned here, and a multitude of other specific requirements, must all be balanced during the design phase. The engineering support teams that can provide rapid and accurate evaluations of chip-to-system level concerns, and respond with offerings of highly optimized PTFE-SIP packaging solutions, will allow for multiple 'turns' of design, better solutions, and therefore more optimal system utilization and integration.

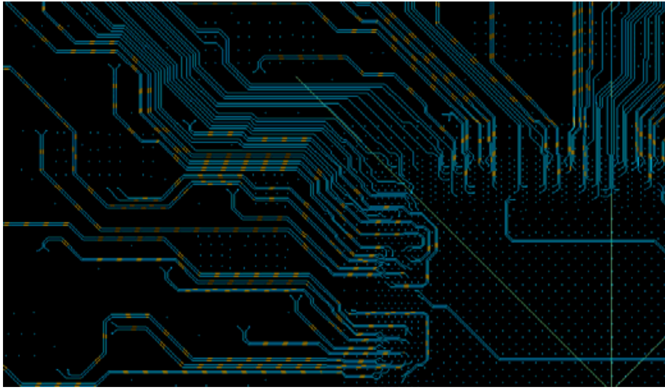

Figure 5. Typical escape pattern on a stripline signal layer in the northwest quadrant of a high performance PTFE-SIP substrate.

Pre-Production Process Development

Previously, compliant PTFE-based laminate products were generally designed and qualified for use in the format of a single die with stiffener; a limited number of passives were sometimes included. The laminate materials are compatible with lead-free reflow temperature. The stiffener was applied prior to die attach, and the lid was applied after die attach. For PTFE-SIP application without a stiffener, the concept of using the lid for package flatness control would therefore only be useful after it is attached. Practically, lid attach can only happen after die attach. Given the thin nature of the PTFE-SIP substrate and aspect ratios being contemplated, to enable high yield die attach it was expected that interim flatness control was required. This was accomplished through the development of in-process fixtures, designed to be compatible with standard inline placement tools and reflow ovens. Various fixtures were designed and fabricated to hold the large substrate size (65mm) flat during component placement, reflow, wash, bake, underfill dispense, underfill cure, lid attach, and inspections. Several toolset iterations were evaluated in development; for example, at least six versions of the reflow fixtures were used. One tray example is depicted in Figure 6. It was found that several designs would allow high yield assembly. In the end, criteria associated with volume piece handling, durability, and cost were more challenging than technical feasibility. The exact nature of how these assembly fixtures work remains proprietary with EI technologies. However, it was found that the designs using larger substrate sizes (>45mm) actually worked in favor obtaining good flatness, and smaller substrate sizes did not need very much flatness control owing to balanced substrate design. Thus, the entire range of compliant PTFE-based substrate production was found to be easily 'flattenable' without use of a permanently bonded stiffener, so long as appropriate processing fixtures were employed. Mimimal interference with the component layout and wiring design process was needed; highly packed PTFE-SIP formats were found to be assembled with relative ease.

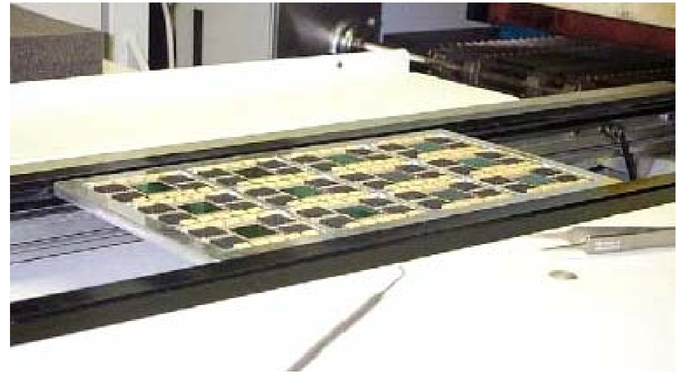

Figure 6. Tray fixture example, 3x4 package processing.

The lid was designed so that small, specific regions of the substrate were directly contacted and used as areas for adhesive bonding. The thermally conductive adhesives were also dispensed in larger regions over other components, such as the die. In this manner, the lid simultaneously bonded to components of various heights as well as certain areas of the substrate. The lid, therefore was of a stepped height design. An example of a lid, flipped and positioned opposite it's PTFE-SIP laminate example, is shown in Figure 7. In searching for appropriate materials, aluminum-silica-carbide (ALSIC), copper, aluminum, and other lid material were considered. All were found to be feasible, but in particular milled aluminum is often chosen for consideration of rapid prototype fabrication time, low fabrication cost, weight, stiffness, thermal performance, and bonding strength. This choice gives some mismatch of 'CTE' between the aluminum and most organic substrates. However, it was found that a combination of the use of compliant lid/substrate adhesive and relatively thick lid design provided for outstanding flatness control and high reliability, despite this apparent mismatch. The thin compliant nature of the PTFE-SIP substrate makes it easily controllable.

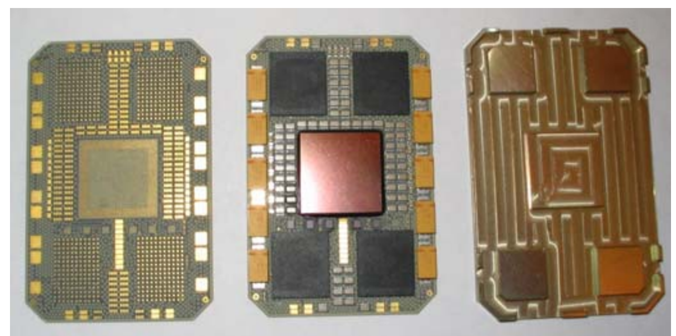

Figure 7, L to R: PTFE-SIP Laminate, PTFE-SIP Laminate with components and it's stepped lid design

(milled lid shown flipped). In this example, the die is underfilled and SRAMs are not underfilled.

This compliant nature of the materials in PTFE-SIP is also a reason why the chip package is very reliable as a multichip substrate carrier; it essentially functions as a thin film, so that actions of one component with the substrate and lid do not disturb or contribute to that of the other components. This stress distribution and mitigation effect is in sharp contrast to the behavior of a stiff, rigid substrate such as ceramic and other versions of organics utilizing stiff laminate material. While a stiff substrate is certainly self-supporting for flatness, it is subject to stress effects relating to distance from neutral point where the effective size is the entire package size as opposed to each component. Because of the high stiffness of ceramic, underfilling a stiff component in effort to obtain stress reduction of component connections is less efficient than when the substrate is compliant. PTFE-SIP laminate, therefore, has a virtually unlimited size constraint upon it and is suitable for very large SIP applications when reliability is a key consideration.

The thermal performance of the PTFE-SIP configuration is outstanding, especially when used in combination with a milled copper lid. It was found that the compliance of the PTFE-SIP substrate allows overall package flatness to be acceptable many lid materials in reasonable thickness (stepped from 3mm to 1mm or less). More importantly, component-to-component height variation can be taken up by substrate bending, so as to get a thin, consistent bondline between each component and the lid. Some height variation of components is always present, due to component manufacturing tolerances and height/tilt of the component solder joint. The ceramic substrate, very stiff and unable to bend without fracturing, requires component to component variation to be taken up in the resulting bondline. This variation provides for reduced thermal performance since the bondline variation would necessarily give a thicker, thermally undesireable result. When only one high power ASIC is present (perhaps with several low-power memory devices) bondline variation over the low power devices is less of a problem than when several high power ASICS are present. In that case, each ASIC demands a thin, uniform bondline for best thermal performance. By using a pressure process after adhesive dispense, each thermally critical component can enjoy a uniform thin bondline to the lid. The slight bending of the substrate does not affect reliability; the solder joints easly absorb the additional coplanarity and the thermal advantage is a better tradeoff for reliability.

Production Volume Process Ramp

Several versions of PTFE-SIP laminate assemblies are in production in small quantities (under 1000/month); the transition to higher volume assembly at EI Technology in Endicott is in progress. In addition, high-speed CNC milling machines appropriate to fabricate corresponding volumes of the lids are also being added to the existing toolset. The successful integration of the various components in this organic high performance PTFE-SIP was designed to be scalable for ensuing high volume production, following prototype evaluation. The coming challenges involving yield management, test and rework process development, and overall process learning are anticipated to drive the next generation of integrated SIP packaging design to even higher levels.

Conclusions

The PTFE-SIP substrate was shown to be successful in densely packed multichip applications. With proper assembly fixture designs and processes, large thin substrates can be loaded with components and used in high performance system-on-package applications.

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