

Assembly Process Development for Chip-Scale and Chip-Size μ BGA™

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Abstract

Chip-scale package families for silicon products as well as miniature discrete surface mount devices can be combined to help the engineer and designer meet the most demanding goals for electronic miniaturization. The significant advantage to employing the miniature chip-scale packaging technology is threefold; higher component density, more efficient assembly automation and enhanced product performance. A primary concern to anyone utilizing a new technology is keeping development costs under control, optimization of existing manufacturing capability and minimizing the time-to-market. This paper will review chip-scale and chip-size package variations, solder alloy options, furnish guidelines for solder stencil development and outline the actual processes used to successfully produce SMT assemblies utilizing CSP technology.

Introduction

To maximize the benefit of chip-scale packaging and surface mount technology, the user must consider efficient and cost effective assembly processing. Many of the products being introduced in a miniature chip-scale package are compatible with existing surface mount assembly processes, however, the contact size and array pitch will vary, accommodating both die size and I/O. Key factors that an engineer should review before developing the product using CSP may include physical features and construction of the device, environmental limitations, suitable substrate materials and a general understanding attachment methodology. IC manufacturers and users choosing a chip-scale device for rigid or flexible circuit applications, should consider the limitations of circuit fabrication capabilities, assembly process compatibility, product reliability and cost.

CSP Packaging Alternatives

In an effort to coordinate device standards activity, the United States standards organization (EIA/JEDEC JC-11) and the Japan counterpart (EIAJ EE-13), meet each year to present work in progress. The meeting is structured to allow open and candid discussion on each organization's proposals and trends in device packaging.

During a recent joint meeting, JEDEC JC-11 and EIAJ member companies presented package outlines for several Thin, Fine-pitch BGA (TFBGA) variations. The device

outlines are similar to a degree, however, some devices are somewhat larger than the silicon die and manufacturing technologies differ a great deal.

General CSP Package Variations

JEDEC documents generally identify only the basic device structure, plastic, ceramic or tape, however, the registered outline MO-195 (currently in process of refinement) does not define the materials or method for manufacturing the device. There are three basic package methodologies in use as well as three variations of base materials used for the devices interposer. Figure 1 details the primary differences between package construction.

The 0.5 mm pitch array device defined in the JEDEC document MO-195 describes a package having a maximum height limit of 1.2 mm, has a nominal contact diameter of 0.3 mm and allows for optional depopulation of contacts within the array matrix. Contact depopulation may include a zone within the array pattern or a selective deletion of contacts to enable efficient conductor routing on the circuit structure.

Standards for CSP

Both JEDEC and EIAJ are developing a fine-pitch BGA Design Guide as well. The documents are still in the development stage but, some aspects have been agreed upon. For example, the contact pitch in the JEDEC guideline has been broadened from the basic 0.50 mm to include 0.65 and 0.80 mm. The document also includes a "low profile" variation as well. The low profile package has a maximum height limit extended to 1.70 mm with the contact diameter increasing as the array pitch spacing expands from 0.50, 0.65, 0.80 mm.

Ball Pitch and Contact Variation for Fine Pitch BGA Packaging

	TFBGA	LFBGA
Contact Pitch	Thin Profile (< 1.20 mm)	Low Profile (1.70 mm max.)
0.50 mm	0.25 - 0.35 mm	0.25 - 0.35 mm
0.65 mm	0.25 - 0.35 mm	0.35 - 0.45 mm
0.75 mm	0.25 - 0.35 mm	0.35 - 0.45 mm
0.80 mm	0.25 - 0.35 mm	0.45 - 0.55 mm

The first chip-scale devices to reach the market as a commodity product are for memory applications typical of those illustrated in Figure 2. 40 I/O BGA device is targeted for the 16M x 8 Flash ROM market and the 46 I/O package for the 4M, 8M and 16M x 8 and

x16 low voltage Flash memory. The 60 and 90 I/O examples are typical of the configurations for SDRAM applications.

The chip-size μ BGA® device shown in Figure 3 features a flexible polyimide base interposer and is the package technology selected to replace the TSOP for Intel's Flash memory product. Unique in its design, the package profiled in Figure 4 utilizes a system of low modulus encapsulation materials, polyimide film and gold plated copper foils for interfacing of the silicon die to the contact array. This package technology has been adapted through licensing agreements by most of the leading IC manufacturers. In addition to Intel's application, T.I, AMD, Hitachi, Siemens, SGS Thompson, Amkor and others (16 in all) have μ BGA devices in development. The primary benefit these companies are able to achieve is a more reliable product (when compared to the alternative CSP configurations).

The μ BGA package technology has the capability to adapt to a variety of die designs (typical of those shown in Figure 5), is manufactured using existing packaging methodology and the μ BGA is supported by a strong and growing supplier infrastructure. For higher performance packaging requirements needing thermal dissipation beyond that possible through the ball contact to a board level thermal plane, the package can be configured with an alloy heat spreader typical of that illustrated in Figure 6 and is typical of the final product shown in Figure 7.

Contact Alloy Options

While the eutectic contact is the primary alloy for contacts on chip-scale BGA devices, other materials have been specified for special applications. The user specifying a solid copper alloy sphere contact, for example, will typically achieve a more uniform standoff height. And, when spheres are attached to the device having a higher melting temperature solder (typical of that illustrated in Figure 8), the package can be socketed without contact deformation.

Another benefit of the solid-core contact is that the device can be de-soldered from a circuit structure without dislodging or damaging the contact sphere.

Assembly Process for Attachment of CSP

Assembly process yield and product reliability are two key issues facing manufacturers of electronic products. Although electronics as a category encompasses a very wide spectrum of packaging technology, solder alloy attachment and interconnecting of the devices with printed circuits continues to be a practical and economical method of assembly.

Solder attachment of the chip-scale BGA device to miniature electronic products typical of that shown in Figure 9, is not unlike the processes already widely used for surface mount and fine-pitch lead-frame package technology. That is, if a company is achieving acceptable assembly yields for SMT, it should not require additional resources to implement CSP technology.

PCB Assembly Compatibility Issues

- CSP must be compatible with standard
- pick-and-place assembly methodology
- Solder attachment processes should be typical of that used for conventional SMT

The process flow shown in Figure 10, employ solder paste stencil printing, device pick-and-place and reflow solder processes. These processes are currently in common use for SQFP and TSOP (< 0.5mm pitch) assembly but, when compared to fine-pitch QFP and TSOP, users are actually reporting fewer solder process defects on the chip scale BGA device package.

CSP Solder Attachment

Although a tin/lead eutectic alloy is very common material for sphere type contacts, other alloys are available and may be considered for package interface. Tin/lead solder is favored for attachment applications because of its compatibility with eutectic alloy spheres, but the softer alloys will collapse to a degree during the reflow soldering process.

SMT Process Planning

The efficient utilization of assembly equipment and human resources is paramount in controlling manufacturing costs. Circuit board assemblies have become more complex as one may observe. It is not unusual for both sides of the circuit structure to be equal in component density.

The PCMCIA shown in Figure 11 is an example of a two sided assembly utilizing a single process line by alternating side one and two within the four unit panel. Although two passes through the line is necessary, the machine utilization is most efficient (See Figure 12).

Ball and Attachment Alloy

A majority of devices using the ball array contact adapt an alloy that is compatible with eutectic solder attachment processes. 63/37 eutectic solder for example, converts to a liquid condition between 179 and 183° C, the surface temperature must rise to 210-220° C for 30 to 60 seconds, expelling the flux and completing the attachment sequence.

Both sphere and attachment alloy composition will impact assembly process profile.

Although those materials noted may be more common, other alloys may be considered for μ BGA contact and attachment interface.

Solder Alloy Considerations

Alloy	Liquidus Temp.*
63Sn/37Pb (Tin/Lead)	183°C
62Sn/36Pb/2Ag (Tin/Lead/Silver)	179°C
62Sn/36Pb/2In (Tin/Lead/Indium)	179°C
95.5Sn/3.5Ag (Tin/Silver)	221°C
95Sn/3.5Ag/1.5In (Tin/Silver/Indium)	218°C
25In/75Pb (Indium/Lead)	264°C
10Sn/90Pb (Tin/Lead)	325°C

* Solder alloy is typically heated 30-50°C above the rated liquidus temp. of the material to complete the wetting characteristic needed for joining.

One may consider an alternative contact alloy that will retain its shape after attachment. For example, the higher melting or liquidus point of the lead dominant alloys will not collapse when exposed to normal reflow temperature (210-220° C).

A solid-core alloy can be adapted for interfacing as well, but most of these materials require a secondary plating over the basic alloy to retard oxidation and promote wetting of the solder.

Assembly for the chip-scale package should not require specialized equipment or processes beyond that currently in use for other surface mount device attachment. Most important, the stencil-printing process must provide uniform and consistent solder paste application. This together with strict process monitoring can control and maintain solder quality on the device. Overall, the defect ratio for array contact package attachment is only a fraction of that experienced using fine-pitch leaded devices.

Stencil fixtures for the fine-pitch BGA retain many of the features and techniques employed for general surface mount applications. In fact, although miniature array devices can be adapted for both high and moderate I/O applications, many assemblies may include a mix of chip-scale and leaded fine-pitch devices.

Solder Stencil Development for CSP

Unlike the narrow rectangular land pattern geometry typical for attaching the leaded QFP while the contact sites for BGA devices are circular or square. Land pattern geometry recommended for chip-scale array device attachment is 0.25 to 0.30 mm (.010" to .012"). The stencil opening can be equal in size to the diameter of the land pattern or square and slightly larger as detailed in Figure 13, to meet specific requirements. To achieve a more robust solder connection, process engineers may specify an expanded stencil opening as shown in Figure 14 to furnish a higher solder paste volume at each attachment site as compared in Figure 15.

Defining Stencil Aperture and Geometry

Changing the shape of the openings from round to square has proved beneficial for CSP applications.

Although the fine-pitch CSP land pattern is generally a circular shape matching the ball contact size, stencil openings that have a square geometry furnish better solder printing quality. The square stencil pattern can serve two purposes. It can increase the solder volume slightly and when adapting the smaller pitch CSP and, the square pattern promotes a more uniform release of the solder paste from the stencil surface.

Another technique that has improved paste transfer on the smaller land geometry's is the tapered land pattern opening. The tapered wall is formed by chemical etching or with a laser. During stencil fabrication, the opening that will be closest to the board surface is made one or two mils wider than the opening at the top surface as illustrated in Figure 16.

The square stencil pattern serves two purposes:

1. It can increase the solder volume slightly when adapting the smaller pitch CSP
2. The square trapezoidal pattern releases paste from the stencil surface more uniformly.

CSP Device Placement

Placement of the chip-scale or chip-size device should be accurate within 0.1 mm (.004"). Even though perfect placement is desirable, the array device, because of the surface tension created when the solder is in a liquidus form, will self align during the reflow solder process.

Solder Process Description for CSP Program A:

- 188 I/O μ BGA w/ .020" pitch
- Printer Type: Fuji w/ vision alignment
- Solder Paste/Supplier: Kester R244
- Particle Size: Type 4
- Flux Type: Low Solids RMA (no clean)
- Viscosity: 900-1000 kcps (cartridge)
- Stencil Thickness: .006" stainless
- Aperture Size: .012" sq. (chem etched)
- Aperture Shape: Square w/ .006" R corners
- Trapezoidal: .001" taper
- Reflow Type: Convection
- Oven Supplier: ABW
- Max. Surface Temp: 210°- 220°C
- Duration Above Liquid: 60 sec. max.

During process development, the finished condition of the solder connections under the array device may be of some concern. Product liability and reliability are key issues that must be confirmed using industry recognized methods.

Reflow Solder Processing

Forced air/gas convection soldering has proven advantages for reflow solder processing of the Chip-scale or chip-sized BGA package. The profile shown in Figure 17 represents temperature levels targeted for a multiple-zone forced (hot air/gas) convection process. The peak reflow temperature and dwell time at liquidus is a critical factor. When using the eutectic 63Sn/37Pb solder alloy for example, the paste material will convert to a liquid at 183° C however, the temperature must continue to rise an additional 30-50° C to ensure that wetting takes place between device and mounting structure.

Please note:

The dwell time above the liquidus point, may extend to 60 seconds to insure that all the flux materials separate from the alloy mass.

- Solder Process Description for CSP Program B:
- 46 I/O μ BGA w/ 0.75 mm pitch
- Printer Type: MPM
- Solder Print Inspection Cyberoptics in-line LSM
- Solder Paste/Supplier: Kester R244
- Particle Size: Type 3
- Flux Type: Low Solids RMA (no clean)
- Viscosity: 900-1000 kcps
- Stencil Thickness: .006" stainless
- Aperture Size: .014" (laser cut)
- Aperture Shape: Round
- Trapezoidal: .001" taper
- Reflow Type: Convection
- Oven Supplier: Vitronics
- Max. Surface Temp: 210° - 220°C
- Duration Above Liquid: 60 sec. max.

Actual measurement and profile or shape of the solder joint can be made with destructive as well as nondestructive techniques. The destructive process requires a cross-section typical of that furnished in Figure 18 that allows the inspection of the device through the solder joint. Other nondestructive methods for solder inspection may be more practical after a product is in production. Although useful during product development, x-ray inspection of critical segments of the assembly have proved to be very efficient for monitoring the processes.

What has proved to be most beneficial for solder process quality and uniformity control is inspection of the solder paste printing before attaching the CSP device. Unlike gull wing lead devices, solder rework is not practical and removal of the device is typically the only way to correct serious solder defects. Inspection of the solder printing should include measurement of both thickness and coverage. The final proof of process may require

physical stress testing. Depending on the products use category, various methods of temperature cycling can be utilized to prove that the product can meet required operating conditions and life expectancy.

General Comments:

Assembly Process:

Reflow profile for CSP is typical of that used for lead-frame type fine-pitch SMT device assembly.

Devices that appear to be misaligned will self align during reflow and should not be adjusted by hand.

Need to develop high density probe methods because conventional spring-contact probing is difficult.

Summary

Chip-scale device standards will continue to evolve as more companies enter this lucrative market. The market driver is the manufacturer attempting to gain customer favor by providing better performance, smaller size and reliable operation at a reasonable (competitive) cost. The variations of contact pitch, ball diameter and package outlines will eventually be minimized. One issue has been resolved without reservation, assembly processes for attaching the devices has proved to be repeatable and predictable for low and high volume manufacturing. More assembly service companies and product developers are successfully utilizing CSP for efficient automated SMT assembly, and many have found that when the devices are furnished in tape-and-reel packaging, machine utilization can be further enhanced.

Assembly using CSP devices is not unlike the processes already widely used for surface mount and fine-pitch technology.

If a company is achieving acceptable assembly yields for SMT, it should not require additional resources or new methodology to implement chip-scale or chip-size BGA technology.

Chip-scale and chip-size packaging is not a futuristic concept. Devices are currently being distributed and used in a wide variety of portable and hand-held products and as more silicon is made available in the miniature BGA configuration, the main stream of the industry will also embrace this technology ...another step in the evolution (or revolution) of electronic packaging.

Authorized (licensed) μ BGA™ Device and Package Service Providers

- Intel
- Texas Instruments
- SGS Thomson
- Hitachi Ltd.
- LG Semicon
- Samsung
- Sony

- Hitachi Cable *
- Hyundai (ChipPac) *
- Amkor-Anam *
- Mitsui Hightec *
- Shinko *
- AMD
- Siemens
- ASE *

* Companies providing packaging services

Biography

Vern Solberg is the Director of Advanced Manufacturing Technology with Tessera in San Jose California. Mr. Solberg is a member of IPC, IMAPS (ISHM/IEPS), and SMTA, focusing on product "Design for Manufacturing". His primary activity is related to application engineering and assembly process development, serving as a technical advisor to in-house as well as customer engineers and design specialists.

Current activity includes:

Author of "Design Guidelines for Surface Mount Technology" published by McGraw-Hill of New York, Chairman/Secretary for IEC-TC91/WG2, International Standards for SMT Assembly Processes, Chairman for the ANSI/IPC-SM-782, SMT Design and Land Pattern Standards Task Group, Editorial Advisory Board Member for "Surface Mount Technology Magazine" and "Chip Scale Review Magazine", USA. based trade publications, Member of the Surface Mount Council (SMC), Member of EIA JEDEC JC-11, Committee for Device Outline Registration and Standards.

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