Board-Level Thermal Cycling and Drop-Test Reliability of Large, Ultrathin Glass BGA Packages for Smart Mobile Applications

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***Abstract*— Glass substrates are emerging as a key alternative to silicon and conventional organic substrates for high-density and high-performance systems due to their outstanding dimensional stability, enabling sub-5-μm lithographic design rules, excellent electrical performance, and unique mechanical properties, key in achieving board-level reliability at body sizes larger than 15 × 15 mm^2. This paper describes the first demonstration of the board-level reliability of such large, ultrathin glass ball grid array (BGA) packages directly mounted onto a system board, considering both their thermal cycling and drop-test performances. To investigate board-level reliability, glass BGA packages, 18.5 × 18.5 mm^2 in body size and 100 μm in thickness, were first designed and fabricated with a daisy-chain pattern. The glass test vehicles were fabricated at panel level, and then BGA balled by ball drop process with SAC105 solder balls, 250 μm in diameter at 400-μm pitch. After singulation, the glass packages were mounted onto printed circuit boards using standard surface mount technology assembly processes, and then subjected to reliability testing through thermal cycling and drop tests following JEDEC reliability standards. The effect of the coefficient of thermal expansion (CTE) of glass was evaluated by investigating low- and high-CTE glass substrates, with the CTEs of 3.8 and 9.8 ppm/°C, respectively. While all glass packages passed 1000 thermal cycles at −40/125 °C as predicted by thermomechanical modeling using the Engelmaier–Wild model, the fatigue life of high-CTE samples exceeded 5000 thermal cycles. In addition, 28/30 drop-test samples passed the required 40 and 200 drops on corner and inner circuits, respectively, with no clear effect of the glass CTE. The predominant failure modes were systematically identified for both reliability tests.**

***Index Terms*— Drop testing, glass package, thermal cycling.**

I. Introduction

EMERGING mobile applications with increasing demands in miniaturization, I/O density, and bandwidth at reduced power and low cost are driving the need for a new class of ultrathin, high-stiffness substrate technologies, enabling higher system integration densities in advanced package architectures. Low-coefficient-of-thermal-expansion (CTE) organic packages and silicon interposers have been proposed to address these challenges, with silicon-matching CTEs to extend chip-level reliability to die sizes exceeding 100 mm^2 and reduced I/O pitches of 40 μm and below. However, such substrates face critical reliability concerns at board level due to: 1) the large CTE mismatch with the organic board; 2) the recent trend toward ball grid array (BGA) pitch scaling below 400 μm; and 3) aggravated warpage with reduced substrate thickness and increased size up to 20 × 20 mm^2, degrading both assembly yield and fatigue life of traditional solders. The use of underfills, conventional at chip level, is moreover undesirable at board level to preserve reworkability. Extensive research has been carried out to solve this complex board-level reliability challenge with minimum system-level impact by bringing innovations in solder materials and new compliant interconnection structures.

Drop test and thermal cycling reliability, equally critical in mobile applications, require contrasting solder material properties. While soft solders with low Ag content are better suited for drop test due to their lower modulus, yield strength, and ability to absorb shock energy, hard solders with high Ag content are beneficial for thermomechanical reliability due to their higher yield strength, hence their ability to prevent plastic deformation [1]. Indium has developed a Mn-doped SAC solder alloy, SACm (SACm0510), addressing this challenge by fine control of the interfacial reaction and intermetallic (IMC) formation, but its current availability in paste form only limits its BGA pitch scaling capability to 500 μm [2], [3]. Various compliant interconnections have also been demonstrated in the last decade, including multipath fan-shaped interconnects [4], G-Helix [5], copper microwire interconnects [6], and bump-on-polymer structures [7]. In addition, reinforced polymer collars developed by Kulicke and Soffa [8] as a wafer-level packaging technology indicated 30%–50% improvement in thermal cycling reliability [8]. However, the drop-test performance has yet to be demonstrated with these approaches, and their adoption in surface mount technology (SMT) high-volume manufacturing has been so far limited. The most common solution to achieve system-level reliability currently consists in introducing an additional package level between the low-CTE substrate and motherboard, which inherently adds to the system thickness and cost. A direct package-to-

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board SMT solution meeting thermal cycling and drop-test performance requirements at system level, without the need of an intermediate package level, is thus highly sought after.

Glass is emerging as a key substrate material for smart mobile applications due to its high dimensional stability, better electrical performance, and low insertion losses compared to silicon, large-panel processability for a similar cost than organic substrates, and ability to form high-density copper-plated through vias [9]. However, no through silicon or glass vias are present in this paper. Furthermore, with its high elastic modulus, glass transition temperature (T_g), and tunable CTE in the 3.8–9.8 ppm/°C range, glass substrates exhibit better warpage performance than their organic counterparts and unique strain relief for reliability mitigation with minimal additional process steps. Board-level thermal cycling reliability of such glass packages has already been demonstrated at 7.2 × 7.2 mm^2 body size, highlighting the benefits of dielectric strain buffer layers on either side of the glass package to enhance thermomechanical reliability. Both low- and high-CTE glass package variations, 3.8–9.8 ppm/K, showed better reliability than silicon interposers of the size, undergoing up to 1500 thermal cycles [6].

This paper evaluates the extendibility of glass BGA packages to larger package sizes, up to 18.5 × 18.5 mm^2, demonstrating for the first time balanced drop test and fatigue performances, focusing as a key innovation on the effect of glass CTE on warpage and reliability mitigation. Finite-element modeling (FEM) was first conducted to extract the warpage response and fatigue life of the glass BGA packages. A daisy-chain test vehicle was designed for thermal cycling and drop tests. The test vehicles were fabricated at panel level on 100-μm-thick glass substrates and assembled using standard SMT processes. Reliability testing and failure analysis was finally carried out to provide a comprehensive study of large glass BGA packages at board level.

II. Finite-Element Modeling

To analyze the warpage behavior and thermomechanical reliability of glass packages, a 2-D half-symmetry model of a 100-μm-thick glass package was created along the diagonal from the center to the corner. Modeling was performed with ANSYS 16.0. Symmetry boundary conditions were applied to the left boundary of the package, which represented the center of the package, and the bottom corner pinned to prevent any rigid body motion.

A unit section of the modeled FEM structure with 22.5-μm-thick dielectric build-up layers (45 μm in total thickness) on either side of the 100-μm-thick glass package with 12-μm-thick patterned copper (24 μm in total thickness) was assembled with SAC105 solder balls, 250 μm in diameter, on 1-mm-thick printed circuit board (PCB), as shown in Fig. 1.

All package materials, with the exception of copper and solder, were considered elastic and temperature-independent, and were modeled using properties defined in Table I [10]. This assumption was made because the glass [11] and polymer [12] have glass transition temperatures above the simulated temperature range. Plasticity of copper was represented with a bilinear elastic-plastic law with isotropic kinematic hardening using a tangent modulus of 1034 MPa and a yield stress of 172.4 MPa.

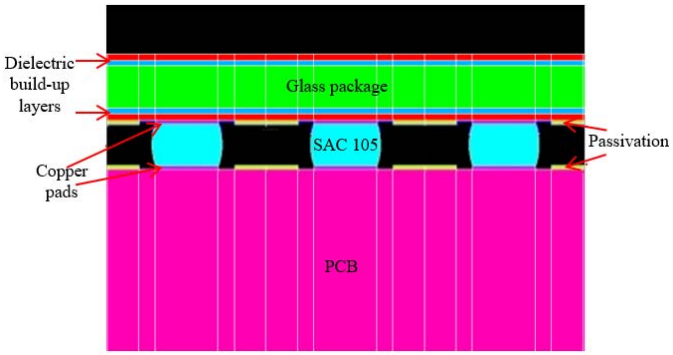

Fig. 1. Unit section of glass BGA package in 2-D half-symmetry FEM structure.

TABLE I
PROPERTIES OF MODELED MATERIALS

Material	Modulus (GPa)	CTE (ppm/°C)	Poisson's Ratio
Low-CTE glass	77	3.8	0.22
High-CTE glass	74	9.8	0.23
ZIF build-up layer	7	21	0.30
Passivation	13.45	4.5	0.30
Copper	121	17.3	0.30
FR-4 (PCB)	24	17	0.30

TABLE II
ANAND'S MODEL PARAMETERS FOR SAC105 SOLDER

Anand's Parameters	Units	Value
A	s^{-1}	5200
Q/R	K	10150
Ξ	-	6.0
M	-	0.18
S	MPa	30
N	-	0.008
h_0	MPa	34000
A	-	1.62
s_0	MPa	23

The SAC105 solder was modeled as a viscoplastic material with Anand's unified constitutive law, capturing time-independent plasticity and creep of the solder. Anand's model parameters for SAC105 are given in Table II [13].

Thermomechanical loads were then applied to the package assemblies to estimate the fatigue life of the solder joints and provide design guidelines for reliability. The modeled structure was first subjected to a drop in temperature from 260 °C to 25 °C to simulate the cool-down phase of the SMT reflow process. Five thermal cycles between −40 °C and 125 °C (following the JESD22-A106B thermal shock standard) were applied. The ramp-up and ramp-down times were 1 min each, and the dwell time at the temperature extremes was 5 min. These times are less than the experiments for computational speed and were not observed to significantly affect the predicted fatigue lives.

TABLE III
FATIGUE LIFE PREDICTIONS USING COFFIN–MANSON MODEL

Package Material	Plastic Strain Range	N_f (Cycles to failure)
Low-CTE Glass	1.45 x 10^{-2}	702
High-CTE Glass	0.78 x 10^{-2}	2204

TABLE IV
MATERIAL CONSTANTS FOR SAC105 [15]

Solder	ε_f	c_0	c_1	c_2	t_0
SAC105	0.225	.480	9.3e-4	-1.92e-2	500

During SMT assembly, mechanical coupling between package and board is established as the solder solidifies and forms interconnections. Therefore, the stress-free temperature was assumed to be 170 °C, which approximates the temperature at which the solder solidifies enough to mechanically couple the package together. The mismatch in CTE between the package and the organic PCB induces warpage and plastic strains in solder joints upon temperature excursion, eventually leading to failure. The equivalent plastic strain range in the furthest solder joint was extracted from the fifth cycle and used to predict the fatigue life of the SAC105 solder.

Two models based on plastic strain range per thermal loading cycle as a damage metric were explored to predict the fatigue life. The first model was the following popular Coffin–Manson equation [14], which is an empirical fit to determine low-cycle fatigue life (<10 000 thermal cycles):

$$N_f = \left(\frac{\theta}{\Delta\gamma_p}\right)^{1/a} \tag{1}$$

where N_f represents the number of cycles to failure, a is the fatigue strength exponent assumed to be 0.5413 from the literature [15], θ is the fatigue ductility coefficient assumed to be 0.2516 [15], and $\Delta\gamma_p$ is the plastic strain range. Table III shows the predicted cycles to failure.

The following Engelmaier–Wild fatigue model was the second model and included cyclic frequency and temperature effects [16]:

$$N_f = 0.5 \times \left(\frac{2\Delta\varepsilon_f}{\Delta\varepsilon_p}\right)^{1/c} \tag{2}$$

$$\frac{1}{c} = c_0 + c_1 T_{SJ} + c_2 * \ln\left(1 + \frac{t_0}{t_d}\right) \tag{3}$$

where $\Delta\varepsilon_f$ is the fatigue ductility coefficient, $\Delta\varepsilon_p$ is the strain range amplitude, c is the fatigue strength exponent, c_0, c_1, c_2, and t_0 are solder specific constants with experimentally determined values, T_{SJ} is the mean cyclic thermal solder-joint temperature (42.5 °C), and t_d is half-cycle dwell time in minutes (15 min). According to [17], the parameters for the solder-creep fatigue model for SAC105 solder are shown in Table IV.

From above-mentioned calculations, the fatigue strength exponent, $c = 0.4516$, is obtained, yielding the fatigue life as shown in Table V. Based on predictions from this model, both low- and high-CTE package configurations are expected to survive at least 1000 thermal cycles, satisfying Joint Electron Devices Engineering Council (JEDEC) reliability standards.

TABLE V
FATIGUE LIFE PREDICTIONS USING ENGELMAIER–WILD MODEL

Package Material	N_f (Cycles to failure)
Low-CTE Glass	1007
High-CTE Glass	3969

TABLE VI
PARAMETERS AND MATERIAL DESCRIPTION FOR FABRICATION OF GLASS BGA PACKAGES

Parameter	Material Description
Substrate Core	Low- & high-CTE glass (Asahi EN-A1 & CF-XX)
Core Thickness	100 µm
Build-up Layers	ZIF 22.5 µm ZIF 22.5 µm
Solder Resist	ZIF 22.5 µm – SMD design
Metal Layers	BGA daisy-chain pattern with 25% Cu coverage
Cu Surface	Bondfilm – 10 µm Cu thickness
Surface Finish	ENEPIG (Atotech Germany)
BGA Balling and Dicing	250 µm SAC105 BGA (Nanium)

III. TEST VEHICLE FABRICATION AND ASSEMBLY

A. Glass Package Fabrication

Daisy-chain glass package test vehicles with a body size of 18.5 × 18.5 mm^2 were designed and fabricated. Table VI summarizes the stack-up material specifications. Both low- and high-CTE 100-μm-thick panels were fabricated using glass substrates from Asahi glass with the process flow described in [10]. Two dielectric build-up layers 22.5 μm in thickness were first laminated on either side of the 6 × 6-in^2 bare glass panels. Patterned daisy-chain routing was then formed by double-sided Cu electrolytic plating. Solder mask defined (SMD) pads were created by laminating an additional dielectric layer of over the bond pads and creating the openings to the copper pads by laser drilling. Standard ENEPIG surface finish was plated on the copper pads by Atotech GmbH with an industry-controlled process. The metalized glass panels were then sent to Nanium for the attachment of 250-μm SAC105 solder BGAs by ball drop, in a 45 × 45 area array configuration at 400-μm pitch, followed by singulation by mechanical blade dicing.

In compliance with JEDEC standards for thermal cycling and drop test, two PCB designs were developed.

B. PCB Design for Thermal Cycling

The BGA area array at 400-μm pitch was divided in a network of daisy chains interconnected between the dogbone structures on both the package and the PCB. The copper pads on the PCB consisted of a one-metal redistribution layer with

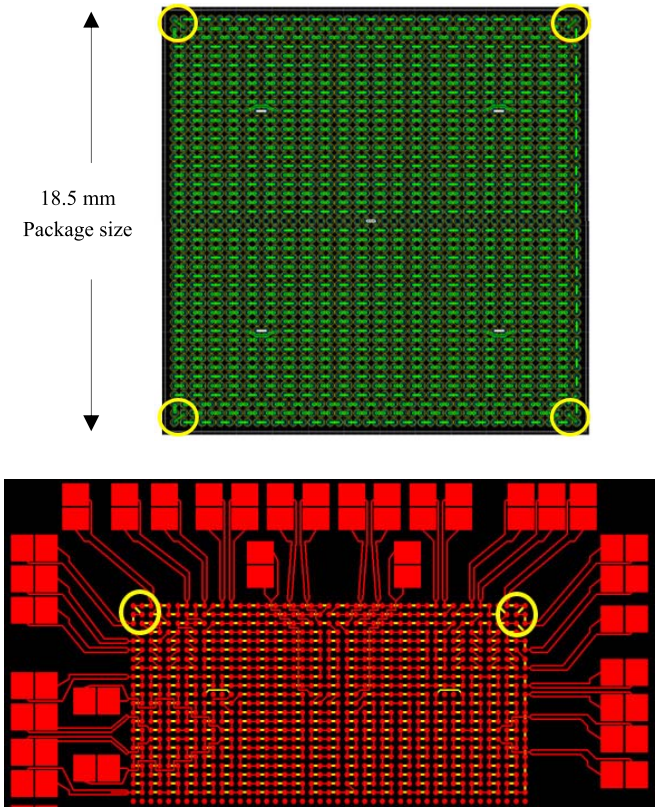

Fig. 2. Dog-bone structures on the package side of the test vehicle (top) and PCB board design with four-point probing pads (bottom).

ENEPIG surface finish and non-SMD passivation. The daisy-chain structures consisted of four corner sides as indicated by the yellow circles in Fig. 2, and 48 inner chains. The corner circuit comprises six BGAs per corner, and the rest of the BGAs belong to the 48 inner circuits.

C. PCB Design for Drop Test

Test boards used to evaluate the drop-test performance of microelectronics packages must be designed following guidelines provided by JEDEC JESD22-B111 standards [18]. However, these recommendations only apply to package sizes up to 15 mm in length or width that is smaller than the body size considered in this paper. Thus, a new design, consistent with the JEDEC JESD22-B111 drop-test boards, was developed and implemented by Qualcomm. Symmetric about the center, four BGA packages were mounted on each board in the suggested configuration, as shown in Fig. 3 [19].

The daisy-chain layout consisted of two daisy chains per sample: one corner daisy chain connecting six power I/Os per corner and one inner daisy chain running through all signal I/Os.

IV. Assembly Process and Yield

A. Precharacterization

The glass BGA packages were selected for reliability testing based on fabrication and balling yield of the substrates. After singulation, optical microscopy, X-ray, and confocal surface acoustic microscopy (C-SAM) inspection were used to inspect for any fabrication related process defects.

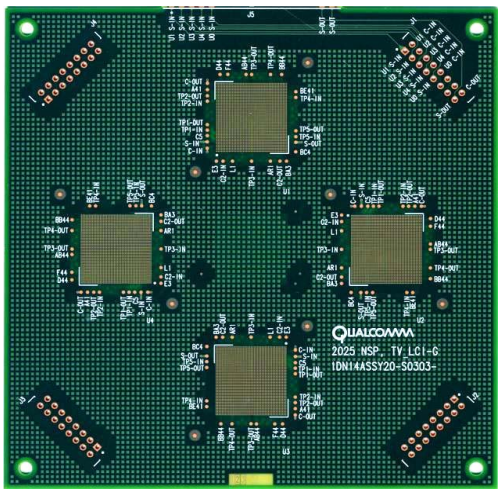

Fig. 3. Drop-test board design for 18.5 mm × 18.5 mm packages [17].

TABLE VII
Yield of SMT Assembly for TCT and Drop Test

Test	Low-CTE Glass (25 samples)	High-CTE Glass (21 samples)
TCT	5/5	5/5
Drop	14/20	16/16

Prior to SMT assembly, the edges of the glass package were coated with a filler-free epoxy-based polymer (provided by Namics Inc.) for edge protection to prevent glass cracking due to distribution layer stresses and dicing-induced defects [20]. Silicon dummy dies, 12 × 12 mm^2 in dimension and 100 μm in thickness, were assembled on the top of the glass BGA packages with capillary underfill. Additional details on the die assembly process can be found in [21].

B. Assembly

The glass packages were then assembled onto dedicated PCBs, for thermal cycling and drop test, respectively, using a Finetech Matrix Fineplacer, using no-clean tacky flux. The reflow conditions were optimized to match the reflow profile of standard SMT processes and minimize BGA voiding. Cross section and scanning electron microscopy/energy dispersive spectroscopy (SEM/EDS) elemental analysis of the joint composition confirmed suitable intermetallic formation.

A total of 46 samples were assembled for thermal cycling and drop tests. For the first time, ultrathin glass packages were successfully assembled in an SMT line.

C. Post-Assembly Evaluation and Yield

After SMT assembly, electrical measurements performed at time t_0 showed that 6 out of 20 parts from the low-CTE drop-test batch did not yield, resulting in a yield of 87%, as reported in Table VII.

X-ray characterization on non-yielded samples showed no major defects. All joints were well formed, with no nonwet/

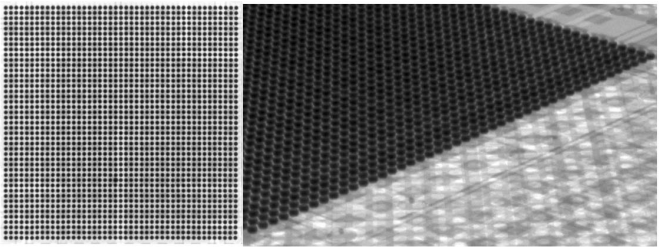

Fig. 4. X-ray characterization of nonyielded drop-test sample.

TABLE VIII
FAILURE DISTRIBUTION ON LOW- AND HIGH-CTE SAMPLES

Failed Sample#	Corner chains	Inner chains	Failed @
Low-CTE #1	3/4	2/46	1100
Low-CTE #2	2/4	1/46	1100
Low-CTE #3	2/4	2/46	1100
Low-CTE #4	1/4	1/46	1200
Low-CTE #5	1/4	0/46	1200
High-CTE #1	4/4	46/46	5300
High-CTE #2	4/4	46/46	5300
High-CTE #3	4/4	46/46	5300
High-CTE #4	4/4	46/46	5300
High-CTE #5	4/4	46/46	5300

unformed solders or head-on-pillow defects as shown in Fig. 4. The yield loss is presumably due to fabrication process defects, such as discontinuities in the routing layers, since the parts were not electrically connected at t_0 despite no major defects observed in Fig. 4 [19].

V. RELIABILITY TESTING—THERMAL CYCLING TEST

A. Procedure and Failure Criteria

Thermal cycling test (TCT) was conducted following JEDEC JESD22-A104D standards, between temperatures of −40 °C and 125 °C with a dwell time of 15 min at each temperature extreme, completing one cycle/hour. The resistance of each daisy chain of the test vehicles was monitored intermittently at room temperature every 100 cycles. The failure criteria were either an increase in the chain resistance by 20% or electrically open daisy chain. These electrical resistance failure criteria are chosen to be strict to account for cracks, which may be open at extreme temperatures.

B. Thermal Cycling Test Results

All sample configurations qualified a minimum of 1000 thermal cycles. However, the high-CTE samples survived more than 5000 cycles, recording stable daisy-chain resistances. Owing to higher CTE mismatch, first failure in low-CTE samples was recorded at 1100 cycles. Table VIII shows the distribution for corner and inner chain failures for low- and high-CTE samples. As expected, the majority of failures affected corner daisy chains, as these chains had the largest distance to neutral point and would experience the greatest damage. As such, the monitoring focused on the most critical solder joints.

TABLE IX
FATIGUE LIFE CALCULATIONS: CORRELATING MODELING PREDICATIONS WITH EXPERIMENTAL DATA

Glass Package	Coffin-Manson	Engelmaier-Wild	Experimental (Mean value)
Low-CTE	702	1007	1140
High-CTE	2204	3969	5300

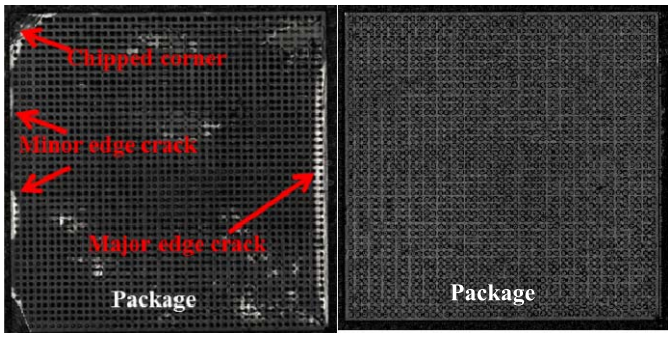

Fig. 5. C-SAM with reference sample (left) with defects, in comparison to a failed low-CTE sample after 1400 cycles (right).

C. Model-to-Experiment Correlation

Based on the fatigue life calculations summarized in Table IX, the experimental results indicate a close correlation with Engelmaier–Wild model in comparison to the Coffin–Manson model. Although only board-level reliability is considered in this paper, the glass CTE can be further optimized and fine-tuned for a chip-package-board configuration, to balance both chip- and board-level reliability.

D. Failure Analysis of TCT Samples

Failure analysis of the TCT samples was performed with three characterization methods: 1) C-SAM to examine the structural integrity of the glass package; 2) optical microscopy on cross sections of failed interconnections to determine the predominant failure modes; and 3) SEM/EDS characterization to investigate and conclude on the failure mechanisms.

1) C-SAM Characterization: C-SAM was performed on the failed parts to inspect the integrity of glass and confirm that no glass-related failures occurred during thermal cycling. No delamination, chipping, or edge cracking of the glass substrates were identified, as shown in Fig. 5.

2) Optical Inspection: To identify the predominant failure modes, the samples were underfilled to prevent any solder smearing during polishing and molded in epoxy resin for cross-sectioning. All samples exhibited similar failure behaviors, as shown in Fig. 6, with fatigue cracks originating close to the intermetallics-to-solder interface on the glass package side and propagated into the bulk of the solder.

No cracks were observed on the PCB side. Furthermore, these results confirm the modeling predictions with higher plastic strain concentrations found at the BGA corners situated

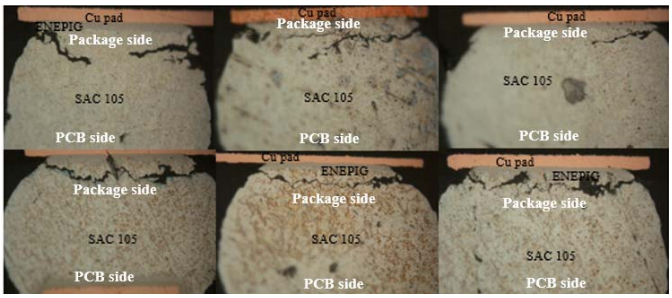

Fig. 6. Failure mode at the top of the solder ball in low-CTE samples.

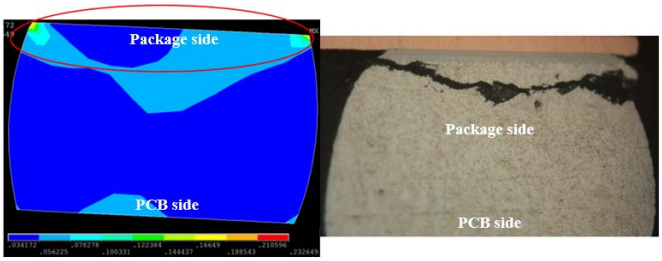

Fig. 7. Plastic strain distribution versus crack location in failed low-CTE sample.

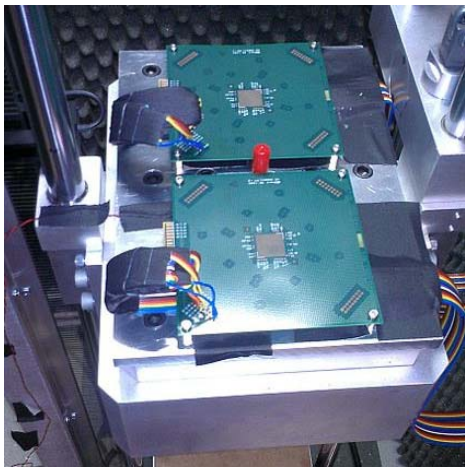

Fig. 8. Drop-test boards mounted onto the shock machine, wired for *in situ* resistance monitoring.

on the glass package side. High strain concentration was observed on the package side where all the solder cracks were located, as shown in Fig. 7.

VI. Reliability Testing—Drop Test

A. Drop-Test Procedure

Drop testing was performed consistent to JEDEC JESD22-B111 standards using Lansmont shock test equipment. With the components facing down, the drop-test boards were mounted to the shock table, as shown in Fig. 8 [19]. The test boards were subjected to a 1500-G, 0.5-ms duration shock pulse. Testing was carried out until 200 drops, for each sample, and the resistance of the corner and inner daisy chains was monitored *in situ* at a rate of 250 kHz. In compliance with JEDEC, failures were defined as the instances of discontinuity, which were verified by at least more instances in the next five drops. For verification, all samples were manually probed again to confirm the fails recorded *in situ*.

TABLE X
Summary of Drop-Test Results

Sample/ Glass CTE	Corner Circuit				
	# of Fails	1st Fail Cycle #	Nominal 5% Fail	B	η
Low CTE	8/15	24	23	1.456	179
High CTE	7/16	6	10	0.705	558
Sample/ Variable	Signal Circuit				
	# of Fails	1st Fail Cycle #	Nominal 5% Fail	B	η
Low CTE	0/13	--	--	--	--
High CTE	0/16	--	--	--	--

Pass Marginal Fail

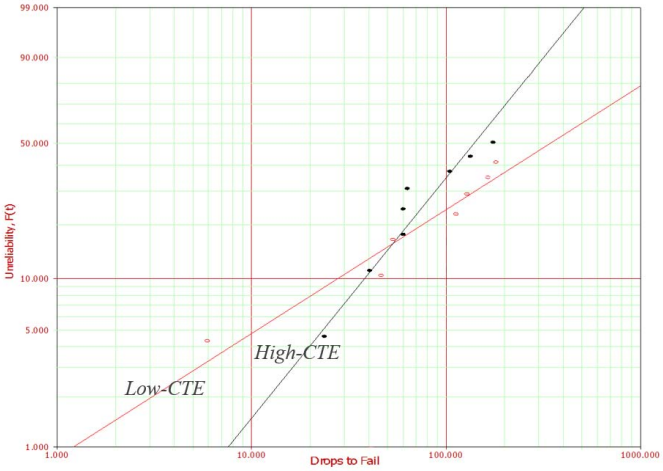

Fig. 9. Weibull failure distribution plot for drop testing of corner circuits.

B. Drop-Test Results

A total of eight boards were placed in drop testing with up to four low- or high-CTE samples mounted on each board. Daisy-chain resistances were measured by the data acquisition system during each drop cycle.

Daisy-chain failure criteria were established based on the following three conditions: 1) a 20% increase in daisy-chain resistance; 2) corner circuit to sustain at least 40 drops; and 3) inner circuit to survive at least 200 drops.

The drop-test results for the corner and signal circuits are compiled in Table X [19]. On the corner circuit, marginal failures were observed on both low- and high-CTE samples. Approximately 50% of the corner nets failed before 200 drops across all samples. Furthermore, no failures on the signal circuit were detected. High-CTE samples appear to have three failure distributions: A fail at six drops is likely due to a latent processing defect, and failures at 47 and 54 drops are 50% lifetime of the next distribution, which fails past 100-drop cycles.

Weibull failure distributions, as shown in Fig. 9, indicate a low Weibull slope (β), suggesting a wide range of variability caused by a yield issue at time t_0, and possibly attributed due

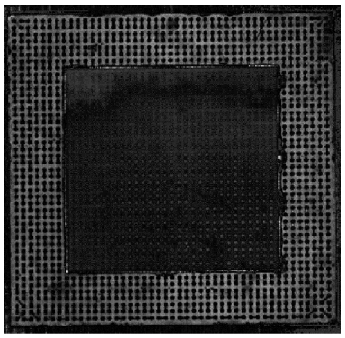

Fig. 10. C-SAM characterization after drop testing on low-CTE sample post 200 drops.

to process defects in substrate fabrication. Moreover, with low number of samples and the wide failure distribution (due in part to outliers), absolute values of unreliability may not be used. Ignoring the outliers with early failure, low- and high-CTE samples exhibit similar failure distributions, indicating that there is a limited effect of the glass CTE on the drop-test performance [19].

C. Failure Analysis of Drop-Test Samples

Failure analysis of the drop-test samples was again performed with three characterization methods: C-SAM, optical, and SEM/EDS to determine the failure mechanisms.

1) C-SAM Characterization: After drop testing, C-SAM inspection (Fig. 10) was performed with a high-resolution 230-MHz transducer. No signs of delamination or cohesive glass cracking could be noticed, despite some minor initial defects being present. This suggests that the polymer applied to protect the glass edges was effective in preventing crack propagation as described in [20].

2) Optical Characterization: On individual BGA rows, it could be observed that defects attenuated moving toward the inner circuit from the corners, which is expected as the solder balls get closer to the neutral point. For all sample configurations, there were two characteristic failure modes described from here on as Mode 1 and Mode 2. Mode 1 failure in the Cu redistribution layer was found most predominant among all sample types, as shown in Fig. 11 [19]. Several other literature studies have indicated Mode 1 failure to be a common failure mechanism for drop-test reliability [22], [23]. A crack in the copper trace is initiated at the point where there is critical stress concentration. In the presence of strong intermetallic adhesion, the failure migrates to the thin copper trace where stress exceeds its ultimate strength [23]. Mode 2 failures occur near the Cu–Ni interface.

Further analysis was carried out with scanning electron microscopy to understand the cause of Mode 1 and Mode 2 failures.

3) SEM/EDS Characterization: Interfacial characterization was first performed to investigate the intermetallics formed between ENEPIG and SAC105. A quantitative analysis of nickel phosphorus layers in the ENEPIG surface finish confirmed the phosphorus content to be in the expected 8%–9% range. Excellent solderability was confirmed with good intermetallic (Ni_3Sn_4) formation achieved during BGA balling as shown in Mode 1 crack in Fig. 12.

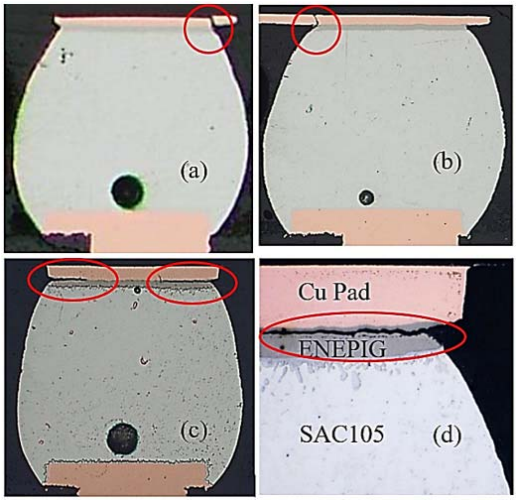

Fig. 11. Optical images of cross sections of failed drop-test samples with (a) and (b) Mode 1 failure: crack in the Cu routing layer and (c) and (d) Mode 2 failures: crack in the Ni layer near the Cu–Ni interface.

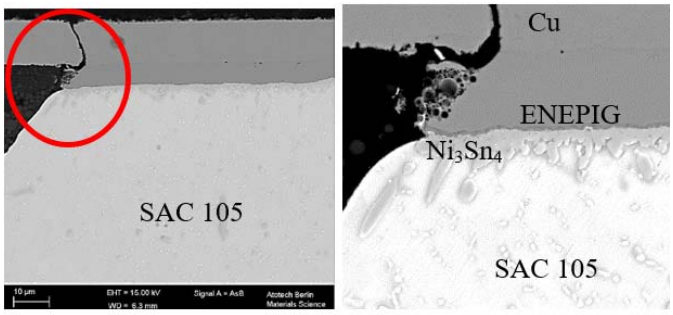

Fig. 12. IMC formation on a BGA with Mode 1 crack.

Mode 2 failures, which are not a standard failure mechanism, were investigated by point scan mappings at central sites away from the crack tip. These scans revealed the presence of small globules and particulates from the passivation at the Ni and Cu pad interfaces, which were entrapped during the fabrication process. The samples with SMD-defined passivation were fabricated by laminating the dielectric film over the Cu pads and laser drilling openings to expose the Cu pad surfaces. Subsequently, plasma cleaning was applied to remove any particulates from the pad surface. Inadequate or ineffective cleaning may have caused dielectric particulates residues on the Cu pads onto which the ENEPIG surface was plated, leading to Mode 2 failures.

VII. Conclusion

This paper reports the first demonstration of balanced drop test and thermomechanical reliability of ultrathin, large glass BGA packages. These BGA packages comprise glass substrates that are directly mounted onto the board, without the need for intermediate packages. This approach, therefore, qualifies as a new major platform for system integration and miniaturization without modification of the processes or the interconnection structure.

During TCT, all samples qualified 1000 JEDEC-based thermal cycles using the SAC105 solder. Low-CTE samples

recorded first failure at 1100 cycles, whereas high-CTE samples passed with stable daisy-chain resistances until 5300 cycles. High-CTE glass, therefore, constitutes a promising platform for the integration of high-performance systems as it can accommodate high-density interconnections to support split dies, while maintaining outstanding board-level reliability. Experimental results achieved indicate excellent correlation with the thermomechanical modeling predictions. However, from a system-level perspective, the TCT reliability can further be optimized to balance both chip- and board-level reliability that will be pursued in the future work at the 3-D Packaging Research Center in the Georgia Institute of Technology. During drop testing, 28/30 samples passed the drop-test failure criteria (corner circuits in samples survived 40 drops and inner chains passed 200 drops). Thus, for drop performance, no clear effect of the glass CTE could be observed. More importantly, no glass-specific failure modes were observed, confirming applicability of glass as a superior substrate material for large, package-to-board integration.

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