Cold Ball Pull Test Efficiency for the PCB Pad Cratering Validation with the Ultra Low Loss Dielectric Material

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Abstract
Cold ball pull testing is used to validate the resistance of PCB pad cratering for the different ultra-low loss dielectrics materials (Dk=3~4.2 and Df <= 0.005 @ 1GHz) in the study. The materials were fabricated in multiple PCB shops using a common test board design utilizing a coupon to result in a 16 mil nominal pad size for the pulls. After fabrication, a 20 mil SAC305 ball is SMT attached to the 16 mil nominal pads for pulling. Each material had 3 coupons with 50 pull locations on each to generate 150 data points for statistical analysis. The peak pull force differences of the material builds can be compared to differentiate the results. As a result, the different ultra-low loss dielectric material's performance to withstand PCB pad cratering can be compared comprehensively with the cold ball pull test.

Keywords: IPC_9708, Pad Cratering, Cold Ball Pull, Ultra Low Loss, Dielectric Material

Introduction
As 4G/LTE cloud computing and evolving 5G are deployed, high performance server, network and telecom products are required to support increasing infrastructure performance demands. As a result, PCB design and performance requirements challenge materials to meet the needs of these applications including: lower and lower Dk and Df, high frequency and high speed for the low signal loss requirements, higher bond strength for the finer pitch BGA devices with smaller diameter pads, as well as the higher Tg for lead free assembly compliance. In addition to the necessary electrical and thermal performance, the more stringent reliability requirements of these infrastructure products must also be taken into account due to the longer term service life of these kinds of end products. Thicker and larger board sizes are usually used for the design of these infrastructure type products. Other factors considered include: higher filler content to reduce moisture uptake and CTE, lower Dk glass with vinyl silane surface treatment compared to E glass, resin chemistry able to adhere with low profile Cu foils and copper bonding treatments, as well as halogen free flame retardants for RoHS green compliance. Combining the above factors when compared with SnPb solder and conventional dicy-cured unfilled FR4 used in the past, the fear was that the newer materials required to support the increased thermal and performance demands would result in higher incidences of PCB pad cratering failures due to larger sized IC packages, smaller pad diameters, more complex stackups etc., or accelerate potential CAF growth and other mechanical and thermal mechanical reliability concerns during PCB assembly specifically at in circuit test (ICT) and other handling phases, shipping and service life[1].

PCB pad cratering was defined in the IPC-9708 as the formation of a cohesive dielectric crack or fracture underneath the pad of a surface mount component, occurring most commonly in BGA and BTC packages under mechanical testing as shown in Figure 1 [1]. The strains and strain rates applied to PCB assemblies during the mechanical bend and shock testing can lead to a variety of failure modes in the vicinity of the solder joints. The prevalence and distribution of these failure modes depends on several factors, including the solder metallurgy used, the package type, construction, component-to-PCB-pad size ratio and PCB materials. Usually, multiple failure modes occur concurrently at different strain and strain rate levels.

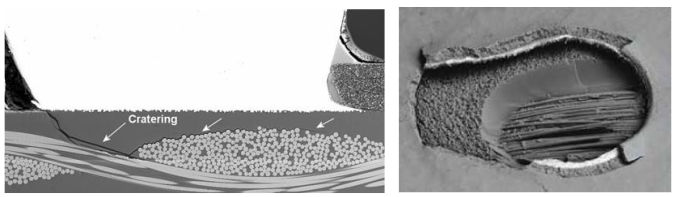


Figure 1 - Example of a Pad Cratering with Cohesive Dielectric Failure Going Down to Glass Fibers [1

The IPC 9708 standard provides some guidance around the different pad cratering failure modes as follows [1]:

Pad Lift (Figure 2): Solder pad lifts with solder ball. The lifted pad may include the ruptured base material. This failure mode is an adhesive failure of the conductor (foil), as opposed to pad cratering, which is a cohesive failure of the dielectric resin.

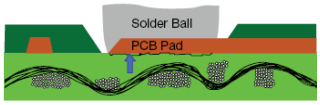


Figure 2 - Pad lift

Conductor cracks (Figure 3): The PCB pad is lifted, but is still partially attached to the conductor, as well as cohesive failure.

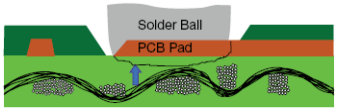


Figure 3 - Conductor cracks

The crater with glass fibers exposed (Figure 4): The PCB pad is cratered, and the underlying glass fibers are exposed, a cohesive failure of the dielectric resin with secondary adhesive failure to the glass fiber reinforcement

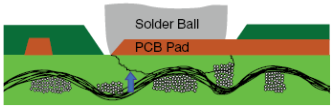


Figure 4 - Crater with glass fibers exposed

The crater with no glass fibers exposed (Figure 5): The PCB pad is cratered, the underlying resin is exposed, but no glass fibers are visible, a cohesive failure of the dielectric resin.

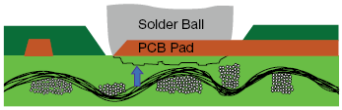


Figure 5 - Crater with no glass fibers exposed

In order to mitigate pad cratering from happening, it is necessary to characterize the resistance of the dielectric materials to mechanical stress. Therefore, various methodologies have been developed for dielectric material characterization such as mechanical bending (monotonic and spherical), AE detection, drop shock, cold ball pull, hot pin pull etc. [2-16]. The first two are related to PCBA level tests while the last two are related to pad level tests. The PCBA level tests will usually generate multiple failure modes concurrently at different strain and strain rate levels making it difficult to decouple the individual failure modes and identify the weakest location in the assembly due to its higher force acceleration and many variables such as solder metallurgy, package type, construction, component to PCB pad size ratio, and PCBA materials etc., which also means the PCBA level test will not be time and cost effective. With pad level tests, it is easier to control the failure mode in the dielectric layer beneath the pad and to define the adhesion between the pad, resin and glass fiber [16]. Between the two pad level tests, the cold ball pull test is more economical than the hot pin pull test because of the materials and time required to conduct the test and collect statistically relevant sample sizes.

Experiment and set up
Test Coupons

Ten dielectric materials were chosen for study by the iNEMI ultra low loss project work group. The materials were selected based on a set of parameter definitions and the material's supplier willingness to participate and provide said materials for testing.

The selection criteria used to narrow the material field were as follows based on suppliers laminate data:

Electrical Targets:

- Dk: 3-4.2 @ 1GHz
- Df : <= 0.005 @ 1GHz

Thermo-Mechanical Targets:

- Tg: >160°C
- Z-CTE: <3.0% from 50°C to 260°C

Construction:

- Capable of multiple dielectric thicknesses from 3 mil to 10 mil
- VLP or HVLP copper for cores
- UL V-0 rating capable

Test Vehicle Design

The project work group decided on a standard stack-up on which the material test vehicle would be designed. The criteria used to construct the stack-up was as follows:

- 22 layers
- Four - 2oz layers in the center of the stack-up
- 150 mils minimum thickness
- Single lamination
- Back drilled electrical structures
- OSP surface finish for reliability test structures
- Spread glass plys (i.e. 1086, 1067, etc.)
- Medium to high resin content for all prepregs

Glass ply type, resin content, and layer thickness were desired to be matched between all stack-ups at four PCB shops (G, T, H, V), however not all material suppliers offered the material in the same glass styles for the desired layer thickness. Stack-ups for each material were modified to provide as close as possible to the nominal stack-up identified by the work group.

Test Method Description:

The test method employed in this study followed the IPC 9708 Cold Ball Pull methodology with the following refinements:

Measured average pad size tested: 16 +/-0.5 mils round
Solder ball size attached: 20 mils
Solder ball composition : SAC405
Solder stencil used to paste pads: Stainless steel 5 mils thick with 20 mil openings
Solder paste used to attach balls: Production SAC305 paste
Peak reflow temperature employed to reflow solder balls to the PCB pads: 245°C minimum.
Test equipment: Production Bond Tester with 5Kg wire pull load cell cartridge
Test Jaw size: 750um
Clamping pressure: 21psi
Test pull speed: 5mm/sec

The coupon design incorporated into the material test panel consisted of two 5x5 round pad arrays for each of five unique pad sizes (14, 15, 16, 17, and 18 mil diameter pads – see Figure 6). The pads in the arrays were spaced at 1mm pitch and NSMD design with a 5 mil solder mask clearance as shown in Figure 7.

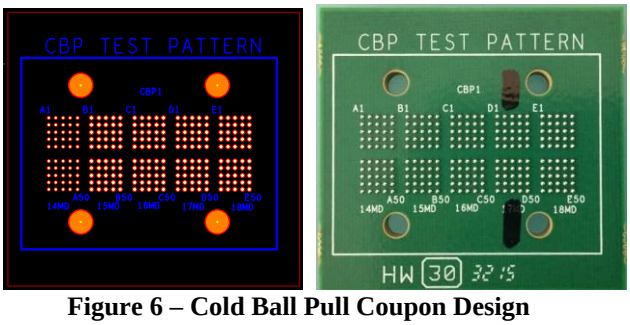


Figure 6 – Cold Ball Pull Coupon Design

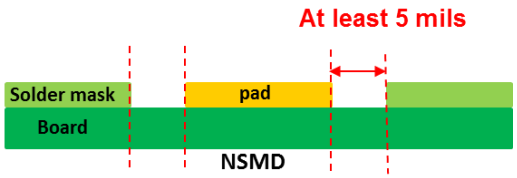
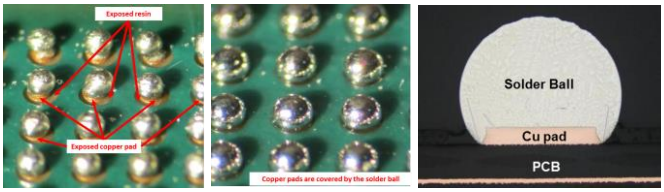


Figure 7 - The design of test coupons

Actual pads sizes for each of the pad groupings were measured by a production co-ordinate measurement machine using optical input and the data averaged for each designed pad size. Solder balls were attached to the pads on each coupon per the conditions stated above. Each sample was inspected at each joint with OM to insure good solder ball attach as shown in Figure 8. Only pads completely covering the copper pads and centered in the NSMD window were considered acceptable



(a) Reject (b) Accept (c) Cross-section joint

Figure 8 -The qualification criteria for the ball attachment

The designed pad arrays which measured closest to 16 mils +/-0.5 on average were chosen to be tested as shown in Table 1. The actual pad size distribution would be up to each PCB shop process control capability such as material and process parameters. The averaged pad size produced by PCB shop V was lower than the 16 mil nominal target and the other PCB shops, which was noted in the comparison of CBP (Cold Ball Pull) strength among all PCB shops. Each material had 3 coupons with 50 pulls on each which generated 150 peak pulls averaged and analyzed by production statistical software. Any missed pulls or sites which did not have an attached solder ball were omitted from the pull data.

Table 1 - PCB pad size selected for CBP test

PCB Supplier	Supplier Material Code	Coupon ID	Avg. Size of Pad (mil)	PCB Supplier	Supplier Material Code	Coupon ID	Avg. Size of Pad (mil)
G	G3	G3-18	15.9974	H	H1	H1-1	16.1813
		G3-5	16.0697			H1-2	16.1440
		G3-7	16.1005			H1-4	16.2365
	GE	GE-16	16.0534		H3	H3-3	16.2135
		GE-2	16.0278			H3-4	16.3765
		GE-3	15.9185			H3-8	16.3462
	GL	GL12	16.1796		H5	H5-5	15.9951
		GL15	16.1356			H5-8	16.0361
		GL16	15.8527			H5-16	15.9453
	GY	GY15	15.9087		HL	HL-14	15.6046
		GY18	15.9886			HL-19	15.9511
		GY9	16.2542			HL-20	15.8537
T	T2	T2-12	16.1495		HW	HW-10	15.8447
		T2-13	16.2180			HW-18	15.8577
		T2-6	15.9129			HW-20	15.8334
	T8	T8-2	16.0088		HY	HY-12	15.7753
		T8-6	15.9781			HY-4	15.8731
		T8-8	15.8365			HY-9	15.8383
	TE	TE-12	16.2122	V	VE	VE-3	14.5598
		TE-2	16.1701			VE-12	14.7232
		TE-3	15.9258			VE-15	14.7579
	TR	TR-2	16.2335		VR	VR-2	13.9114
		TR-5	15.6628			VR-10	13.9253
		TR-9	15.7586			VR-15	13.8564
	TY	TY-10	16.2572		VY	VY-4	14.8740
		TY-15	16.1083			VY-5	14.8332
		TY-2	16.3239			VY-8	15.1471

Result and Discussion

The resulting failure mode after testing can vary based on material, process and design geometry. These failure modes include: bulk solder fracture, interfacial IMC fracture, mixed mode failures and PCB pad cratering, as shown in Figure 9.

In terms of the PCB pad cratering failure mode which is the focus of this study, the failure location can be grouped into 4 categories including: pad lift, conductor crack, cratering with glass fibers exposed and cratering with no glass fibers exposed, as described Figures 2 to 5. The crack itself will follow the path of least resistance to relieve strain and may initiate at the pad edge propagating downward through the resin mass, or beneath the pad nucleating at the interface between resin and glass fibers, or initiating as a pad (conductor) crack propagating into the dielectric layer. The cratering failures might not result in an electrical open but potentially give rise to an electrical failure in subsequent shipping and service life due to continuing crack propagation.

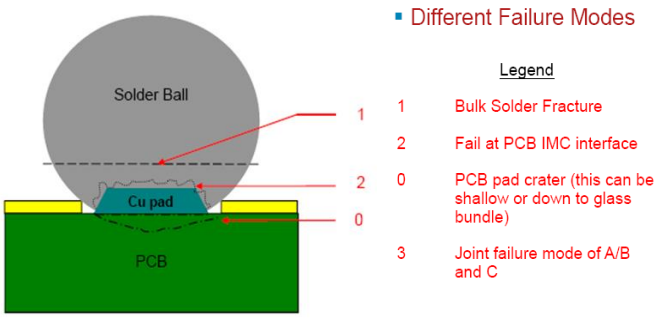


Figure 9- The typical failure mode during CBP test

Based on dielectric material design variables such as resin chemistry, curing agent, glass resin content, filler content and so on, it was not easy to identify which would have the greatest influence on improving fracture resistance to mitigate failure. From the viewpoint of fracture mechanics, the adhesion between different ingredients in the matrix is difficult to be quantified by this test method. The bulk resin material itself can absorb the majority of fracture energy when cracks are initiated and distribution of failure modes by depth of fracture is somewhat random.

Therefore, on the basis of this testing alone we can only conclude that improving the fracture toughness of the bulk resin itself would be the direction to improve performance. Unfortunately, there is no standardized method or requirement for testing fracture toughness for these materials in IPC TM650, so only common mechanical properties such as flexural modulus, flexural strength and peel strength are available for correlation. ASTM test methods for fracture toughness measurement could be referred for further study.

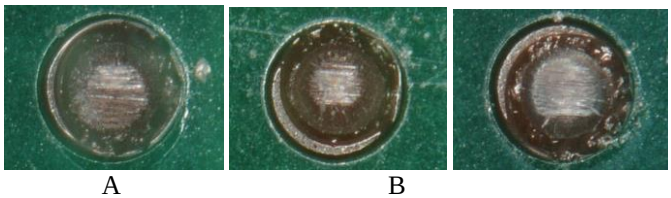
The Cold ball pull (CBP) test was designed to show the fracture strength between the Cu pad and underlying dielectric material by pulling the solder joint vertically from the solder joint above the pad. It was not precise enough to identify crack initiation and propagation separately in the cracking path but could quantify the total energy of the entire fracture process. Figure 11 show the cold ball pull strength comparison among the 10 materials tested from 4 different PCB shops. The process control among the 4 PCB shops is unknown.

PCBs made from the same laminate materials and stack-ups, are still influenced by differences of the PCB shop's process engineering parameters. Average diameters of PCB pads have deviations between lots and between PCB shops, even though the same PCB layout and materials are used. The actual pad sizes are shown in Table 1, where the result of as designed pad sizes range from 16 to 18 mils as shown in Figure 6.

Cold ball pull testing was performed on the coupons from the four PCB shops to compare the adhesion strength of PCB pads to dielectric materials with the pad size closest to 16mil. All failure modes by the test condition are cohesive failures with glass fiber exposed as in Figures 4 and 10, therefore the data is comparable and the strength ranking is listed below grouped by PCB shop

1. G shop：G3>GL>GE>GY
2. H shop：H1>HW>H3>H5>HL>HY
3. V shop：VR>VY>VE
4. T shop：TY>TR>T8>TE>T2

Figure 11 shows the mean diamonds and box plots of the peak pull force values of each material build and the mean and standard deviation statistics. The data shows performance differences for the same material at different fabrication shops, as well as differences in the materials built at the same shop. For example, the performance of material Y is statistically better in shop T than in shop G. Additionally, material 3 is statistically better than material Y in shop G. Uncontrolled process differences between shops in addition to the pad size differences for the V shop builds are the cause for the differences between PCB shops. The ranking within a shop of the different materials built is a good indicator of the laminate's strength for that shop's products.



A B C

Figure 10 - The pad cratering failure mode top view by OM after cold ball pull testing

Conclusions

Cold ball pull testing allows PCB shops to compare which dielectric materials have the best performance to withstand pad cratering based on their process control so as to reduce the field return rate due to pad cratering in PCB assembly and in service life. The comparison of data from different PCB shops is still not suggested due to process deviations at the different shops.

The test method was demonstrated to be reproducible when carefully executed and produced no anomalous results, suggesting it is a good practical test. It was not concluded that the material with certain cold ball pull strength will be capable of withstanding actual PCB pad cratering during shipping and service life of product, but was able to provide differentiation between materials at a single fabricator, thus allowing the end user to select the best candidate material for that PCB shop. The next steps will be to determine peak pull force thresholds at which pad cratering happens when materials are used in real service. Relating this work to results of other methods, such as impact testing, spherical bend testing, DMA, etc. is recommended to accomplish that task. Thresholds are expected to be different depending on product design and fabricator process control.

Acknowledgements

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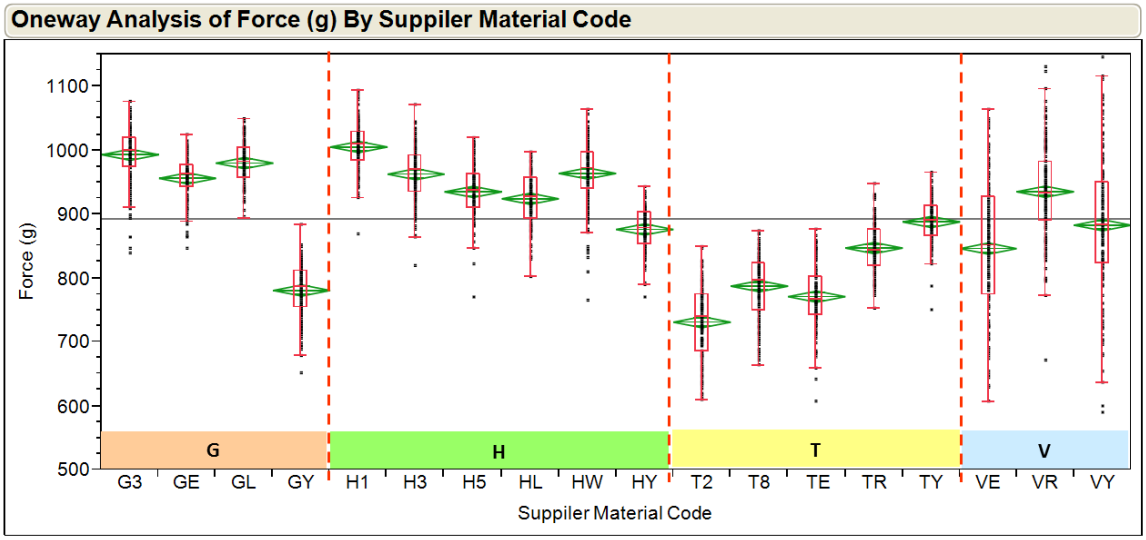

Means and Std Deviations

Level	Number	Mean	Std Dev	Std Err Mean	Lower 95%	Upper 95%
G3	150	993.468	43.3570	3.5401	986.47	1000.5
GE	149	956.482	31.5367	2.5836	951.38	961.6
GL	150	980.370	32.3616	2.6423	975.15	985.6
GY	149	780.930	39.4425	3.2313	774.54	787.3
T2	150	731.295	55.3421	4.5187	722.37	740.2
T8	150	787.651	47.3269	3.8642	780.01	795.3
TE	150	771.238	48.1937	3.9350	763.46	779.0
TR	150	847.340	38.5638	3.1487	841.12	853.6
TY	150	888.232	33.6187	2.7450	882.81	893.7

Means and Std Deviations

Level	Number	Mean	Std Dev	Std Err Mean	Lower 95%	Upper 95%
H1	150	1005.57	37.805	3.0867	999.47	1011.7
H3	149	963.04	42.182	3.4557	956.21	969.9
H5	150	935.34	40.557	3.3115	928.80	941.9
HL	149	924.49	40.490	3.3170	917.94	931.0
HW	150	964.19	48.309	3.9444	956.40	972.0
HY	150	876.45	31.934	2.6074	871.30	881.6
VE	148	846.53	106.539	8.7575	829.22	863.8
VR	150	935.51	70.993	5.7965	924.06	947.0
VY	150	883.16	107.170	8.7504	865.87	900.4

Figure 11 - The adhesion strength of PCB pad to dielectric materials by CBP test

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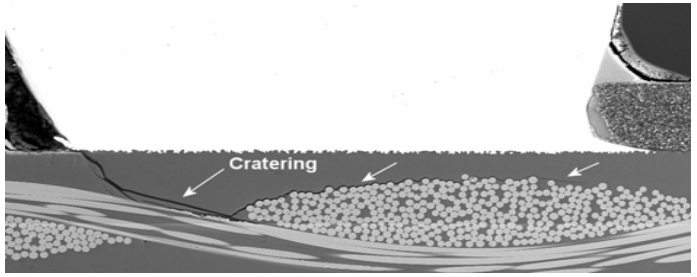
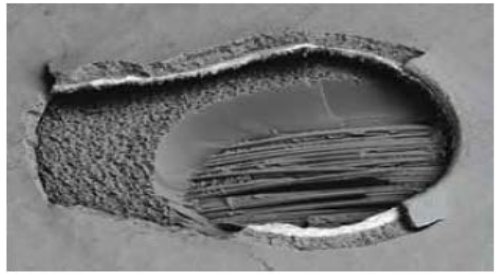
Background for Pad Cratering Issue

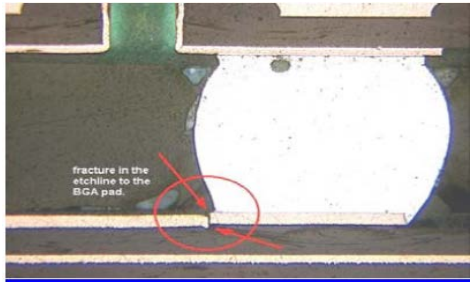
- **Pad Cratering has become the predominant failure mode for Pb-free product during in PCB assembly (in line testing), shipping and its service, especially on larger and thicker board for telcom, server and so on.**
- **Generally, a pad crater is a defect or flaw in the Printed Circuit Board (PCB) exhibited by a mechanical fracture of the solder pad to laminate interface due to thermal or mechanical stresses. especially on the larger BGA and QFN.**
- **The fillers used to make PWBs survive higher reflow temperatures have made them more brittle.**
- **Phenolic" cured resins systems replace "Dicy" cured resins to make PWBs survive Pb-free reflow**
- **High frequency material present lower adhesion with Cu so as to cause high propensity on pad cratering**
- **Need develop efficient methodology to assess dielectrics materials' ability to withstand mechanical forces which can lead to pad cratering, as well to rank order materials subjected to various mechanical stresses.**

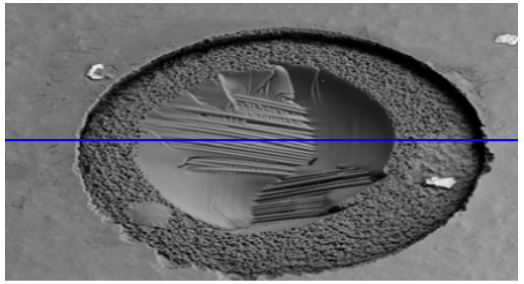
Example of a Pad Cratering with Cohesive Dielectric Failure
-The IPC 9708 standard provides some guidance around the different pad cratering failure modes

	Type		Description
1		Pad lift	Solder pad lifts with solder ball. The lifted pad may include the ruptured base material. This failure mode is an adhesive failure of the conductor (foil), as opposed to pad cratering, which is a cohesive failure of the dielectric resin.
2		Conductor cracks	The PCB pad is lifted, but is still partially attached to the conductor, also adhesive failure.
3		Crater with glass fibers exposed	The PCB pad is cratered, and the underlying glass fibers are exposed, a cohesive failure of the dielectric resin with secondary adhesive failure to the glass fiber reinforcement
4		Crater with no glass fibers exposed	Crater with no Glass Fibers Exposed (Figure 5): The PCB pad is cratered, the underlying resin is exposed, but no glass fibers are visible, a cohesive failure of the dielectric resin.

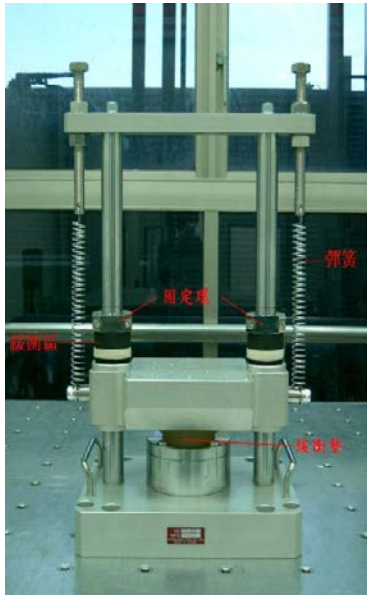


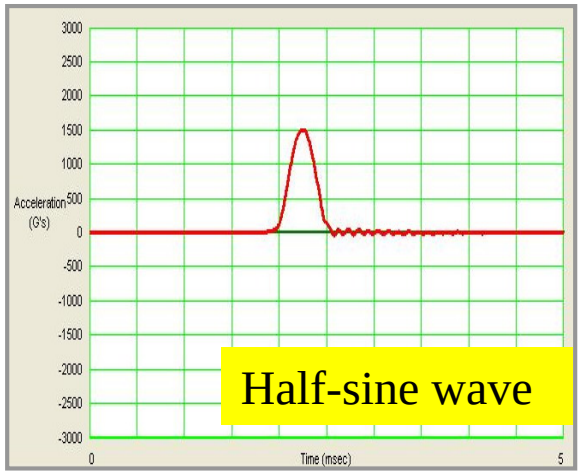


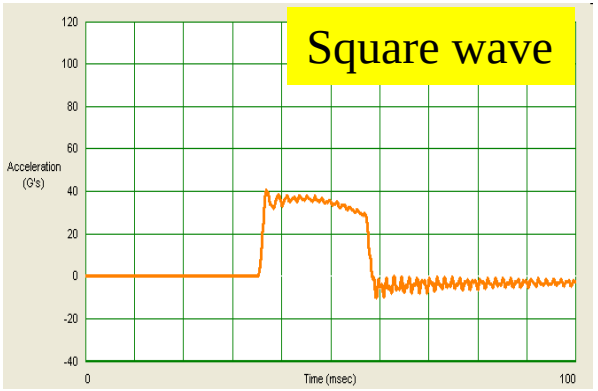




Pad Cratering Test by Mechanical Shock Test/Drop Test at High Strain Rate (IPC9703) (PCBA level)





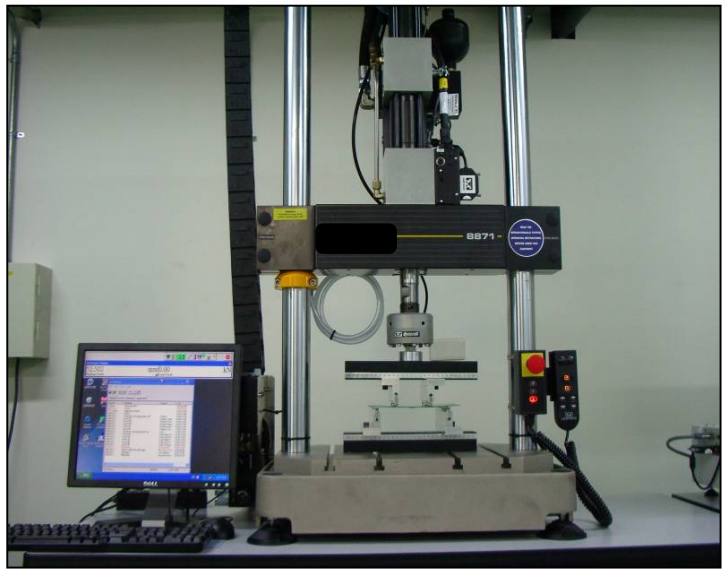


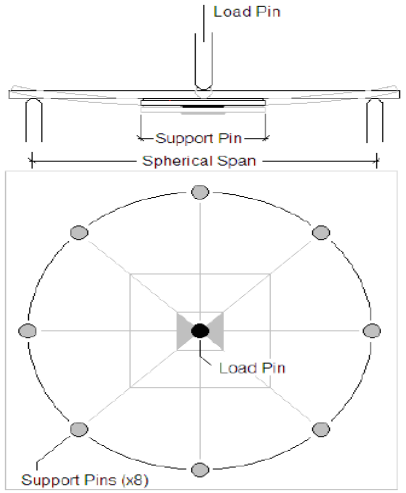
Shock Data Acquisition

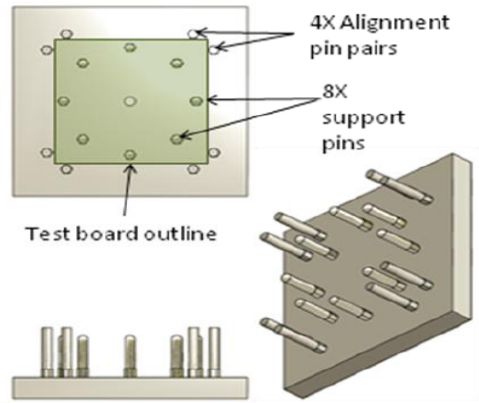
Table 1 — Component Test Levels

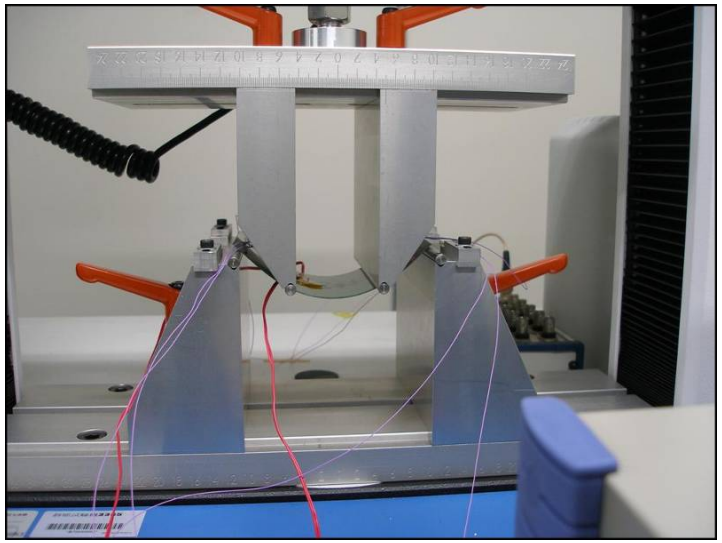
Service Condition	Equivalent Drop Height (inches) / (cm)	Velocity Change (in/s)/ (cm/s)	Acceleration Peak (G)	Pulse Duration (ms)
H	59 / 150	214 / 543	2900	0.3
G	51 / 130	199 / 505	2000	0.4
B	44 / 112	184 / 467	1500	0.5
F	30 / 76.2	152 / 386	900	0.7
A	20 / 50.8	124 / 316	500	1.0
E	13 / 33.0	100 / 254	340	1.2
D	7 / 17.8	73.6 / 187	200	1.5
C	3 / 7.62	48.1 / 122	100	2.0

Pad Cratering Test by Three/Four-point/Spherical Bending Test to Fail (IPC9702 and 9707) (PCBA level)

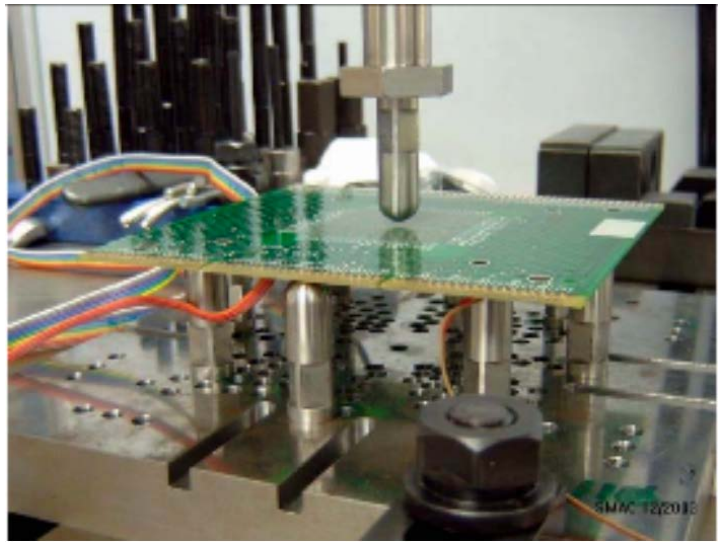


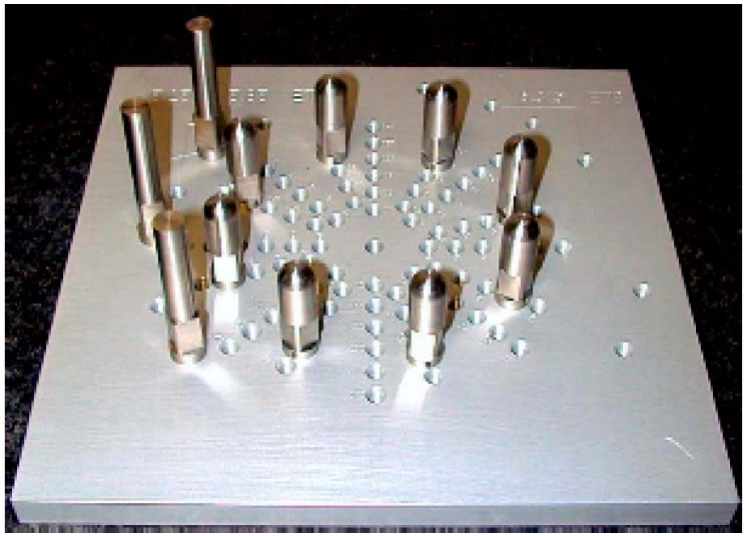






Four-point Bending (IPC9702)

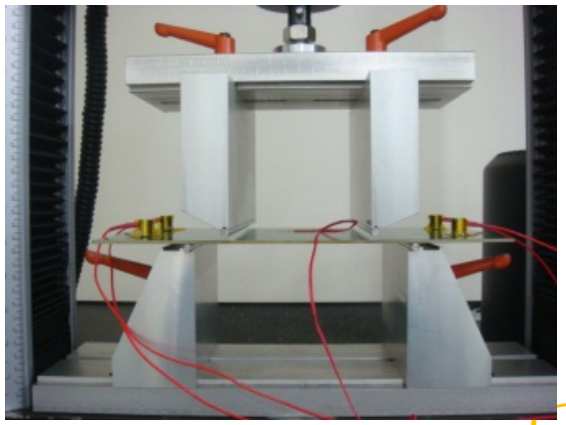


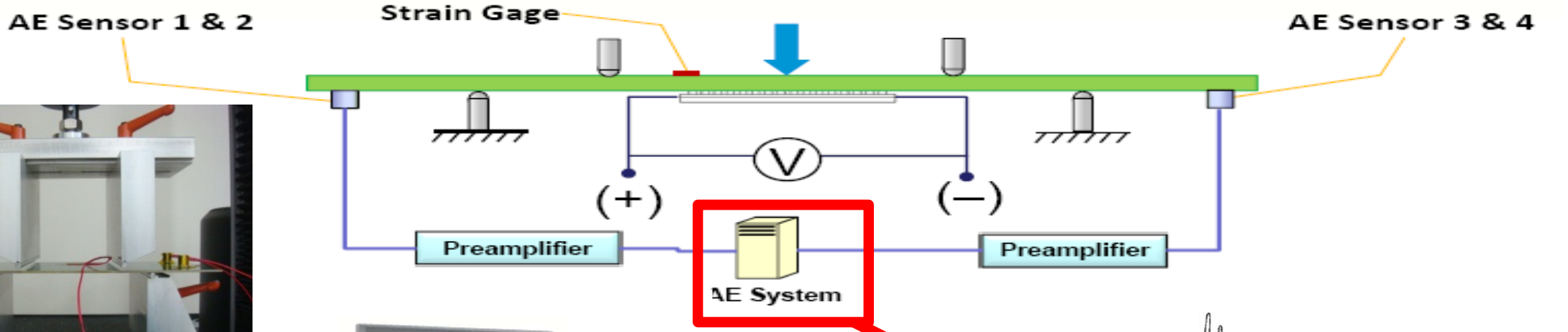


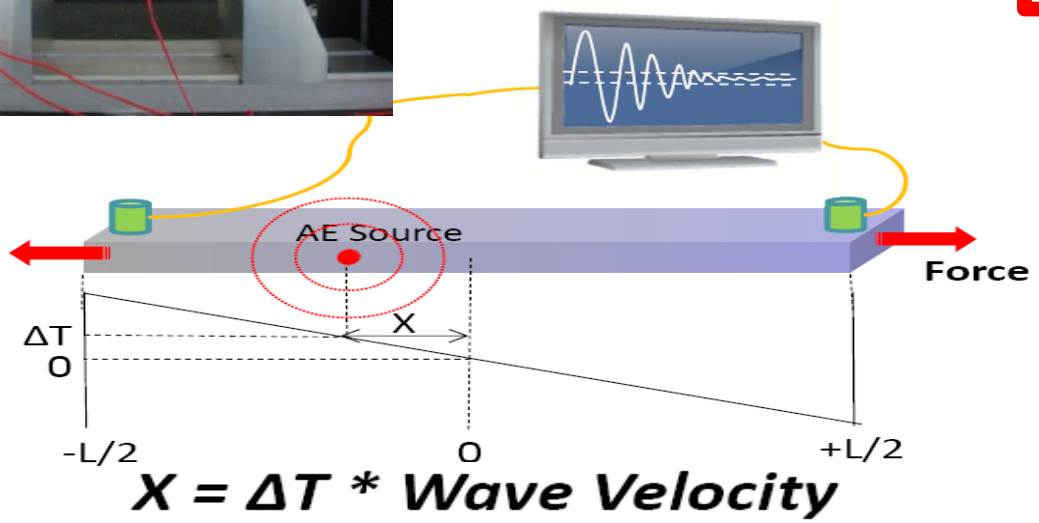
Spherical Bending (IPC9707)

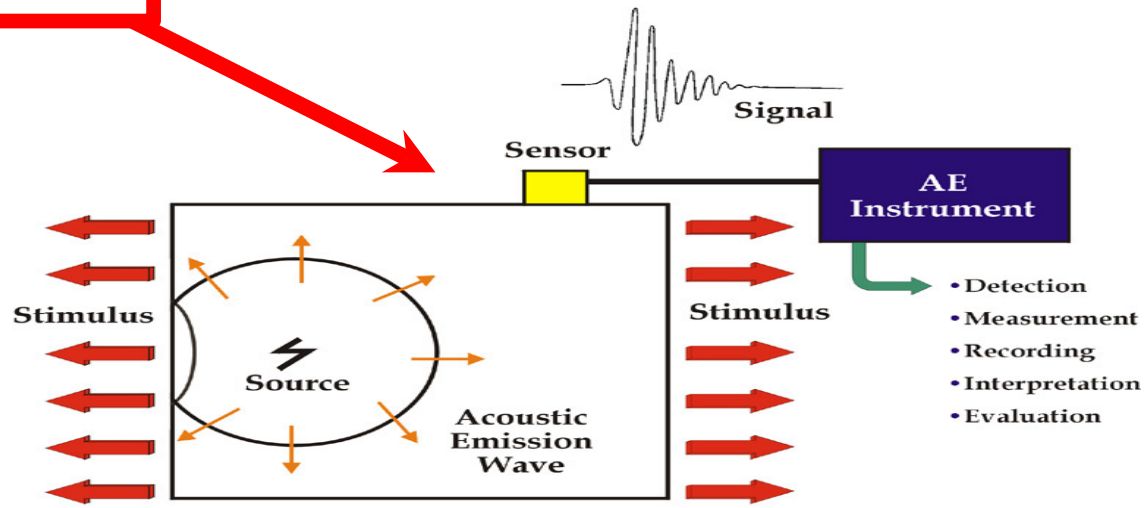
Pad Cratering Test by AE + Static Bending (PCBA level)

IPC9709 : *Test Guidelines for Acoustic Emission Measurement during Mechanical Testing*





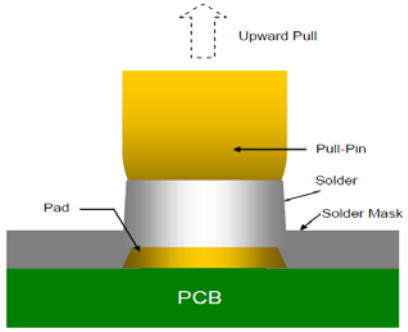


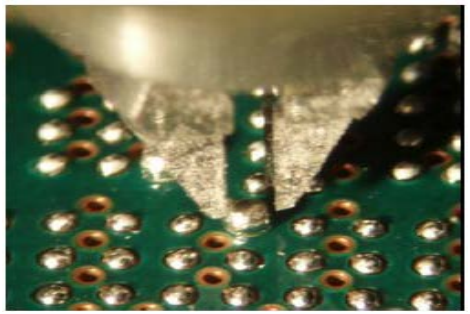


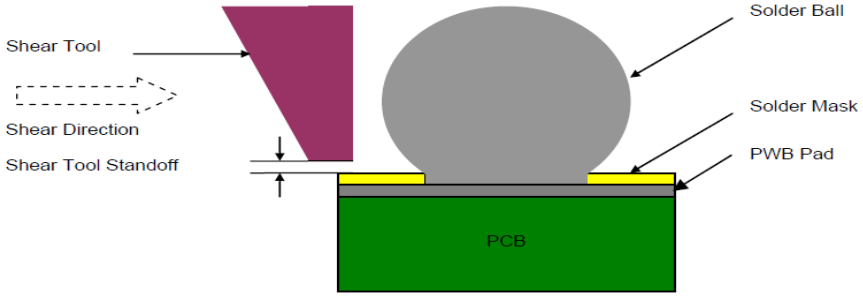
Source:"Investigation of Pad Cratering in Large Flip-Chip BGA using Acoustic Emission"
Anurag Bansal, Gnyaneshwar Ramakrishna and Kuo-Chuan Liu , IPC APEX 2012,

Pad Cratering Test Method Comparison (PCB level)

Test Method	Benefits	Challenges
Hot Pin-Pull Test	1. Can be used on any pad geometry 2. Does not require solder ball attachment 3. More sensitive in differentiating PCB material and design variables than the shear test	1. Requires pins to be soldered to pads, which can be expensive and time consuming 2. Requires solder paste printing
Cold Ball-Pull Test (CBP)	1. Quick test after BGA ball attachment 2. Cost effective – does not require expensive pins 3. Can produce comparable failure modes as the pin pull test	1. Can only be used for BGA pad geometries 2. Requires BGA ball attachment 3. Depends on solder ball, hence requires control of more parameters (clamping pressure, hold time, ball size, ball-to-pad-size ratio, ball metallurgy, jaw size etc.)
Ball-Shear Test	1. Quick test after BGA ball attachment 2. Does not require as much control of test parameters as the ball pull test	1. Can only be used for BGA pad geometries 2. Requires BGA ball attachment 3. Entails using "L-shaped" ball matrix for shear test 4. Less sensitive in differentiating PCB material and design variables than the pin-pull and ball-shear tests 5.Shear values can be artificially inflated due to soldermask definition







The criteria of dielectric materials to be tested

- Electrical Targets:

Dk: 3-4.2 @ 1GHz
Df : <= 0.005 @ 1GHz

- Thermo-Mechanical Targets:

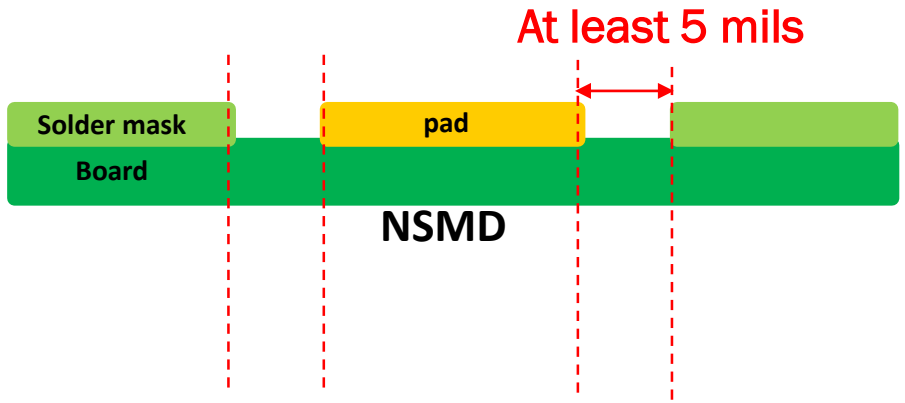
Tg: >160C
Z-CTE: <3.0% from 50 to 260C

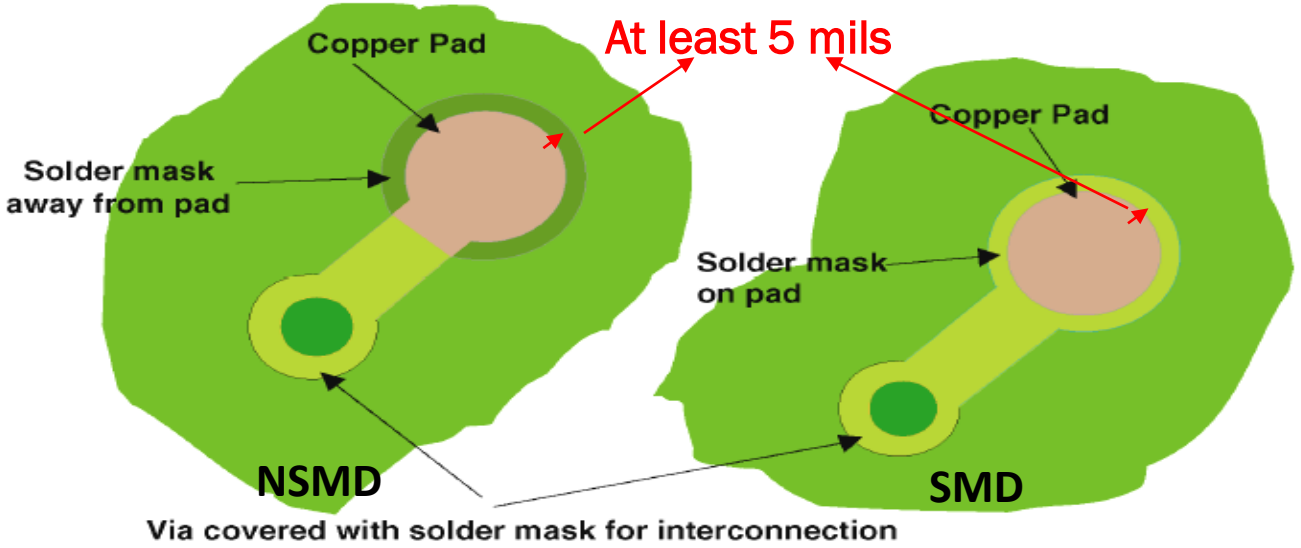
- Construction:

Capable of multiple dielectric thicknesses from 3 mil to 10 mil
VLP or HVLP copper for cores

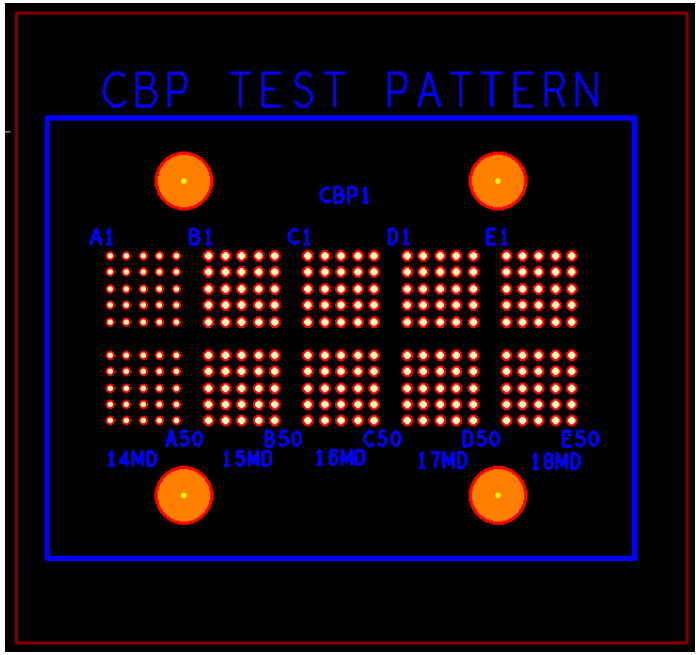
- UL V-0 rating capable

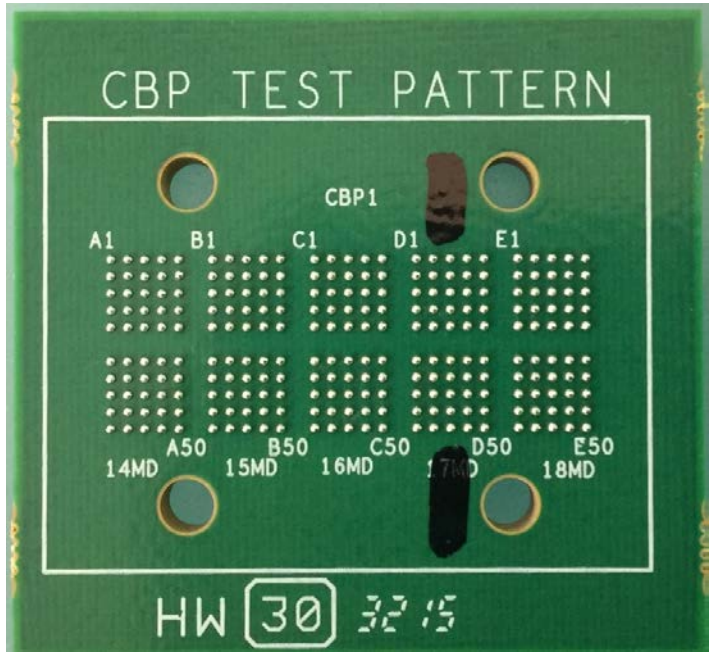
Design of CBP Standard Coupon





These are as designed sizes, they may not be actual





The coupon design incorporated into the material test panel consisted of 2 5x5 round pad arrays for each of 5 unique pad sizes (14, 15, 16, 17, and 18 mil diameter pads). The pads in the arrays were spaced at 1mm pitch and NSMD design with a 5 mil solder mask clearance.

PCB pad size selected for CBP test

PCB Supplier	Supplier Material Code	Coupon ID	Avg. Size of Pad (mil)
G	G3	G3-18	15.9974
		G3-5	16.0697
		G3-7	16.1005
	GE	GE-16	16.0534
		GE-2	16.0278
		GE-3	15.9185
	GL	GL12	16.1796
		GL15	16.1356
		GL16	15.8527
	GY	GY15	15.9087
		GY18	15.9886
		GY9	16.2542
T	T2	T2-12	16.1495
		T2-13	16.2180
		T2-6	15.9129
	T8	T8-2	16.0088
		T8-6	15.9781
		T8-8	15.8365
	TE	TE-12	16.2122
		TE-2	16.1701
		TE-3	15.9258
	TR	TR-2	16.2335
		TR-5	15.6628
		TR-9	15.7586
	TY	TY-10	16.2572
		TY-15	16.1083
		TY-2	16.3239

PCB Supplier	Supplier Material Code	Coupon ID	Avg. Size of Pad (mil)
H	H1	H1-1	16.1813
		H1-2	16.1440
		H1-4	16.2365
	H3	H3-3	16.2135
		H3-4	16.3765
		H3-8	16.3462
	H5	H5-5	15.9951
		H5-8	16.0361
		H5-16	15.9453
	HL	HL-14	15.6046
		HL-19	15.9511
		HL-20	15.8537
	HW	HW-10	15.8447
		HW-18	15.8577
		HW-20	15.8334
	HY	HY-12	15.7753
		HY-4	15.8731
		HY-9	15.8383
V	VE	VE-3	14.5598
		VE-12	14.7232
		VE-15	14.7579
	VR	VR-2	13.9114
		VR-10	13.9253
		VR-15	13.8564
	VY	VY-4	14.8740
		VY-5	14.8332
		VY-8	15.1471

- The designed pad arrays which measured closest to 16 mils +/-0.5 on average were chosen to be tested
- The actual pad size distribution will be up to each PCB shop process control capability such as material and process parameter.
- Each material had 3 coupons with 50 pulls on each which generated 150 peak pulls averaged and analyzed by production statistical software.

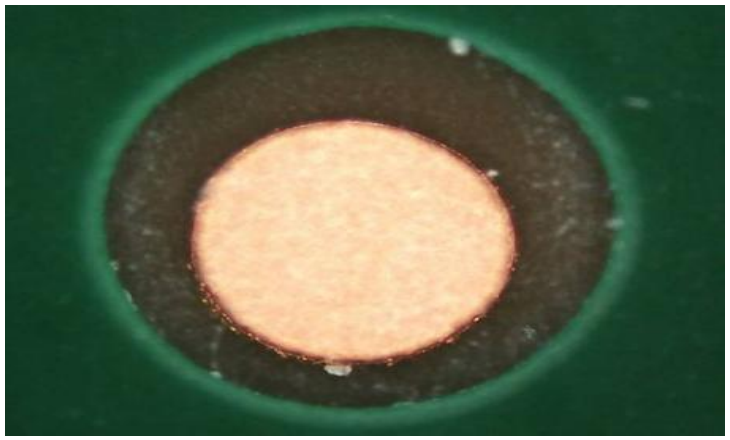
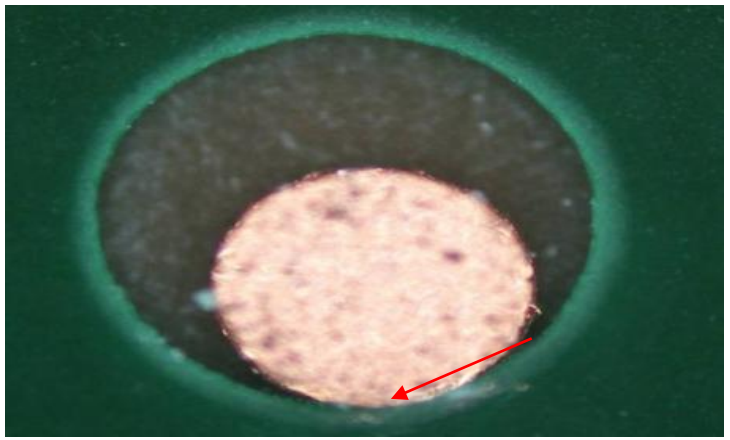
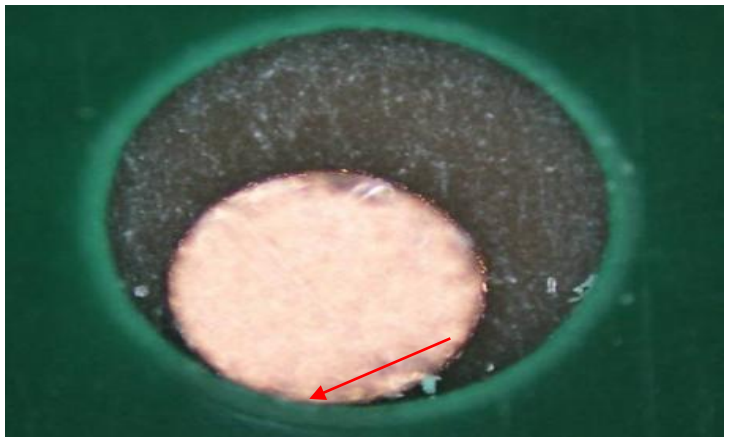
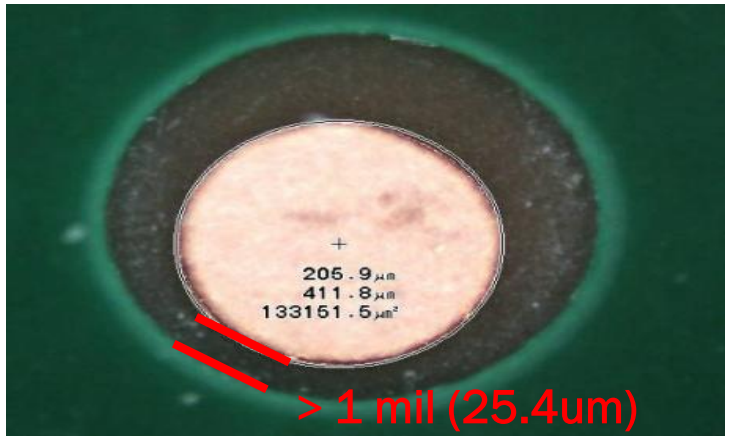
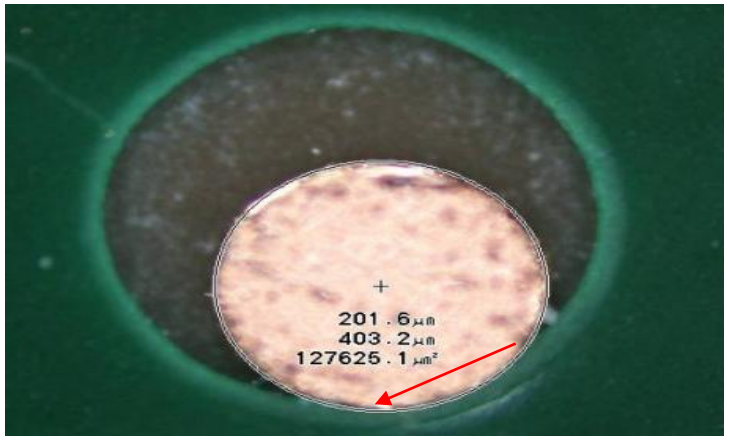
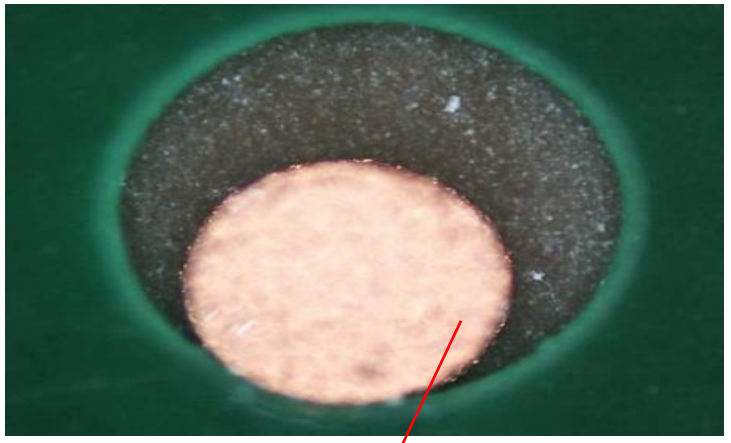
PCB Stackup

- 22 layers
- 4 - 2oz layers in the center of the stack-up
- 150 mils minimum thickness
- Single lamination
- Back drilled electrical structures
- OSP surface finish for reliability test structures
- Spread glass plys (i.e. 1086, 1067, etc.)
- Medium to high resin content for all prepregs

22 Layer Stack-up

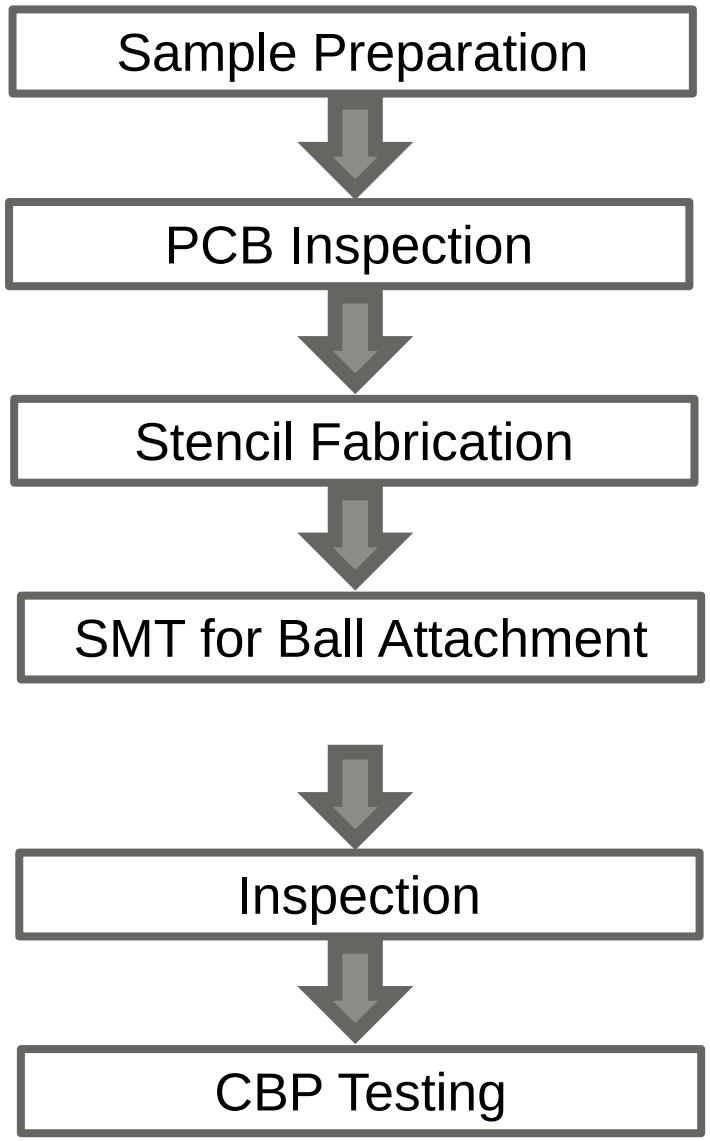
	Description	Layer Type	Thickness	
Layer 1	Plated 1/2 oz Cu (RTF)	Signal	1.6	mils
	Prepreg		3	mils - 1 ply 1078
Layer 2	Unplated 1 oz Cu (HVLP)	Plane	1.3	mils
	Core		4	mil core - 2 ply 1035
Layer 3	Unplated 1 oz Cu (HVLP)	Signal	1.3	mils
	Prepreg		4	mils - 2 ply 1035
Layer 4	Unplated 1 oz Cu (HVLP)	Plane	1.3	mils
	Core		5	mil core - 2 ply 1078
Layer 5	Unplated 1 oz Cu (HVLP)	Signal	1.3	mils
	Prepreg		5	mils - 2 ply 1078
Layer 6	Unplated 1 oz Cu (HVLP)	Plane	1.3	mils
	Core		9	mil core - 2 ply 2116
Layer 7	Unplated 1 oz Cu (HVLP)	Signal	1.3	mils
	Prepreg		9	mils - 2 ply 2116
Layer 8	Unplated 1/2 oz Cu (HVLP)	Plane	0.7	mils
	Core		5	mil core - 2 ply 1078
Layer 9	Unplated 1/2 oz Cu (HVLP)	Signal	0.7	mils
	Prepreg		9	mils - 2 ply 2116
Layer 10	Unplated 2 oz Cu (RTF)	Plane	2.6	mils
	Core		5	mil core - 1 ply 2116
Layer 11	Unplated 2 oz Cu (RTF)	Plane	2.6	mils
	Prepreg		9	mils - 2 ply 2116
Layer 12	Unplated 2 oz Cu (RTF)	Plane	2.6	mils
	Core		5	mil core - 1 ply 2116
Layer 13	Unplated 2 oz Cu (RTF)	Plane	2.6	mils
	Prepreg		9	mils - 2 ply 2116
Layer 14	Unplated 1/2 oz Cu (HVLP)	Signal	0.7	mils
	Core		5	mil core - 2 ply 1078
Layer 15	Unplated 1/2 oz Cu (HVLP)	Plane	0.7	mils
	Prepreg		9	mils - 2 ply 2116
Layer 16	Unplated 1 oz Cu (HVLP)	Signal	1.3	mils
	Core		9	mil core - 2 ply 2116
Layer 17	Unplated 1 oz Cu (HVLP)	Plane	1.3	mils
	Prepreg		5	mils - 2 ply 1078
Layer 18	Unplated 1 oz Cu (HVLP)	Signal	1.3	mils
	Core		5	mil core - 2 ply 1078
Layer 19	Unplated 1 oz Cu (HVLP)	Plane	1.3	mils
	Prepreg		4	mils - 2 ply 1035
Layer 20	Unplated 1 oz Cu (HVLP)	Signal	1.3	mils
	Core		4	mil core - 2 ply 1035
Layer 21	Unplated 1 oz Cu (HVLP)	Plane	1.3	mils
	Prepreg		3	mils - 1 ply 1078
Layer 22	Plated 1/2 oz Cu (RTF)	Signal	1.6	mils

Criteria: PCB Registration Inspection
- EX : Mis-alignment issue in PCB
-Do we need accept the kind of sample for following test?

	B3 (9-2)	B4 (9-4)	B5 (9-1)
16 mil			
17 mil			

Criteria : B3 is OK, B4 and B5 should not be used. Only use samples where there is at least 1 mil clearance between the solder mask edge and the pad

Cold Ball Pull (CBP) Test Flow



1.Sample Q'ty: 5 coupons
2.Clean the PCB surface :Using IPA to clean it.

1.Actual pad size measurement
2.Solder mask opening measurement
3.Solder mask registration inspection

1.Stencil opening size confirmation with pad size
2.Stencil dimension confirmation with pad size
3.Solder stencil used to paste pads: Stainless steel 6 mils thick with 20 mil openings

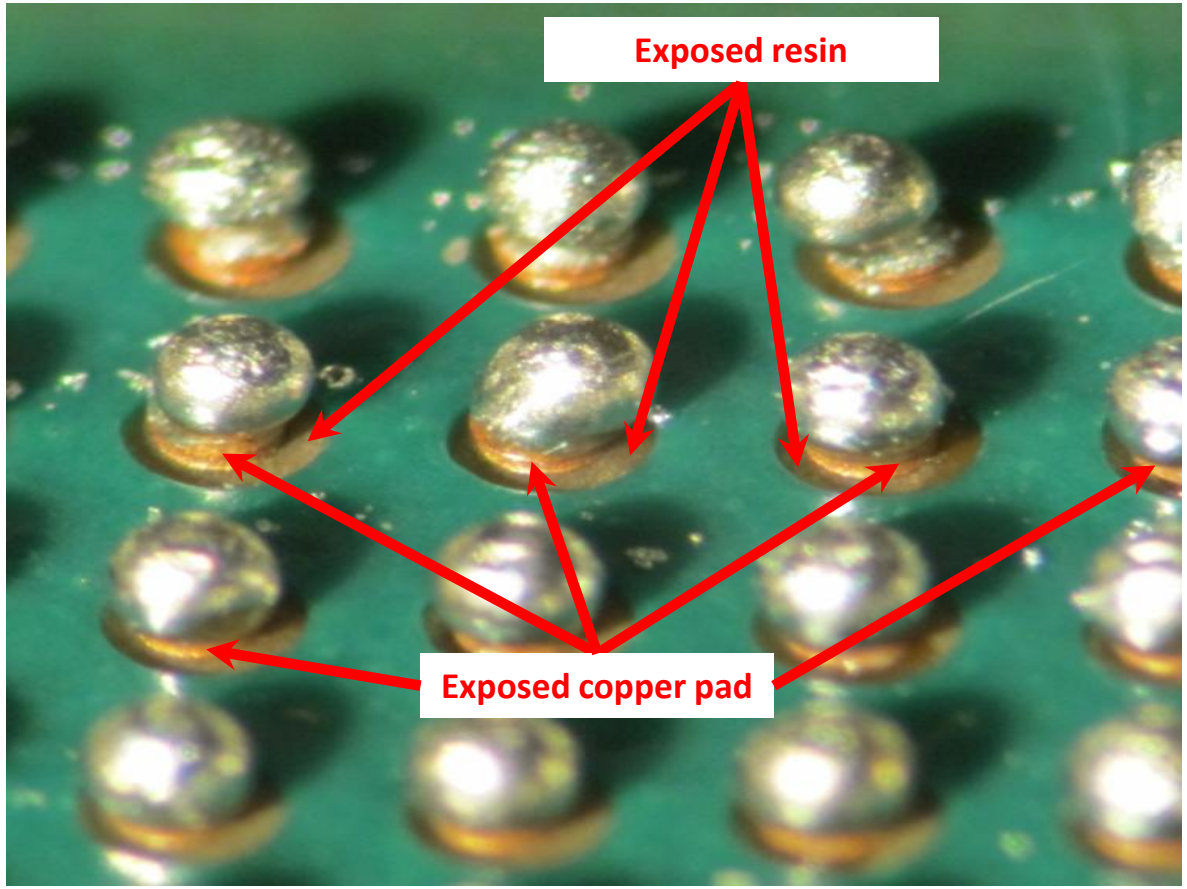
1.Solder Ball: 0.51 mm (20 mil); (SAC405)
2.Solder Paste: ProductionSAC305 paste
3.Reflow Profile: Peak temp. at 245℃ minimum
4.Cooling rate from peak temp: Room temp. without air blowing
5.Nitrogen: Yes O_2 <1500ppm

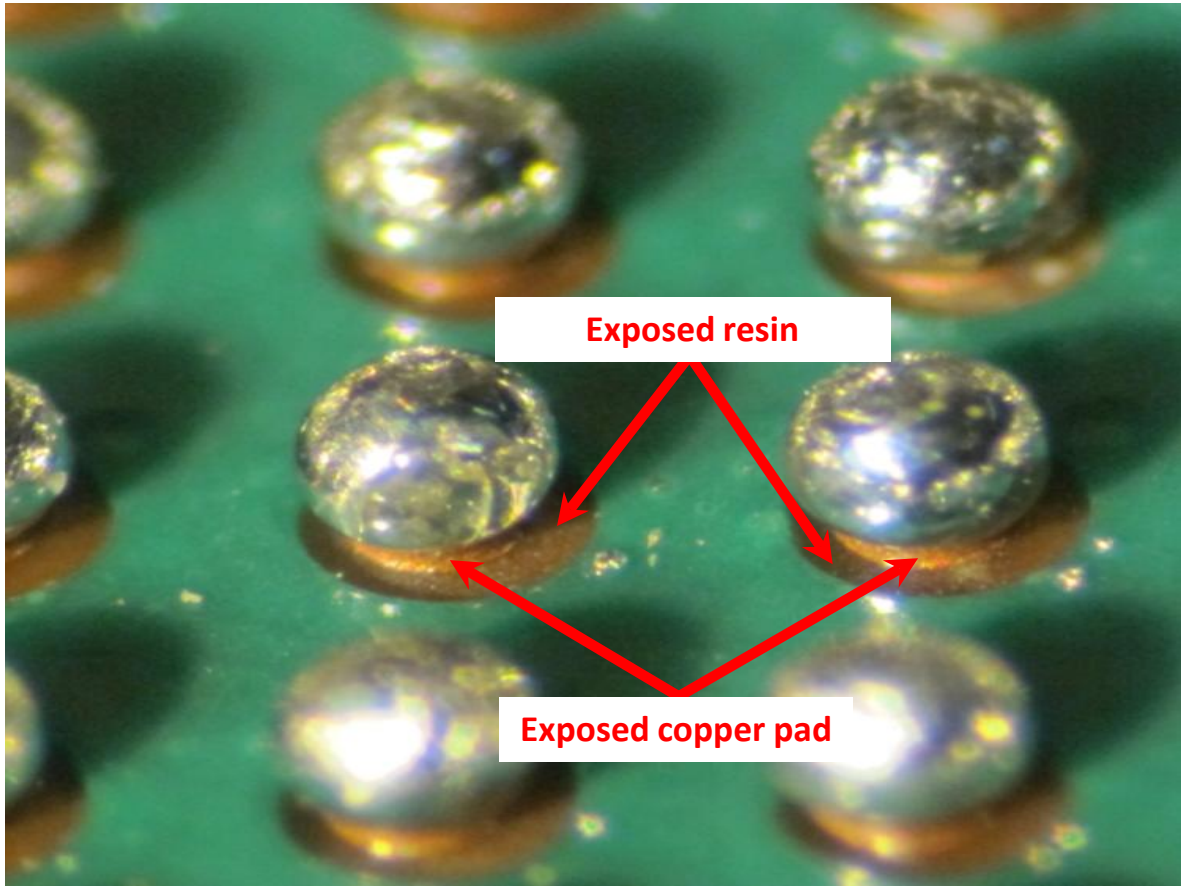
1.Void inspection by X-ray (NG： Void＞25%)
2.The exterior inspection of ball attachment by 3D OM

1.Testing Q'ty: 50 pulls (16mil actual grid location) of each coupon, 3 coupons per material. Totally 150 data point
2.Clamping Pressure: 21 psi
3.Test speed: 5mm/sec
4.Failure Mode confirmation after CBP test
5.Data analysis with production statistical software

The visual inspection of ball attachment

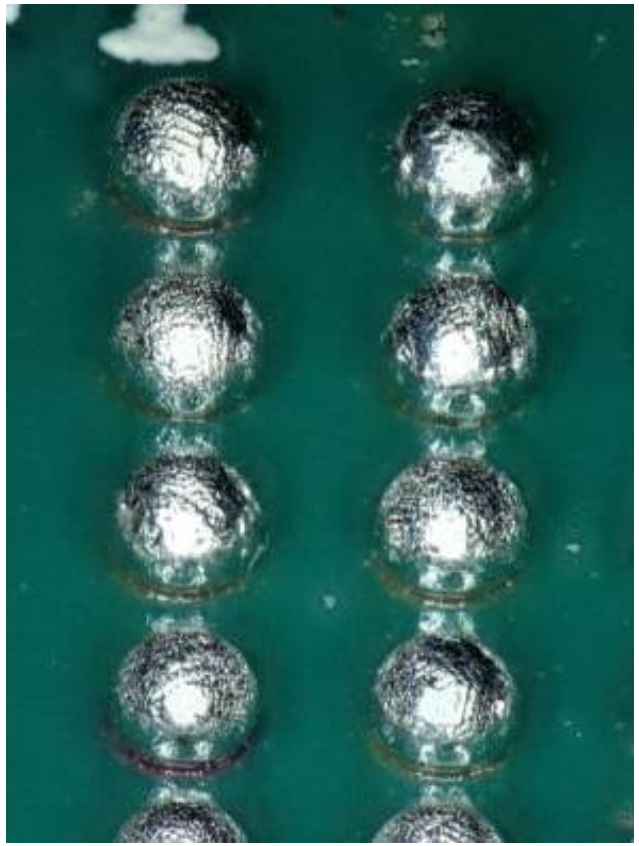
EX : Physical view of *NO* good samples

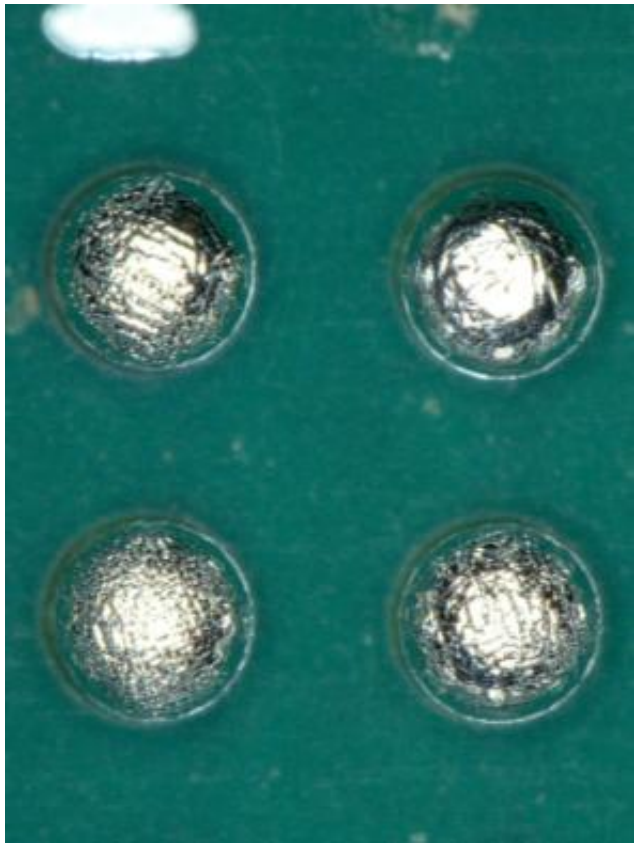


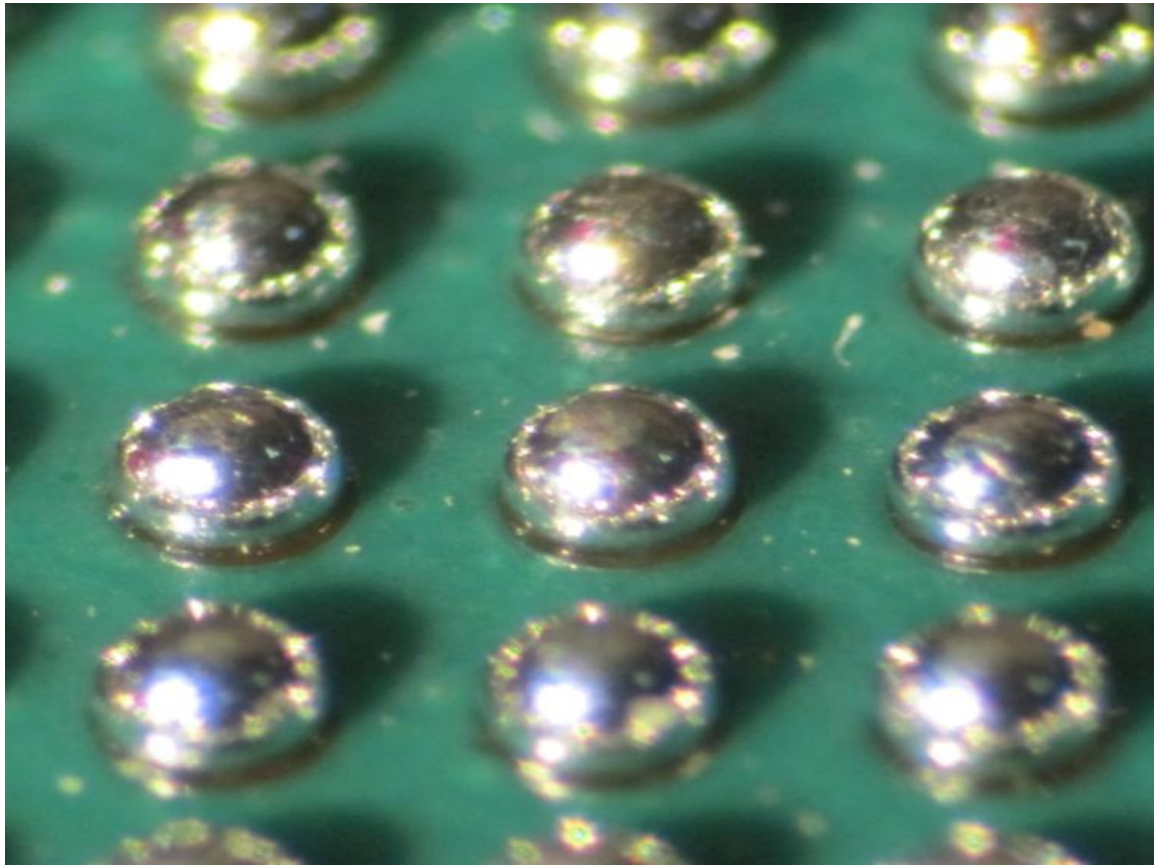


The visual inspection of ball attachment

EX : Physical view of good samples



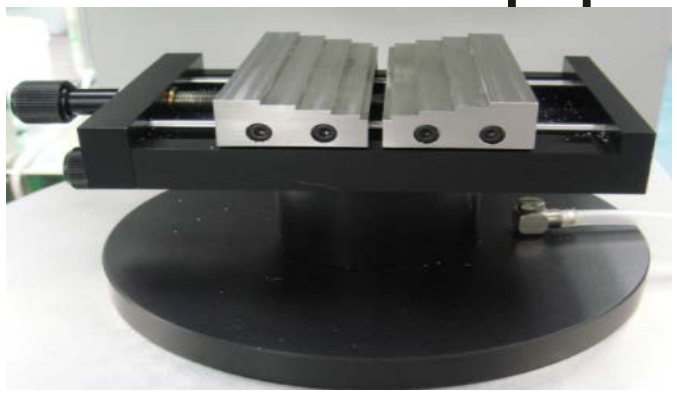




*Copper pads are covered by the solder ball

Test Equipment of CBP

Actual pull condition:
1.Clamping Pressure: 21 psi
2.Test speed: 5mm/sec
3.Jaw type : 750um Jaw

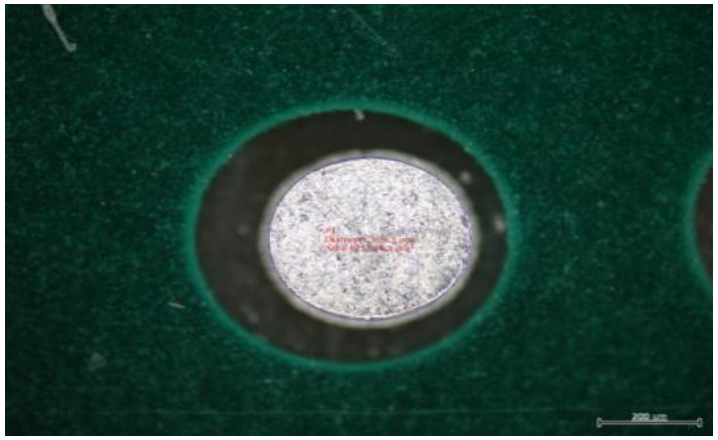
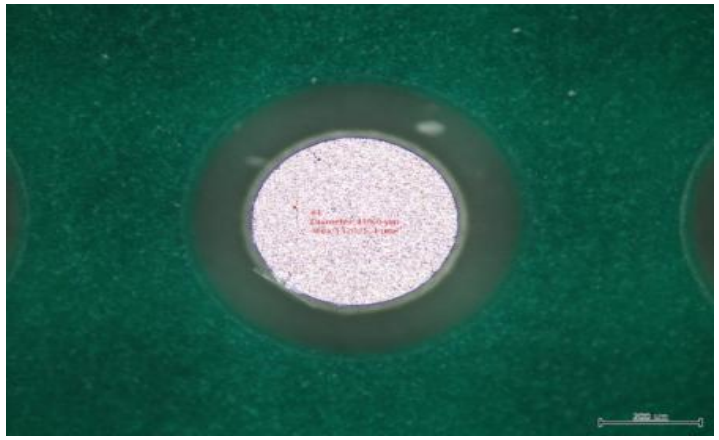
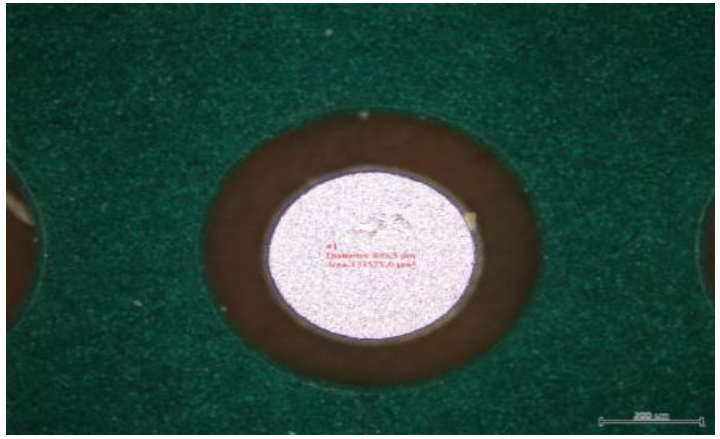
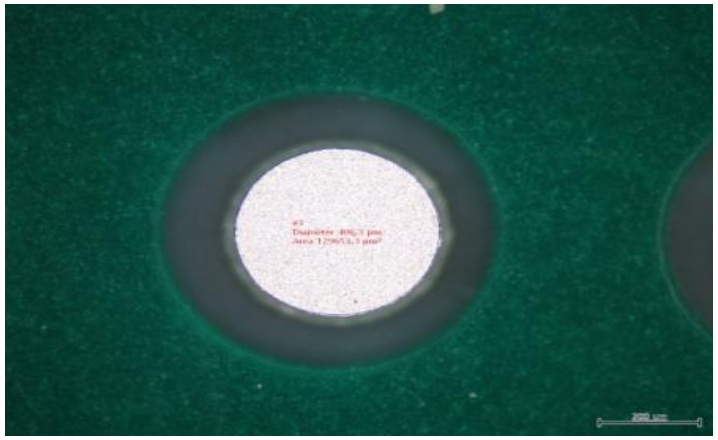
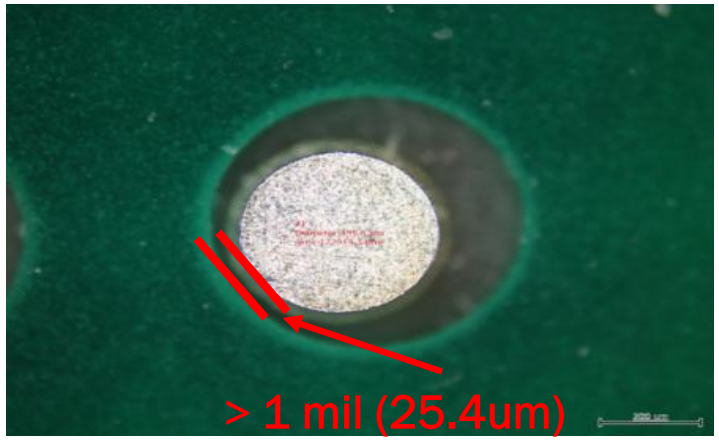
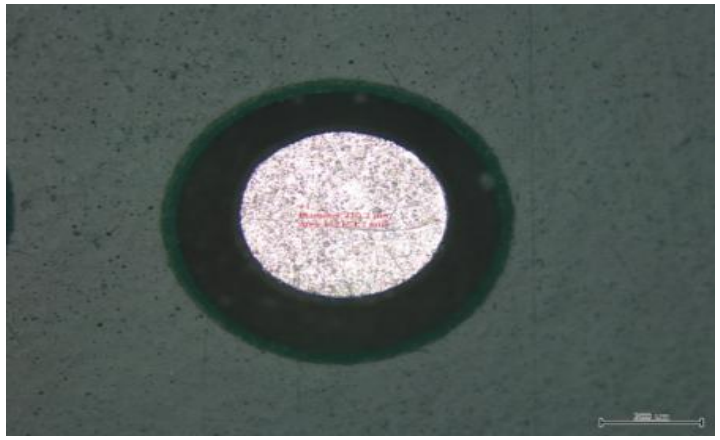


Stage Fixture

Jaw type	Ball diameter
300 um	275~320 um
350 um	330~420 um
470 um	425~520 um
600 um	560~635 um
750 um	700~790 um

Item	CBP
Cartridge	CBP/5KG 5Kg (Max. Pull Force)
	Jaw -CBP-JAW
Ability	Ball Size: 270~825um Speed: 5mm/Sec(Max.)
Module Photo	

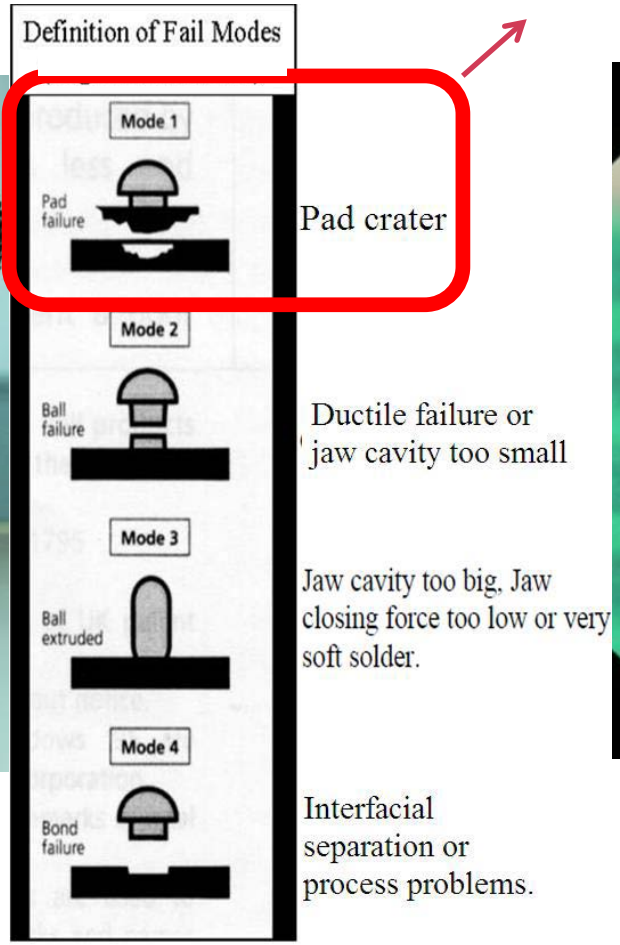
Actual PCB Observation

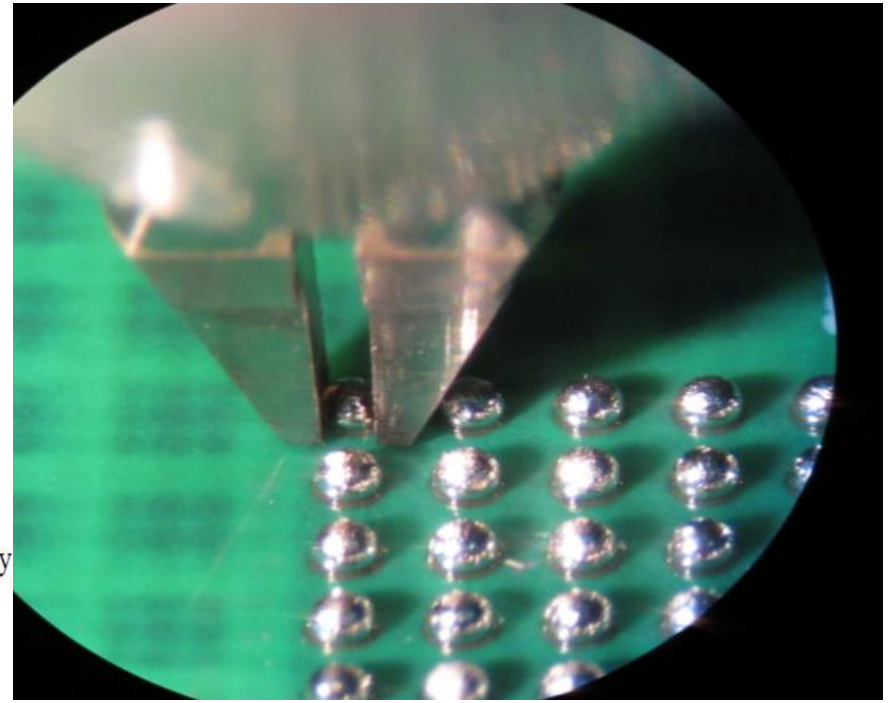
	E	A	C
16 mil			
	D	**F**	**B**
16 mil			

Pad adhesion Testing - cold ball pull

Clamping Pressure: 21 psi

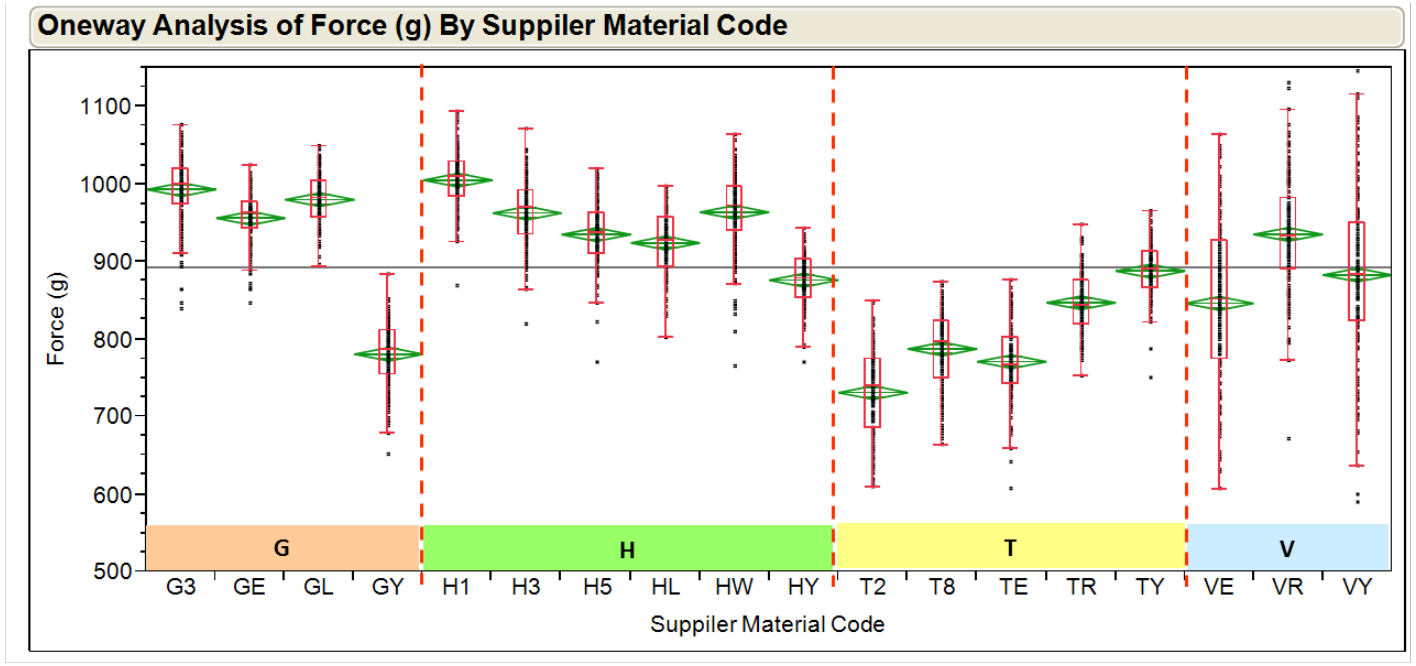
Mode 1 is expected failure mode in the CBP test





Cold ball pull test
(750um Jaw for 20 mil ball size)

The CBP strength among all dielectric materials up to PCB shops



Means and Std Deviations

Level	Number	Mean	Std Dev	Std Err Mean	Lower 95%	Upper 95%
G3	150	993.468	43.3570	3.5401	986.47	1000.5
GE	149	956.482	31.5367	2.5836	951.38	961.6
GL	150	980.370	32.3616	2.6423	975.15	985.6
GY	149	780.930	39.4425	3.2313	774.54	787.3
T2	150	731.295	55.3421	4.5187	722.37	740.2
T8	150	787.651	47.3269	3.8642	780.01	795.3
TE	150	771.238	48.1937	3.9350	763.46	779.0
TR	150	847.340	38.5638	3.1487	841.12	853.6
TY	150	888.232	33.6187	2.7450	882.81	893.7

Means and Std Deviations

Level	Number	Mean	Std Dev	Std Err Mean	Lower 95%	Upper 95%
H1	150	1005.57	37.805	3.0867	999.47	1011.7
H3	149	963.04	42.182	3.4557	956.21	969.9
H5	150	935.34	40.557	3.3115	928.80	941.9
HL	149	924.49	40.490	3.3170	917.94	931.0
HW	150	964.19	48.309	3.9444	956.40	972.0
HY	150	876.45	31.934	2.6074	871.30	881.6
VE	148	846.53	106.539	8.7575	829.22	863.8
VR	150	935.51	70.993	5.7965	924.06	947.0
VY	150	883.16	107.170	8.7504	865.87	900.4

1. G shop：G3>GL>GE>GY
2. H shop：H1>HW>H3>H5>HL>HY
3. V shop：VR>VY>VE
4. T shop：TY>TR>T8>TE>T2

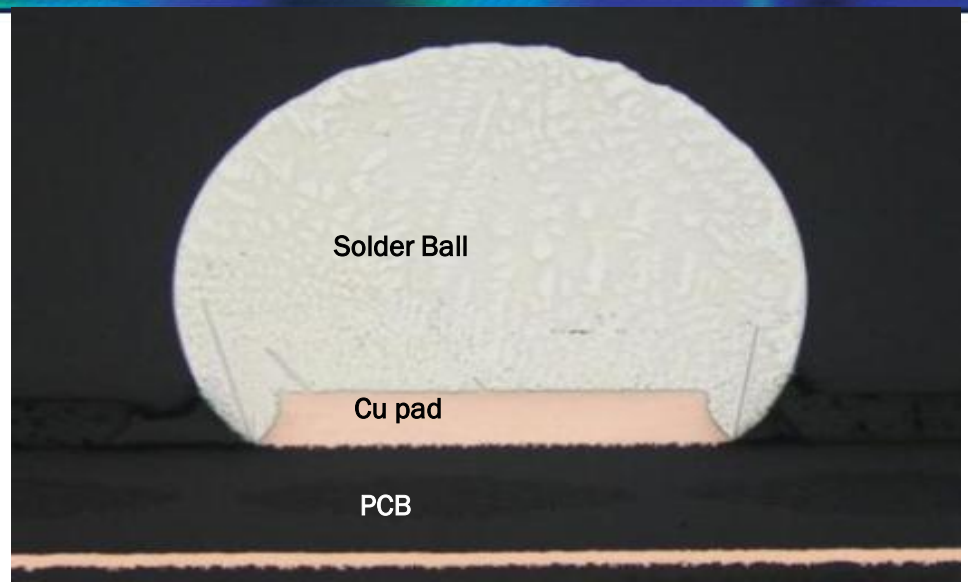
- The data shows performance differences for the same material at different fabrication shops, as well as differences in the materials built at the same shop.
- For example, the performance of material Y is statistically better in shop T than in shop G.
- Additionally, material 3 is statistically better than material Y in shop G.
- There are several potential causes for the CBP performance differences of the materials which may not be directly attributable to the laminate material (copper foil and plating, fabrication process differences between shops, in addition to the pad size differences for the V shop builds).

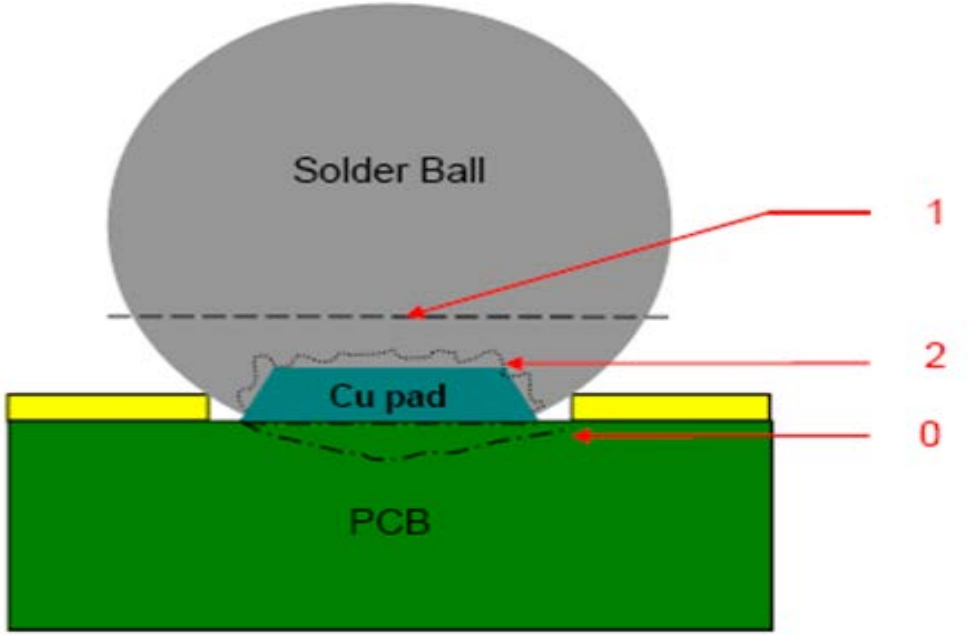
Failure Mode definition

- Different Failure Modes

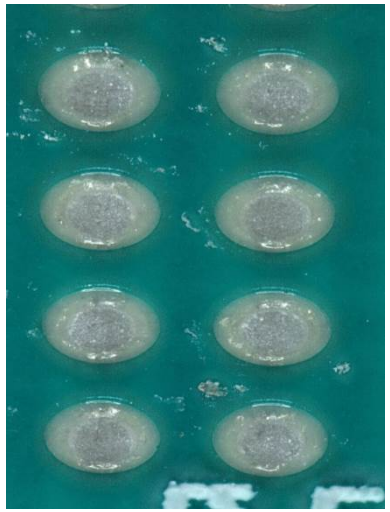
Legend

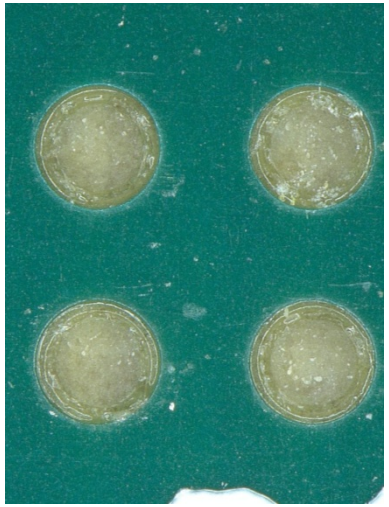
1	Bulk Solder Fracture
2	Fail at PCB IMC interface
0	PCB pad crater (this can be shallow or down to glass bundle)
3	Joint failure mode of A/B and C

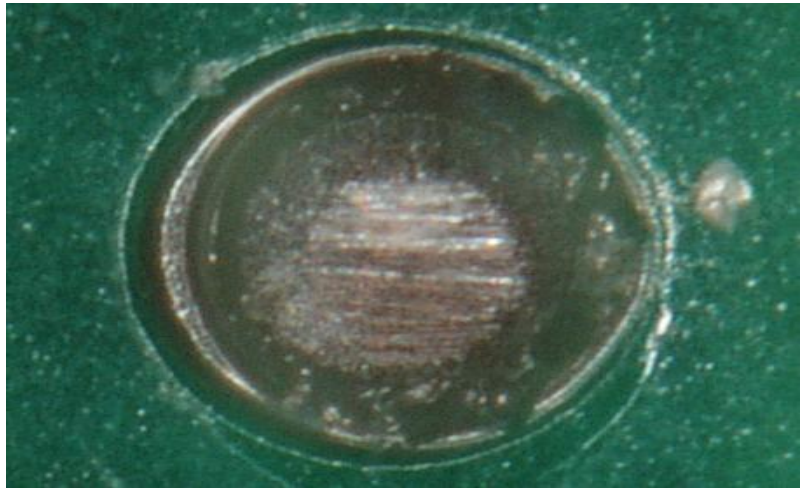


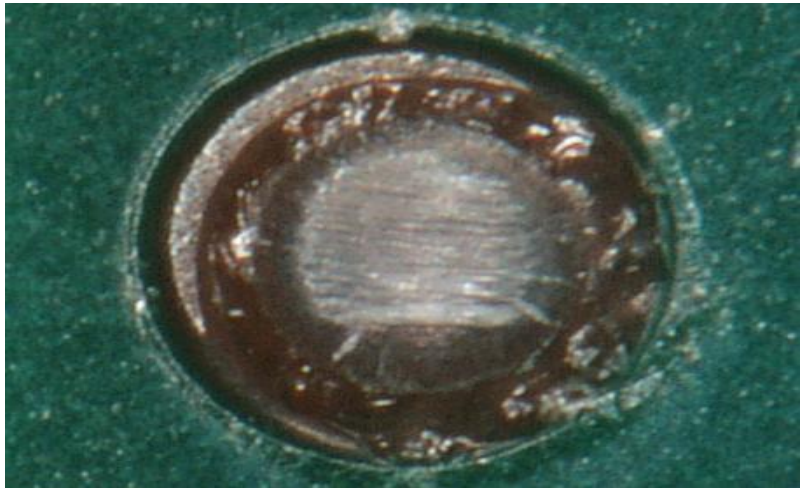


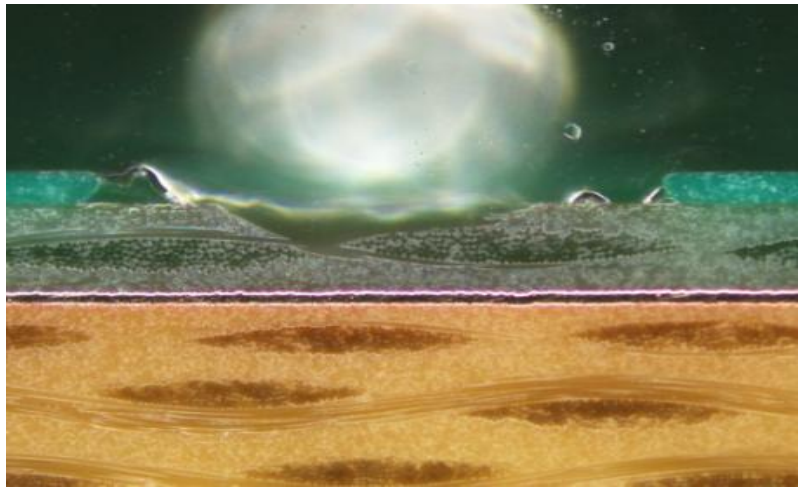
Dominant failure mode : PCB cratering with glass fibers exposed

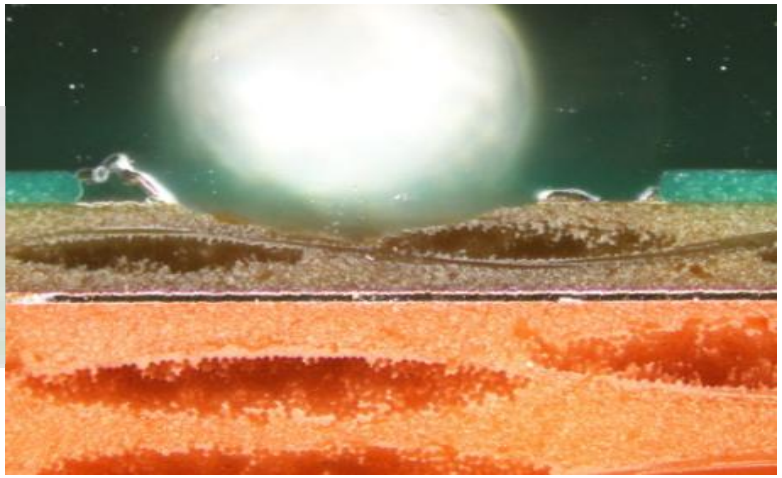


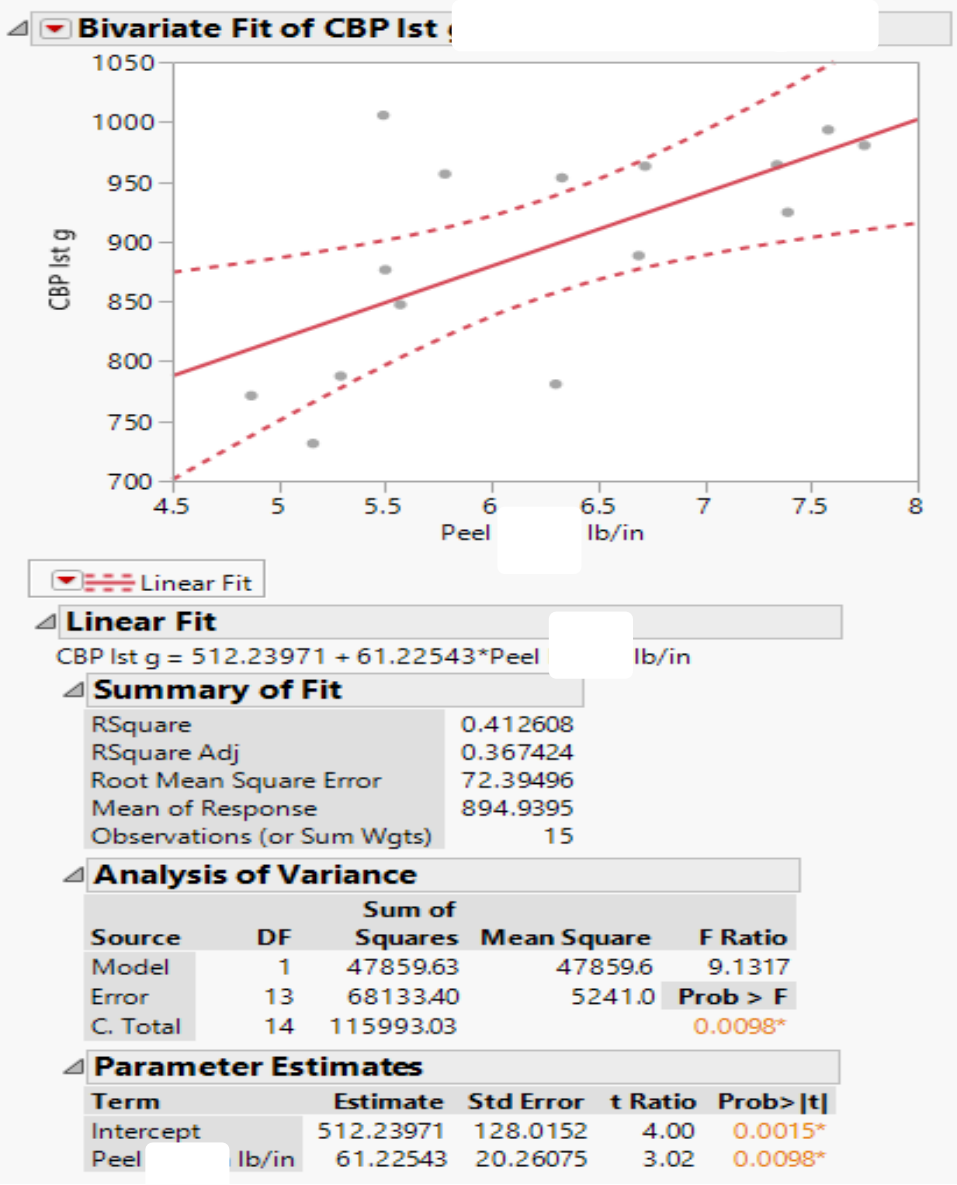












CBP to Peel Strength correlation

1.Positive correlation between CBP and Cu Peel strength.
2.Follows logical path : Higher CBP = High Cu Peel strength

- The peel strength test data here is for the copper foil that the fabricator used on the outer prepreg layer of the stack-up.
- So one would need to run a peel strength test or a cold ball pull test on the fabricator's stack-up to get numbers that would correlate to actual performance.
- We recommend cold ball pull test because of the ability to test an actual pad to correlate to realistic pad cratering performance.

Conclusion Remark

- All failure modes by the test condition designed are cohesive failures with glass fiber exposed as specified in IPC9708,therefore the data is comparable.
- The ranking within a shop of the different materials built is a good indicator of the laminate's strength for that shop's products.
- The same material can perform differently at a different fabricator.
- The ranking of materials can be different based on the fabricator's processing of the laminate materials.
- The test method was demonstrated to be reproducible when carefully executed and produced no anomalous results.

Conclusion Remark

- Cold ball pull testing allows PCB shops to compare which dielectric materials have the best performance to withstand pad cratering based on their process control so as to reduce the field return rate due to pad cratering in PCB assembly and in service life. The comparison of data from different PCB shops is not still suggested due to process deviations at the different shops.

- It was not definitely concluded that the material with certain cold ball pull strength will be capable of withstanding actual PCB pad cratering during PCBA, shipping and service life of product, but was able to provide an indication of the factors in resin system selection and design at a single fabricator, which will impact the relative susceptibility to pad cratering.

- The next steps will be to determine peak pull force thresholds at which pad cratering happens when materials are used in real service. Thresholds are expected to be different depending on product design and fabricator process control.

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- Brand CCL makers for providing ultra low loss dielectric material
- PCB shops for PCB fabrication (Hitachi Chemical, TTM, GCE)
- Intel for CBP test procedure design

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Thank you for your attention!