Determination of Copper Foil Surface Roughness from Micro-section Photographs

Scott Hinaga
Staff Engineer, PCB Technology Group
Cisco Systems, Inc.
Soumya De, Aleksandr Y. Gafarov, Marina Y. Koledintseva, James L. Drewniak,
EMC Laboratory, Missouri University of Science & Technology
Rolla, MO 65401

Abstract

Specification and control of surface roughness of copper conductors within printed circuit boards (PCBs) are increasingly desirable in multi-GHz designs as a part of signal-integrity failure analysis on high-speed PCBs. The development of a quality-assurance method to verify the use of foils with specified roughness grade during the PCB manufacturing process is also important.

Currently, there is no method for adequately quantifying roughness of a signal trace or a power/reference plane layer <u>within a finished PCB</u>. The measurement methods currently available can only be applied to the base foil, prior to its incorporation into a finished board, as they require direct access to the surface to be measured. In a PCB, this surface is not directly accessible, as it is encapsulated within the board, and attempting to expose the surface will necessarily damage or destroy both the board and the surface of interest.

This paper describes a method by which the surface roughness of a metal foil or conductor layer within a PCB may be determined from a microsectioned sample of the same. A small, non-functional area, e.g. a corner of the PCB, can be removed, and the surface roughness of the circuit layers can be assessed without impairing the function of the PCB.

In the proposed method, a conductor (a trace or a plane) in the microsectioned sample is first digitally photographed at high magnification. The digital photo obtained is then used as an input to a signal- and image-processing algorithm within a graphical user interface (GUI). The latter automatically computes and returns the surface roughness values of the layer photographed. The tool enables the user to examine the surface textures of the two sides of the conductor independently. In the case of a trace, the composite value of roughness, based on the entire perimeter of the trace cross-section can be calculated.

1. **Introduction and Background**
2. **Sample Preparation**
3. **Roughness Measurement Technique**
4. **Factors Influencing Repeatability/Accuracy**

Introduction and Background

Signal attenuation in transmission lines due to skin effect loss and surface roughness in copper conductors on printed circuit boards (PCBs) is a well-documented issue, confronting in particular designers of high-speed (>10 Gb/s) circuits **[1-3]**. Knowledge of copper roughness on PCBs is important for high-speed electronics, where accurate separating and modeling of conductor and dielectric losses at the design stage determine quality of the performance of designs **[4]**. To minimize the variation in channel loss within a large population of PCBs built by multiple board shops over an extended period of time and on a variety of different laminate materials, it has become a standard practice at many Original Equipment Manufacturers (OEMs), including Cisco, to attempt to control the surface roughness of copper foils through specification of the roughness grade on the fabrication drawing. Maximum roughness values for PCB circuit foils are governed by the appropriate industry specification for metal foils, IPC-4562A **[5]**. However, as demonstrated in our previous **[6]** and similar **[7]** papers, the roughness profile of an inner-layer trace is influenced not only by the grade of copper foil used on the laminate core material, but also by the oxide or alternative-oxide inner-layer treatment process applied by the PCB fabricator.

Existing measurement methods for conductor surface roughness may be applied to raw copper foil or a sheet of copper-clad core material, either in its original form or following circuitization (including inner-layer treatment). The traditional measurement method used in the PCB industry for over thirty years has been Stylus Profilometry, in which the movements of a mechanical stylus dragged in a straight line across the sample are used to calculate values of roughness **[8]**. More modern non-contact methods commercially available include Laser Profilometry **[9]**, Atomic Force Microscopy **[10]** and White Light

Interferometry **[11]**, which generate a three-dimensional image of the sample's target area, and are thus more representative of the surface profile than the linear measurement generated by a stylus.

However, all of these methods have an important prerequisite: the surface to be studied must be exposed (directly accessible) to the test instrument. Unfortunately for OEMs, in many cases, the first indication of a possible issue with copper surface roughness appears on a finished board, in the form of a signal-integrity test failure involving unexpectedly high channel loss. While high channel loss most assuredly results from sources other than conductor roughness, a complete root-cause failure analysis does mandate that the surface roughness of the trace(s) under test be accurately determined, so that excessive roughness can be eliminated as a contributing root-cause.

Additionally, in the case of a finished and assembled PCB, the circuit layers of concern are laminated within the board, and thus their roughness cannot be assessed by the commercial methods mentioned above. The abovementioned methods are applied today only to PCB components (raw foil and inner-layers) prior to the layer lamination step. Even if one attempts to separate and peel apart a laminated PCB to access the target layers, the surface micro-features of the inner-layer copper will be filled with the dielectric resin to which the foil was previously bonded, and measurement by the above methods will represent not the surface of the actual copper foil, but rather the residual resin adhering to the foil.

The only practical method of accessing an internal layer on a PCB is through micro-sectioning, a quick and inexpensive technique universal throughout the PCB industry. Microsectioning, recognized as an industry-standard technique, has been used for decades as a part of quality assurance in assessing PCB attributes such as hole quality, trace/dielectric dimensions, and plating thickness **[12]**. The ability to use micro sectioned slugs cut from a board to determine surface roughness of the inner-layers would thus be highly useful, building upon a capability already resident at the majority of PCB fabricators, contract manufacturers and electronics OEMs. With the requisite equipment and personnel already in place, such a technique could be deployed without further capital expenditure, as opposed to the previously-described methods which require specialized equipment whose initial cost may exceed $100,000.

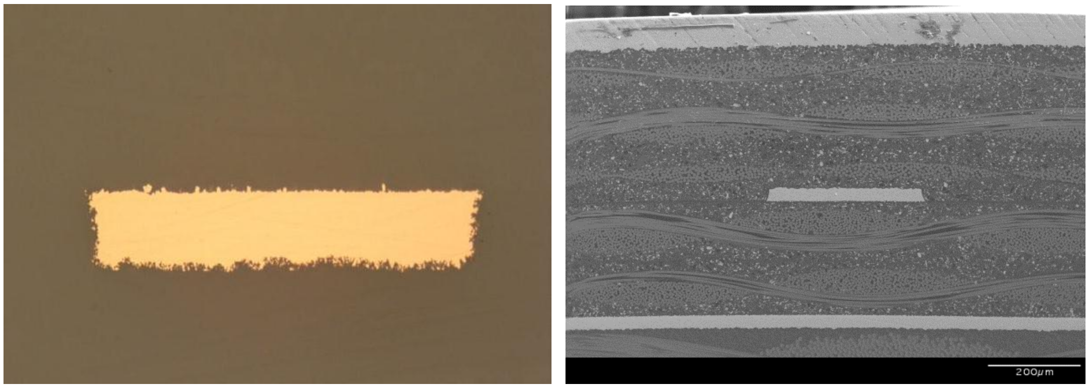
The measurement method described in this paper consists of a software tool which accepts as input a micro-photograph of a PCB micro section in, e.g., *.jpg format. The photograph may be generated either by optical or scanning electron (SEM) microscope, as, for example, those in **[4]**. The pictures may be either monochrome or color. The contour of the target object (signal trace or reference plane) is determined by contrast enhancement between the metal layer, which is lighter in color and/or more reflective, and the surrounding dielectric, which is less reflective. Using the tool, the user is able to select the area of interest within the micro section photograph, and may analyze the top or bottom surface of a copper layer independently, or select the entire periphery of a trace to obtain a composite roughness value. A graphical user interface (GUI) is provided to assist the user in selecting the target area, and to display the measured values using the statistical definitions of roughness most commonly encountered in the PCB industry, viz. Ra, Rq (or Rrms), Rz, and Rt **[4], [13]**.

The authors are aware of a feature within a currently-available image analysis software package **[14],** which is intended to achieve a similar end result. However this technique differs fundamentally from the one presented herein, since the technique **[14]** operates by superimposition of perpendicular grid lines within the microsection photograph and measurement of the length of such, rather than by boundary detection within the image as in our case.

Sample Preparation

Samples for the analysis consist of fairly small (3-10mm) slugs removed from a PCB by punching or routing. The X-Y coordinates of a slug are selected to capture target traces or planes as desired. The slug is encapsulated in a potting compound, typically epoxy-based, so that the copper layers of interest are perpendicular to the plane of view in the finished microsection plug. The surface to be viewed is ground past the zone of mechanical damage from the punching/routing of the slug, then polished to a high degree to ensure that the metal layers are reflective (shiny) and all surface scratches removed.

The plug is then placed on an optical microscope, suitable for micro-photography to produce photos, e.g., in *.jpg format, of the target structures, utilizing the available lighting techniques (specular, diffuse, reflective, etc.) to maximize the contrast between the metal circuit feature and the surrounding dielectric. A typical optical microscope photo is shown Figure 1(a). Following the optical analysis, or in some cases instead of it, the plug may then be sputtered with a conductive layer for SEM photography. An SEM photo is presented in Figure 1(b). There are factors that influence the quality of the *.jpg photo generated, such as the quality of the sample preparation and the microscope set-up. These aspects are discussed in detail in the subsequent sections of this paper. It should be noted that digital images need not be limited to *.jpg format, but may include lossless formats as well, such as *.bmp or *.png, or formats such as *.tif, which may be either lossless or compressed.



(a) (b)

Figure 1: (a) Typical optical photo, (b) Typical SEM photo

Roughness Measurement Technique

The *.jpg image is used as an input to the tool, which displays the photo on-screen, and requests the user to select the region of interest by using the cursor to draw a box around the target area. This step is intended to analyze the image based on the region of interest defined by a user, thereby reducing the computation time for the analysis. Alternatively, the user may select an object whose roughness will be characterized - in this case, it would be either the metal trace or plane. The area being analyzed necessarily consists of light (metal) and dark (dielectric) regions, and the algorithm uses the contrast information within the image to predict the metal/dielectric boundary. If the user is interested in a plane layer, the analyzed area will consist of a light region and a dark region separated by a roughly horizontal boundary, as is seen in Figure 1(b), where the lowest gray horizontal region spans across the image. If the user analyzes a trace, the boxed area will contain the roughly trapezoidal light-colored image of the trace surrounded entirely by the darker dielectric, as is seen in the center of Figure 1b.

The image-processing algorithm, as outlined in Figure 2, uses the pixel information (in grayscale format) embedded in the image to optimize the definable boundary between the light and dark regions. This is done by enhancing the contrast first, and then by analyzing the statistics (mean and variance) of the selected region. The contrast-enhanced image is shown in Figure 3(a). An iterative boundary detection scheme is used to find the boundary, which separates the metal (brighter) and non-metal (darker) regions within the selected region. All gray pixels are thus forced to either pure white (metal), or pure black (non-metal), generating a binary black-and-white image. The boundary between these regions defines the surface texture of the target. This can be seen in Figure 3(b), which shows the binary image obtained from the contrast enhanced image as in Figure 3(a). After obtaining the binary image, the boundary line is extracted as a pixel map into Cartesian coordinate data, based on the input from the user. Each pixel creates one data point. A sample of a bottom surface selected by a user is shown in Figure 3(b). Finally, a de-trending function is applied to eliminate any tilt present in the sample or photo.

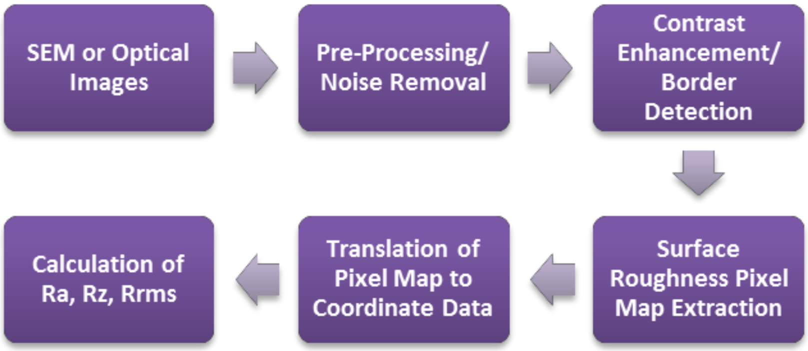
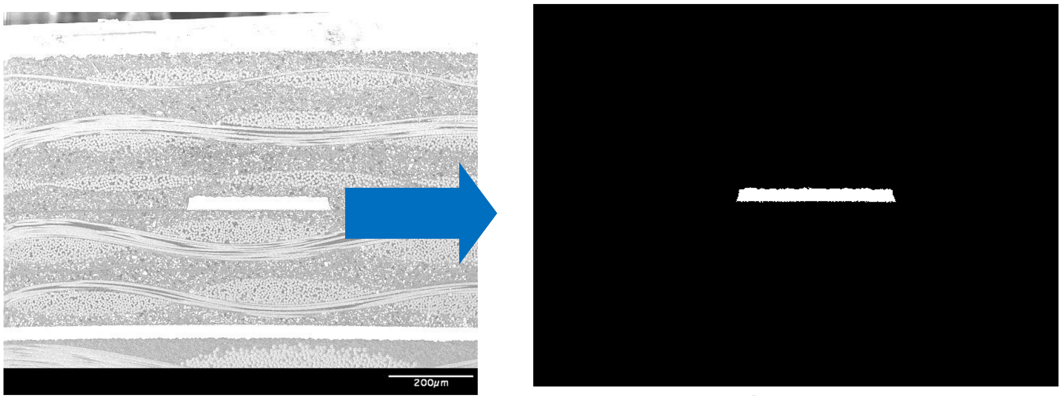


Figure 2: Sequence of image processing steps



(a) (b)

Figure 3: a) Contrast-enhanced SEM photo of sample target trace, b) The subsequent binary image.

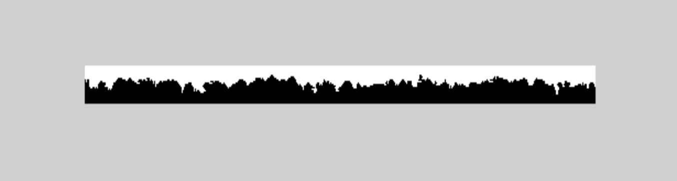
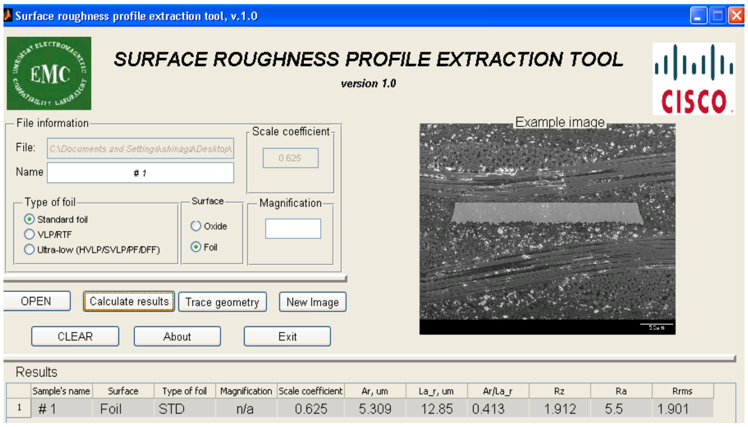


Figure 4: Selection of bottom surface (zoomed), following binary conversion.

The coordinate dataset thus generated from the user-selected surface, e.g. the one shown in Figure 4, is functionally analogous to datasets which could be generated by different techniques, e.g., a two-dimensional stylus measurement, or a three-dimensional data set generated by one of the non-contact measurement methods for a planar slice.

The tool must be provided with a scale factor for the photo in order to tie the size of the peaks and valleys, in pixels, to actual measured distances in mils or microns. This may be in the form of the magnification factor for the *.jpg, typically known when the photo is taken, as is shown in the lower right corner of Figure 1(b). An alternative method is to use the cursor to select or mark a scale bar incorporated into the *.jpg followed by inputting the known length of the bar.

As shown in **[13,15]**, the parameters of peak-to-valley roughness (Rz), average roughness (Ra), and RMS roughness (Rrms) are all obtained by statistical manipulations applied to a base data set consisting of X-Y Cartesian coordinate data. This dataset is essentially a locus of measured points, which define an irregular line bearing numerous peaks and valleys. These three roughness parameters are calculated from simple mathematical expressions, and thus they are indifferent to the source of the base data. The calculated values are displayed by the GUI, as is illustrated in Figure 5.



File information

File: C:\Documents and Settings\shinaga\Desktop\

Name: # 1

Scale coefficient: 0.625

Type of foil: ● Standard foil ○ VLP/RTF ○ Ultra-low (HVLP/SVLP/PF/DFF)

Surface: ○ Oxide ● Foil

Magnification:

Results

	Sample's name	Surface	Type of foil	Magnification	Scale coefficient	Ar, um	La_r, um	Ar/La_r	Rz	Ra	Rrms
1	# 1	Foil	STD	n/a	0.625	5.309	12.85	0.413	1.912	5.5	1.901

Figure 5: Main screen with output of Rz, Ra, and Rrms values

While the primary motivation for developing the technique was to facilitate signal-integrity failure analysis on finished boards, there are additional uses for the tool as well.

First, the method can be used to verify that copper foil used in a given PCB corresponds to the roughness grade specified on the fabrication drawing, provided that the construction of the board calls for inner-layer cores of balanced copper foil construction. In such cases, a small, non-functional area, e.g., a corner, of the board may be removed without affecting the form, fit or function of an operational PCBA, such as a development or prototype board. As the copper planes in the vast majority of high-speed designs are brought out near the edges of the PCB, the surface texture of the planes may be analyzed to verify that roughness-compliant foil was supplied. The OEM may thus check the copper foil on the board independently, without waiting for the PCB fabricator to deliver retained micro section slugs or raw material traceability records. PCB fabricators, in turn, could use this method for the same purpose on micro sections of copper-clad core material. Again, these could be small corner samples which would not render the panel unusable.

Second, the tool may be used to examine the roughness imparted to a board by the PCB fabricator's oxide or oxide-alternative inner-layer treatment process. If the same part number is being built by multiple PCB vendors, an analysis (on non-functional areas as above) can be made to numerically characterize the degree of roughness difference within the supply base, as it is highly likely that the various PCB makers will be using different chemical systems or variations of such. Periodically checking the same supplier over time may reveal roughness variation due to a change in the inner-layer treatment chemistry which might be otherwise unknown to the OEM end-user.

Factors Influencing Repeatability/Accuracy

Several factors are known to influence the repeatability and accuracy of this measurement method. They roughly fall into two groups: (1) factors related to the user's operation of the tool, and (2) factors related to the preparation of the micro section sample and *.jpg photo.

The primary source of variation in measurements using the tool will be due to users' selection of different areas of the photographed surface, where the roughness may be non-uniform across the entire length of the sample. This source of variation is eliminated if users are instructed to select the entire visible object, e.g., a trace, or in the case of a plane, the entire boundary within the field of view. The second source of potential variation may be due to manually selecting the endpoints of the scale bar. This means that the X-Y coordinates marked by different users, even on the same *.jpg, may vary by several pixels. To overcome this ambiguity, the software allows for capturing the target object in the same way as it does with the scale bar, in as much as the length of the scale bar is calculated without reliance on user judgment. However, for this option, it is required that the optical/SEM image contain a scale bar, as shown in the right-hand corner of Figure 1(b) (SEM image).

Preparation of the micro sectioned sample involves a number of variables, some of which can be easily optimized for obtaining the best possible quality of the *.jpg photos. These variables can be summarized as

- orientation of the sample slug to the micro section surface;
- micro section plug preparation;
- magnification factor and sample image size;
- photographic quality (illumination, focus).

Orientation of a sample slug should be such that the PCB layers are normal to the measurement plane to eliminate any accuracy-impacting parallax error. Makers of micro section equipment provide a wide variety of sample clips that will keep the PCB slug vertically oriented during the epoxy potting process. The use of automated sample preparation equipment will ensure that the grind is uniform, and that the cross-section plane remains perpendicular to the PCB sample.

Micro section plug preparation is critical in several respects. First, removal of the sample from the PCB by punching or routing necessarily induces mechanical edge damage in the sample, often including deformation of the internal structures. Ensuring that the sample is ground past this zone into 'virgin' material is a step familiar to those properly trained in microsectioning technique.

The final polishing steps are critical in obtaining a sample which will yield high-quality images. Proper technique ensures removal of surface scratches, which by their contrast may introduce spurious data if they cross the light-dark boundary. Another well-known defect is edge rounding, in which the surface of the polished plug is slightly convex rather than flat. This defect is manifested by the inability to bring the entire target object into focus. For example, if the top surface of a trace is brought into sharpest focus, the bottom will be out of focus to some degree. Use of the hardest possible polishing surface, e.g., thin lapping film, or paper over a metal platen, vs. a soft polishing cloth, in this step will minimize edge rounding.

Choice of magnification factor and sample image size is also subject to user variation. Magnification factor is critical in that the surface roughness features, typically ranging from 1 to 10 µm (Rz), must be substantially larger than the pixel size of the *.jpg. Experimentally, it has been found that magnification factors of 100-250x are sufficient for the rougher foils, whose Rz is typically in the 7-10 µm range, while ultra-low-profile foils with 1-2 µm Rz are better sampled at 500-1000x. In any case, maximizing the size of the target object within the field of view also maximizes the size (length) of the available sample contour, thus improving its statistical validity. However, sometimes the size of the object may be too large, thereby increasing the computational time required by the tool to detect the boundary of the object. It has been experimentally observed that for optimum results, the trace/plane boundary the user intends to analyze should lie near the center of the photograph and occupy approximately 50% of the size of the image. This would ensure the detection of the finest features that might lie within the boundary. Typically, an 8"x6" sized image is used for this analysis.

In any attempt to use a 2-D measurement as a surrogate for a 3-D surface, a minimum sample length must be established in relation to the size of the features measured. This is needed to ensure that the length under consideration provides a statistically sufficient sample. This length will be shorter for ultra-low-profile foils with Rz values of 1-2 µm as compared to standard-roughness foils, whose Rz is four to five times larger. Based on visual inspection of the images for surface roughness analysis, for the worst possible real-life case of Rz ≈ 9 µm for example (see Figure 6), the sample length needed to provide a 99% confidence interval is approximately 350 µm / 13 mils, which corresponds to about 20 correlation lengths Λ for the surface roughness function, as discussed in **[4, 16]**. As the majority of PCB traces are narrower than that, the issue may be overcome in two ways; first, the target trace may be micro-sectioned parallel to the trace; however, due to the difficulty in avoiding the edges of the trace, line widths narrower than 125 µm / 5 mils may best be avoided. For such narrower traces, multiple readings may be taken from a single plug, with the target trace perpendicular, by re-grinding and re-polishing after removing additional material in 0.01-0.05mm increments, as each successive step will expose new surface features. The measured R-values may then be averaged.

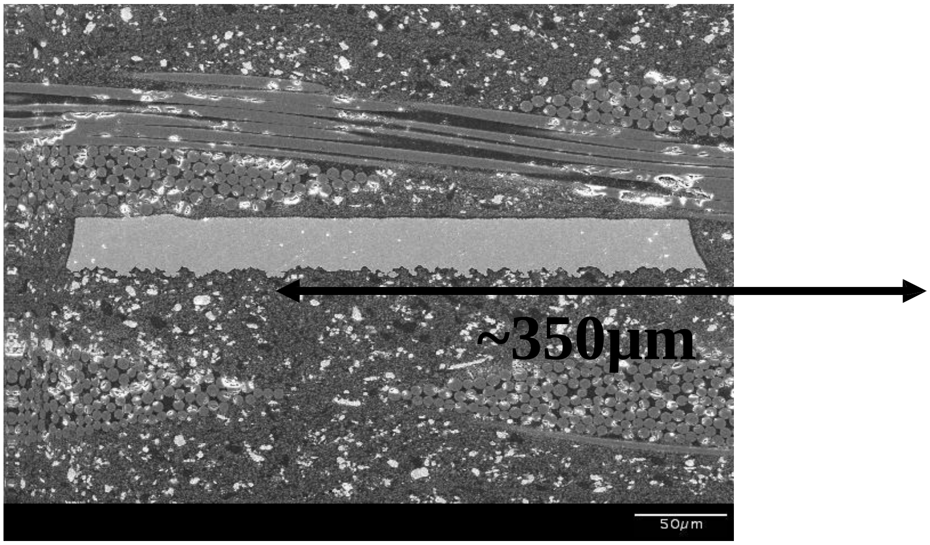


Figure 6: Sample SEM image with Rz ≈ 9 µm

Photographic quality of the *.jpg is important in terms of focus and illumination level. A photo with good focus may be differentiated from one with poor focus in that the former has a lesser number of grayscale steps at the light-dark boundary. While the tool does achieve a sharp boundary by successive elimination of grayscales, starting off with the maximum contrast in the initial pixel map will improve the accuracy of the resolved border and also result in faster processing time. Good microscope technique and avoidance of edge rounding, as is mentioned earlier, are important factors in yielding well-focused photos. It is notably easier to obtain sharply-focused images with a SEM, as compared to an optical microscope.

The optical scope user controls illumination levels via the brightness of the lamp, by the choice of lighting technique (specular, diffuse, and reflective) and by the use or non-use of filters in the light path. The principle is always to maximize the contrast between the light and dark regions – a photograph either under- or over-illuminated will fall short in that respect. Due to the wide variety of microscope designs in the field, the best combination of lighting technique, illumination level and filtering will need to be determined on an individual basis.

A related problem may result from high levels of illumination in conjunction with diffuse lighting and a PCB resin system which is not opaque. Transparent or translucent resin adjacent to the surface under study may allow light to refract or reflect from copper features below the surface plane. Any spurious light which appears in the photo is detrimental to accurate determination of the light-dark border. On the other hand, in the case of a sample that has not been optimally cleaned and polished, it may at times be beneficial to capture the optical microscope image at reduced levels of illumination, thereby minimizing reflections from any surface defects on the metal.

SEM users may maximize contrast by adjustment of the anode voltage, and by ensuring that the sputtered conductive layer thickness and vacuum level are within specified limits.

It should be noted that all sources of variation previously noted will affect even optical roughness measurement techniques based on different operating principles, such as **[14]**. However, the method described herein has an additional requirement: the microsection sample must be free from foreign material contamination, e.g., dust particles, and fibers, lying on top of the light-dark border. Such contaminants, whose grayscale is different from either the copper, or the surrounding dielectric, disrupt the continuity of the light-dark pixel border, and may obscure critical features. Fortunately, loose debris can generally be easily removed from the surface of the microsection plug.

Another important source of variation, not related to the measurement method, is due to actual variation of the roughness level within the PCB - both across different layers, and across the X-Y coordinates within the same layer. These variations occur due to non-uniformity in the copper foil manufacturing process at the foil maker, and in the inner-layer surface treatment process in the PCB shop. For example, a round-robin gage study, in which a single board is passed around the various participants, each necessarily taking a microsection at a different location, would be confounded by any variation in roughness with X-Y position. Likewise, a study in which a single microsection plug of a 12-layer board is sent out without specific instruction as to which of the ten internal layers is to be measured, would be confounded by any differences in roughness between the various layers. The authors are currently unaware of any published data by the copper foil industry regarding inter- and intra-lot variation in roughness on the various grades of foil.

Conclusion

A method of determining the surface roughness of copper foils within a finished PCB is presented, in which measured values of foil roughness are derived from a digital microsection photo of the PCB layer under study. As compared to the existing industry-standard methods, which require costly and specialized equipment for surface analysis, the present method makes use of microsection capabilities already resident throughout the PCB industry. Furthermore, the method is applicable to circuit layers within a finished PCB, whereas existing techniques may be applied only to PCB component materials prior to lamination. The method uses grayscale resolution to define the pixel border between the light (metal) and dark (dielectric) areas of the photo, and then extracts this data into a Cartesian coordinate plot, from which standard definitions of surface roughness are calculated. Accuracy and repeatability of the method are affected by sample preparation and photographic technique. Some strategies for mitigating the known causes of variation are discussed.

Acknowledgements

This work was supported in part by a National Science Foundation (NSF) grant (#0855878) through the I/UCRC program. The authors would also acknowledge the Materials Research Center (MRC) of Missouri S&T for allowing use of their SEM equipment (Hitachi 570 and Hitachi 4700) for this study, and the invaluable help provided by Ms. Clarissa A.Wisner, an MRC electron microscope specialist.

References

[1] Y. Shlepnev, C. Nwachukwu, “Roughness characterization for interconnect analysis”, - 2011 IEEE International Symposium on Electromagnetic Compatibility, Long Beach, CA, USA, August 17, 2011.
[2] P. G. Huray, O. Oluwafemi, J. Loyer, E. Bogatin, X. Ye “Impact of Copper Surface Texture on Loss: A Model that Works”, DesignCon 2010
[3] G. Romo, C. Nwachukwu, R. Torres, S. Baek and M. Schauer, “Stack-up and Routing Optimization by understanding micro-scale PCB effects”, DesignCon Expo 2011, paper 5-TA3.
[4] A. Koul, M.Y. Koledintseva, J.L. Drewniak, and S. Hinaga, “Differential extrapolation method for separating dielectric and rough conductor losses in printed circuit boards”, IEEE Trans. Electromag. Compat., vol. 53, 2011, doi: 10.1109/TEMC.2010.2087341, pp. 1-13 (to be published).
[5] IPC, IPC-4562A - Metal Foil for Printed Wiring Board Applications, April 2008; Table 3-1

[6] S. Hinaga, M. Koledintseva, P. Anmula, and J. Drewniak, “Effect of Conductor Surface Roughness upon Measured Loss and Extracted Values of PCB Laminate Material Dissipation Factor”, Proceedings of the Technical Conference, IPC Expo/APEX 2009, Mar.31–Apr.2, 2009, Las Vegas, USA, paper S20-2

[7] A. Ippich, “A Designed Experiment for the Influence of Copper Foils and Oxide Replacements on Impedance, DC Line Resistance and Insertion Loss”, Proceedings of the Technical Conference, IPC Expo/APEX 2011, Apr. 9-14, 2011, Las Vegas, USA, paper S31-02

[8] IPC Test Methods Manual TM-650, method 2.2.17A; accessible at http://www.ipc.org/ContentPage.aspx?pageid=Test-Methods

[9] See for example: http://www.solarius-inc.com/html/laserscan.html

[10] See for example: http://www.home.agilent.com/agilent/product.jspx?nid=-33986.0&cc=US&lc=eng&pageMode=OV

[11] See for example: http://www.bruker-axs.com/white_light_interferometric_profilometers.html

[12] IPC Test Methods Manual TM-650, methods 2.1.1E and 2.1.1.2A

[13] E. Degarmo, J. Black, R. Kohser, Materials and Processes in Manufacturing; 9th Ed. (2003), p. 223.

[14] Datasheet, Buehler OmniMet 86-3310 Surface Roughness Assessment Module, accessible at: http://www.buehler.com/productinfo/image_analysis/pdfs/surface_roughness.pdf

[15] T. Chi, T. Ballinger, and R. Olds, “Surface texture analysis using stylus profilers,” VEECO, 2010. Available at: http://rpi.edu/dept/cie/mncr/documents/AN525_Dektak_Surface.pdf

[16] X.Gu, L. Tsang, and H. Braunish, “Modeling effects of random rough interface on power absorption between dielectric and conductive medium in 3D problem”, IEEE Trans. Microw. Theory Techn., vol. 55, no. 3, pp. 511-517, March 2007

Biographies

Scott Hinaga holds the position of Staff Engineer in Cisco’s PCB Technology Group, and is responsible for investigation and characterization of new laminate materials. He holds a B.S. from Stanford University, joined Cisco in 2004 and has PCB manufacturing and engineering management experience dating back to 1985.

Soumya De has been a graduate student (Ph.D) with the EMC Laboratory of Missouri University of Science and Technology since 2009. He holds a B.E. in Electronics Engineering from Nagpur University. Currently he is a co-op/intern with Cisco Systems, Research Triangle Park, North Carolina.

Aleksandr Y. Gafarov joined the EMC Laboratory of Missouri University of Science and Technology as a graduate (M.S.) student in Fall 2010, after he received his B.S. degree in Radio Physics and Electronics from Moscow Power Engineering Institute (Technological University), Moscow, Russia.

Marina Y. Koledintseva, Ph.D., has been a Research Professor at the Missouri University of Science and Technology, Electrical and Computer Engineering Department, since 2000. Before that she was a Senior Scientist and Associate Professor of Radio Engineering Department of Moscow Power Engineering Institute (Technical University), Moscow, Russia.

James L. Drewniak, Ph.D., since 1991 has been a Professor with the Missouri University of Science and Technology (MS&T), formerly known as UMR, Electrical and Computer Engineering Department. In 1995-2008 he was the co-director of the EMC Laboratory and the EMC Consortium. In 2002-2007 he was the Director of the Materials Research Center of the same University.