High Throw Electroless Copper – Enabling new Opportunities for IC Substrates and HDI Manufacturing

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Introduction

The one constant in electronics manufacturing is change. Moore's Law, which successfully predicted a rate of change at which transistor counts doubled on Integrated Circuits (ICs) at lower cost for decades, is ceding to be an appropriate prediction tool. Increasing technical and economic requirements, deriving from the semiconductor environment, are cascaded down to the printed circuit and in particular to the IC substrate manufacturers. This is both a challenge and an opportunity for IC Substrate manufacturers, when dealing with the demands of the packaging market.

As a consequence, miniaturization of lines and spaces (L/S) down to 5/5µm and even below to 2/2µm in conjunction with smaller Blind Micro Vias (BMV), is required to meet the very challenging wiring densities for new technologies. However, implications of the 'faster, smaller, and cheaper' mindset also affect high-end High Density Interconnect (HDI) printed circuit board manufacturers. The existing production infrastructure based on panel plating is not capable of 20/20µm L/S – as required by OEMs for high-end mobile devices. As a consequence of this, production technology needs to change to pattern plating.

Miniaturization leads to increased requirements for all process steps involved in the value-added-chain. This paper discusses the corresponding challenges for metallization based on electroless copper processes. In order to minimize the effect of the differential etch process, which is one of the major factors determining surface feature resolution, the thickness of the deposited electroless copper layer on the surface of the substrate must be reduced. Moreover, the thickness at the sidewalls and bottom of the BMV must be improved to ensure excellent via filling performance. These contradicting requirements can only be fulfilled by increasing the throwing power (TP) of the applied electroless copper bath.

This paper introduces two new electroless copper baths developed for IC substrates manufacturing based on Semi Additive Process (SAP) technology *(hereafter referred to as E'less Copper IC)* and HDI production *(hereafter referred to as E'less Copper HDI)* and optimized for high throw into BMVs. An introduction to reliable throwing power measurement methods based on scanning electron microscope (SEM) is given, followed by a compilation and discussion of key performance criteria for each application, namely throwing power, copper adhesion on the substrate, dry film adhesion and reliability.

State of the Art Technologies and Future Challenges

The state of the art production technology for high end IC substrates – characterized by smallest L/S at the outer redistribution layer (RDL) – is the SAP technology in vertical application mode. Contrary to the intuitive meaning of the expression 'semi *additive* process', the technology is in fact still a subtractive build-up technology and the L/S resolution is limited by the differential etch process step that is applied to form the desired pattern and that comes along with an inherent line width reduction.

However, the differential etch is reduced by the usage of bare laminates (build-up films without a copper clad) resulting in a reduced copper thickness that needs to be etched. Leading IC substrate manufacturers are etching approximately 1.0 µm electroless copper plus additional 1.0 – 2.0 µm safety margin because of the rough surface (R_z ~ 2.0 µm) and achieve 9/12 µm L/S with acceptable yield in mass production. A further reduction in L/S requirements below this 21 µm track pitch could be theoretically fulfilled in different ways:

Firstly, a fully additive process (FAP) would make the differential etch step superfluous because the pattern is created before copper is plated. Unfortunately, there is no mass production proven FAP technology established yet in the industry. Secondly, new manufacturing approaches in development like laser embedded conductors (LEC) could contribute to increased wiring densities. Thirdly – and closest to mass production – the state of the art subtractive SAP technology and all involved process steps could be optimized for minimized differential etch. Imperative for this capability extension of the SAP technology is a further reduction of the electroless copper layer thickness on the surface of the build-up layer. The electroless copper layer thickness in the wedge of the BMV on the other hand is limited to a certain minimum because of conductivity and process safety requirements of the following development and via filling process steps. These contradicting requirements of the layer thickness on the surface and in the BMV can only be solved by an increased throwing power of the

electroless copper bath. In this context, throwing power is generally defined as the ratio between the deposited electroless copper thickness in the BMV compared to that on the surface (refer to a detailed explanation in chapter *Throwing Power Measurement Methods*). The impact on L/S resolution of a reduced electroless copper surface thickness is illustrated in figure 1. As can be seen in the upper part of the schematic drawing, the state of the art technology, simulated for targeted 5/5 µm L/S, faces an inevitable line reduction due to the differential etch of about 3 µm (1 µm electroless copper plus an additional safety margin of 2 µm due to the roughness of the surface). In order to increase the actual line width all relevant process steps need to be pushed to the limits. The electroless copper thickness must be reduced and new base materials, characterized by a lower surface roughness compared to standard materials are required. All measures sum up to an actual line width increase of 75% from 2.0 µm to 3.5 µm.

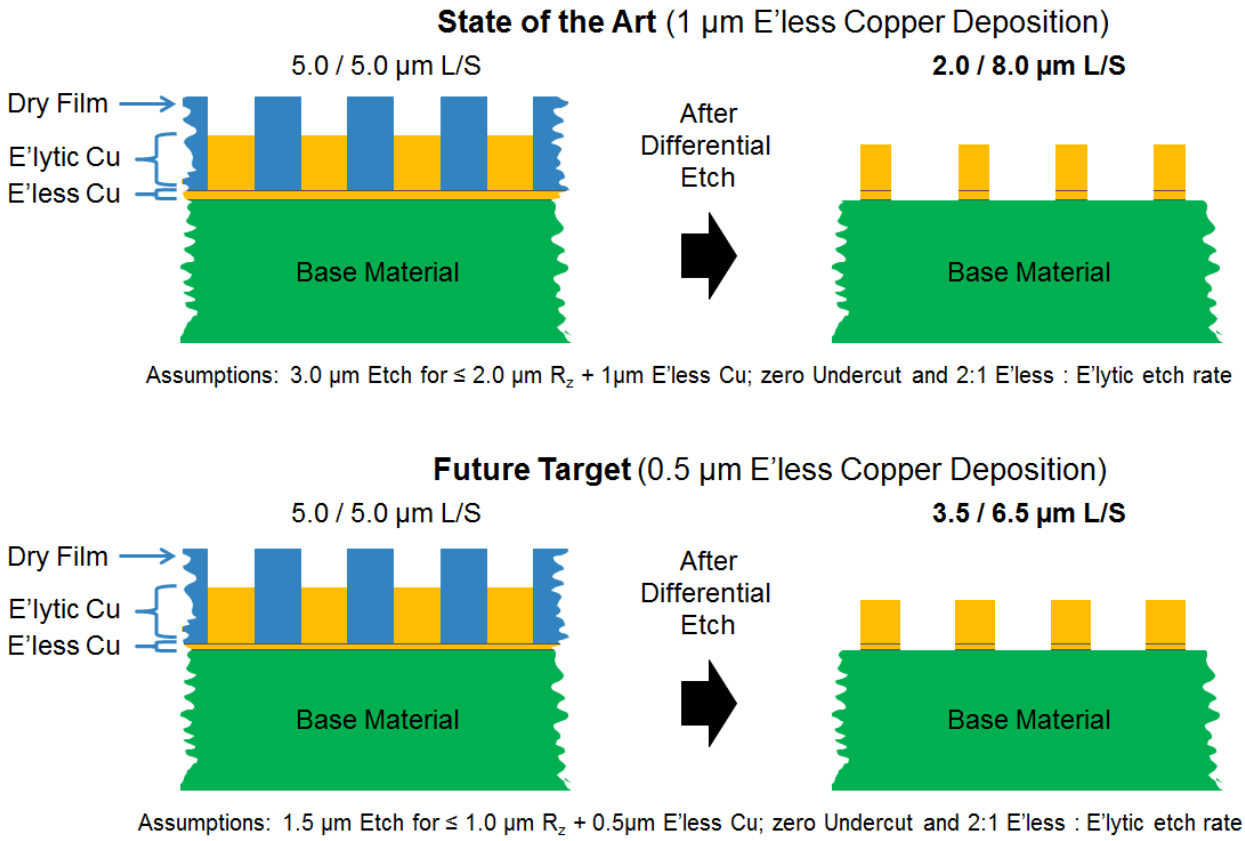

Figure 1: Impact of the electroless copper thickness on L/S resolution for IC substrates based on SAP technology

Throwing power is an essential requirement for electroless copper processes for enhanced fine line capability, but not the only one. Other relevant performance characteristics are the adhesion of dry films onto the electroless copper deposits and the adhesion of the deposited layer itself to the increasingly flattening bare laminates. Both factors directly affect the overall process yield rate.

The picture changes for HDI board manufacturing. The contemporary manufacturing technique for high-end HDI PCBs is panel plating in horizontal application mode. Leading manufacturers achieve approximately 35/35 µm L/S by applying standard 17 µm copper clad base materials and about 18-20 µm electrolytic copper plating. In order to reduce the etch depth required for the pattern formation and thus elevate the L/S resolution significantly down to 20/20 µm, manufacturers intend to change their current production process from panel to pattern plating and more precisely to the advanced modified semi additive process (AMSAP) technology (see figure 2). As a consequence, the existing manufacturing equipment and processes needs to be modified to cope with the new challenges that come along with this approach. The alternative, to push the panel plating technology to its limit by applying a thin copper clad base material – similar to the one used for AMSAP – and by the reduction of the electrolytic copper layer, is still limited in L/S resolution of above 20/20 µm and therefore no viable option.

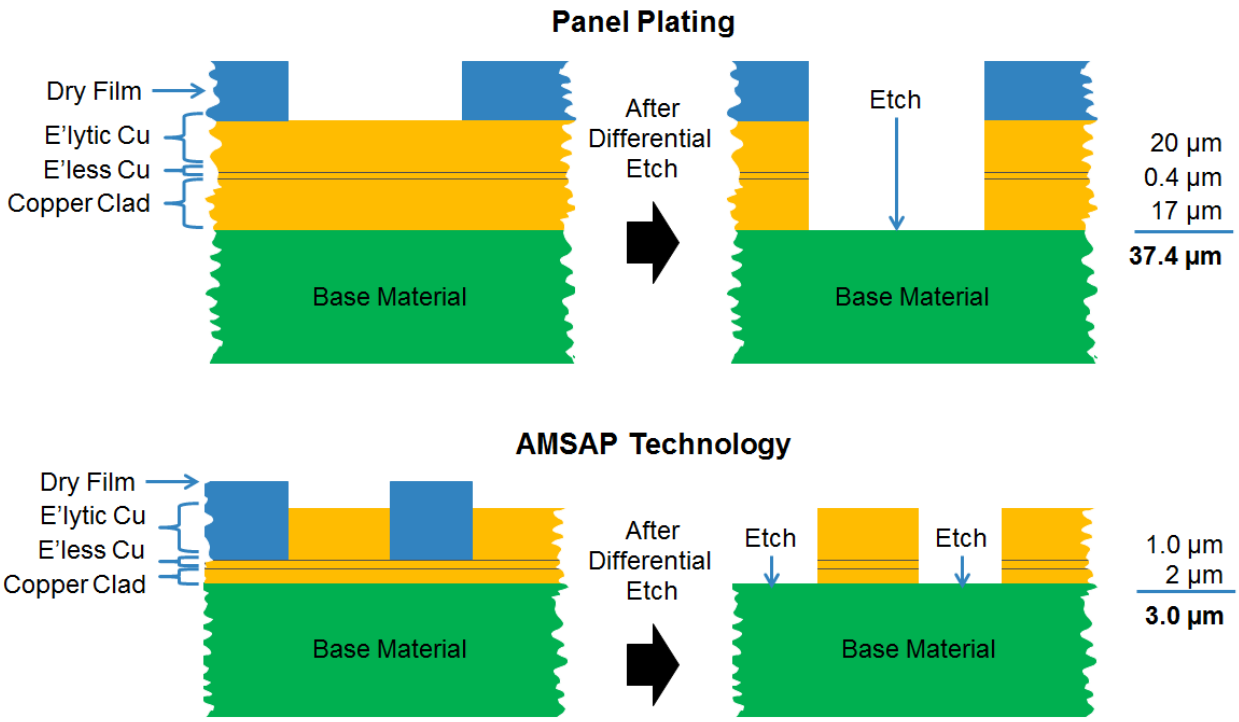

Figure 2: Comparison of the differential etch of panel plating versus AMSAP technology

As can be seen in figure 3, the dry film lamination and development steps within the AMSAP process are located directly after the electroless copper deposition in contrast to the panel plating process where the dry film is applied after the final electrolytic copper build-up. This difference in the process sequence has an impact to the required electroless copper deposition thickness.

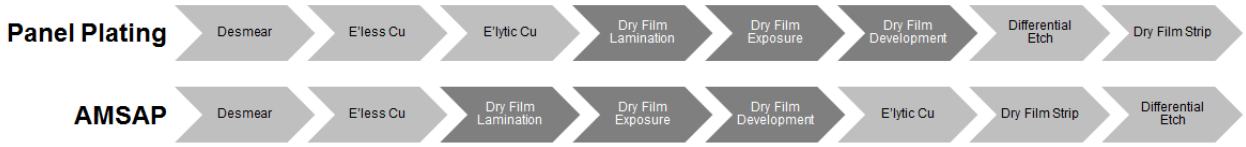

Figure 3: Process flow comparison of Panel Plating and AMSAP technologies

In case of a pattern plating scenario (AMSAP), 0.35 µm to 0.5 µm deposited on the panel surface are not sufficient to ensure a high production yield due to several copper etching steps prior to the via filling. The risk attached is voiding primarily at the bottom of the BMVs due to a thin electroless copper layer that might be completely etched away by the acid pre-treatment during the electrolytic plating process. To prevent this, manufacturers tend to increase the deposition thickness on the surface up to 1.0 µm or even more to increase the process safety, but to the disadvantage of a thicker copper layer that needs to be (differentially) etched.

Another, more cost-effective way is an electroless copper process with increased throwing power for process safety especially at the bottom of the BMVs, the most critical area for voiding. The required absolute electroless copper thickness in the BMV could be achieved while increasing the thickness at the surface only marginally compared to current copper thicknesses targeted in panel plating. As a result, the fine line resolution is improved.

The following table summarizes the main process requirements for electroless copper processes targeting the high-end IC substrate manufacturing as well as HDI application by AMSAP technology.

Table 1: Impact of selected electroless copper performance criteria on IC Substrates and HDI PCB

Selected Performance Criteria	Impact on IC Substrates (SAP)	Impact on HDI PCB (AMSAP)
Throwing Power	Fine line capability, yield	Fine line capability, yield
Dry Film Adhesion	Fine line capability, yield	Fine line capability, yield
Copper Adhesion on the Substrate (Internal Stress and Peel Strength)	Yield	-
Reliability	Yield	Yield

Throwing Power Measurement Methods

A reliable throwing power measurement method is essential for throwing power comparisons as performance criteria of different electroless copper baths. There is currently no industry standard available, which is why throwing power measurements and performance values of different players in the PCB industry are typically not comparable. To overcome this issue two reliable and standardized measurement methods based on cross sections and SEM evaluation are proposed which have been applied for all measurements shown in this paper. These two methods are required to measure the electroless copper thickness in different areas, namely on base materials respectively laminates (*method A*) and directly on copper (capture pad or copper clad on the surface; *method B*).

For the measurement of the electroless copper deposit thickness directly on the base material several factors need to be considered. Conventional throwing power measurement methods – as applied in the area of thick electrolytic copper – are not applicable for electroless copper. Etching and polishing for example potentially reduce the electroless copper thickness and a protection layer could form an intermetallic phase with the electroless copper, both leading to significant measurement errors of the actual layer thicknesses for deposits below 1.0 µm thickness. As a consequence, the sample preparation for the throwing power measurement *method A* excludes any etching or grinding and protection layer and the embedding resin must not induce any heat into the system during curing to avoid any smear of the electroless copper layer. After sample preparation, the throwing power can be calculated by thickness measurement of several different exposed spots in the BMV (see figure 4).

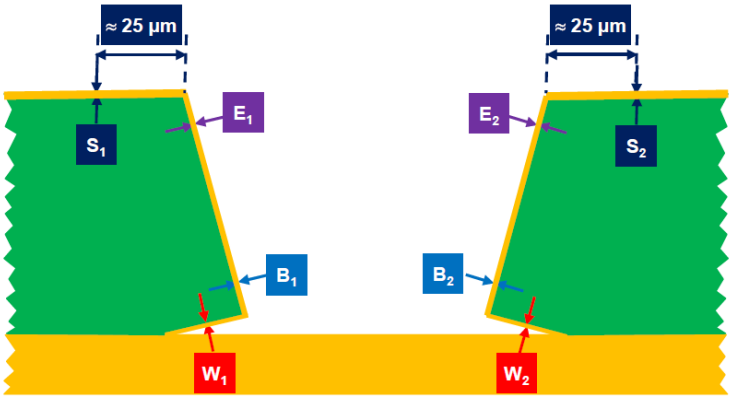

Figure 4: Throwing power measurement method A

The average electroless copper thickness per location and per image is calculated with i = 1,2 and N = 3:

Equation 1: Thickness measurement at different areas in the BMV

$$\overline{S_i} = \frac{1}{N} \cdot \sum_{n=1}^{N} S_{i,n} \qquad \overline{E_i} = \frac{1}{N} \cdot \sum_{n=1}^{N} E_{i,n} \qquad \overline{B_i} = \frac{1}{N} \cdot \sum_{n=1}^{N} B_{i,n} \qquad \overline{W_i} = \frac{1}{N} \cdot \sum_{n=1}^{N} W_{i,n}$$

$$i \in \{1;2\} \qquad N = 3$$

According to the required measurement points, the throwing power is calculated as follows:

Equation 2: Throwing power measurement at different areas in the BMV

$$TPW_S = \frac{\overline{W}_1 + \overline{W}_2}{\overline{S}_1 + \overline{S}_2} \cdot 100\% \qquad TPB_S = \frac{\overline{B}_1 + \overline{B}_2}{\overline{S}_1 + \overline{S}_2} \cdot 100\%$$

$$TPW_E = \frac{\overline{W}_1 + \overline{W}_2}{\overline{E}_1 + \overline{E}_2} \cdot 100\% \qquad TPB_E = \frac{\overline{B}_1 + \overline{B}_2}{\overline{E}_1 + \overline{E}_2} \cdot 100\%$$

In order to achieve a sufficient measurement resolution, it is mandatory to apply SEM for evaluation of the cross sections. The SEM settings used for the thickness measurement are standardized to increase the comparability between different locations and SEM types. Nevertheless, the measurement is still operator dependent but according to intensive testing of the method and statistical evaluations, the expected error is in an acceptable range. The application of focused ion beam (FIB) cutting would be a potential alternative to SEM, but due to the immense cost and throughput constraints for the measurement it is not a viable option.

The presented *method A* is suited to measure the throwing power directly on the base material but not on copper because etching or electro polishing is required in order to distinguish between different copper layers (e.g. electroless copper vs. the capture pad) and the method does not allow these preparation techniques. As described, etching or electro polishing attacks the electroless copper layer quite strongly, that is why two copper protection layers are electrolytically plated in *method B* before and after the electroless copper deposit to be measured (see figure 5). This build-up enables a stable electroless copper thickness even after etching and electro polishing and therefore provides an accurate method of electroless copper thickness measurement on the capture pad or on the copper clad surface.

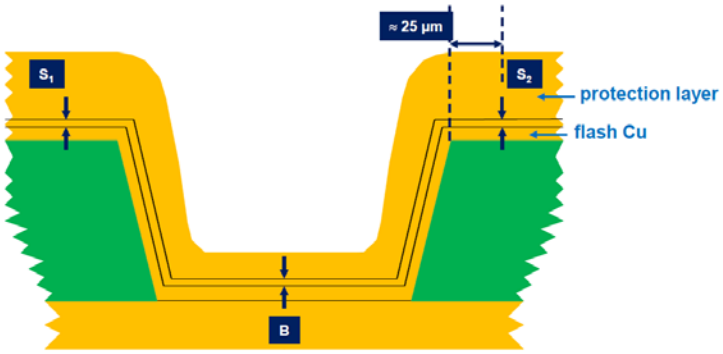

Figure 5: Throwing power measurement method B

The measurement of the throwing power is performed analogue to *method A* by cross sections and SEM images.

Throwing Power Performance

As discussed, throwing power is one of the most important performance criteria for next generation electroless copper baths for both, IC substrates as well as HDI panels. On the one hand, a minimized electroless copper layer thickness on the surface of the laminate is required in order to reduce the differential etch and increase the achievable resolution. The electroless copper thickness in the wedge of the BMV on the other hand is limited to a certain thickness because of conductivity requirements of the subsequent via filling process step. A solution for these contradicting requirements is a high throwing power electroless copper process. Currently, throwing power values of approx. 30% in the wedge and 70% on the capture pad of the BMV represent the typical performance in the industry for vertical IC substrate manufacturing whereas future design rules will require minimum 70% throwing power in the wedge and 100% on the capture pad. For horizontally produced HDI boards in panel plating, the throwing power on the capture pad is approximately 30% and the requirements will increase due to the postulated technology shift to AMSAP.

The throwing power performance is not only a function of the electroless copper bath, but also of the solution exchange influenced by the type of plating equipment, the aspect ratio (AR) of the BMV and the wedge formation respectively the AR of the wedge. Nevertheless, the chemical formulation and the process parameters of an electroless copper bath significantly influence the throwing power performance.

Figure 6 shows a typical BMV (60 µm width × 40 µm depth) on a standard build-up film as widely used in mass production processed with *E'less Copper IC* – a new, vertical electroless copper bath developed for high-end IC substrate manufacturing – in a mass production environment. The aspect ratios of the wedges are 1 : 0.3 (8 µm width × 2 µm depth). By applying the measurement *method A* as described above, the throwing power is approx. 80% in the wedges.

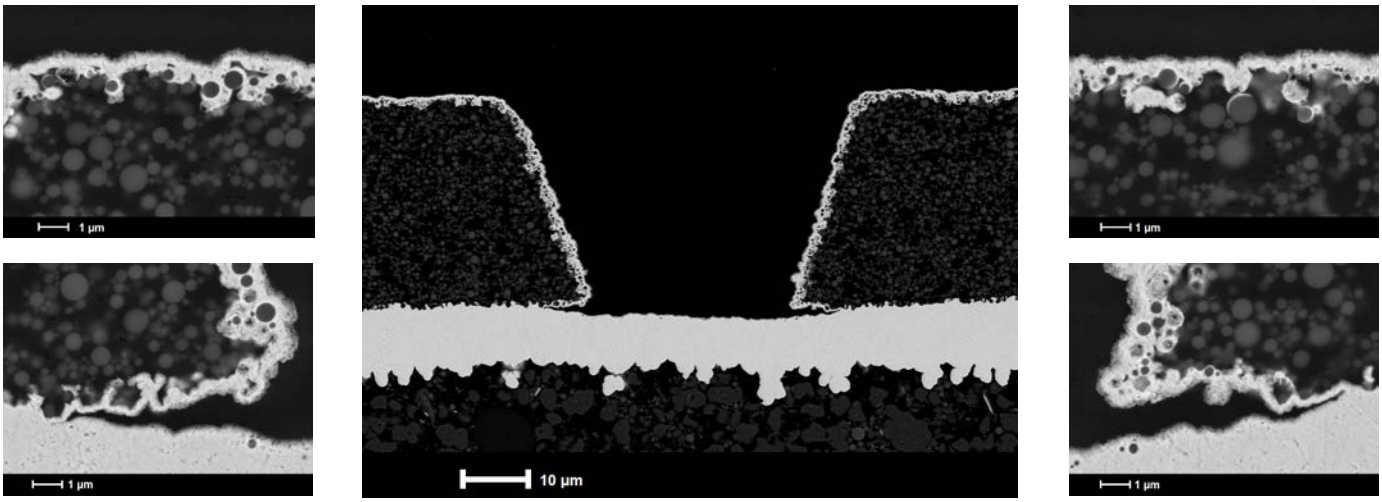

Figure 6: SEM Images of a BMV (60 × 40 µm) on standard build-up film treated with E'less Copper IC

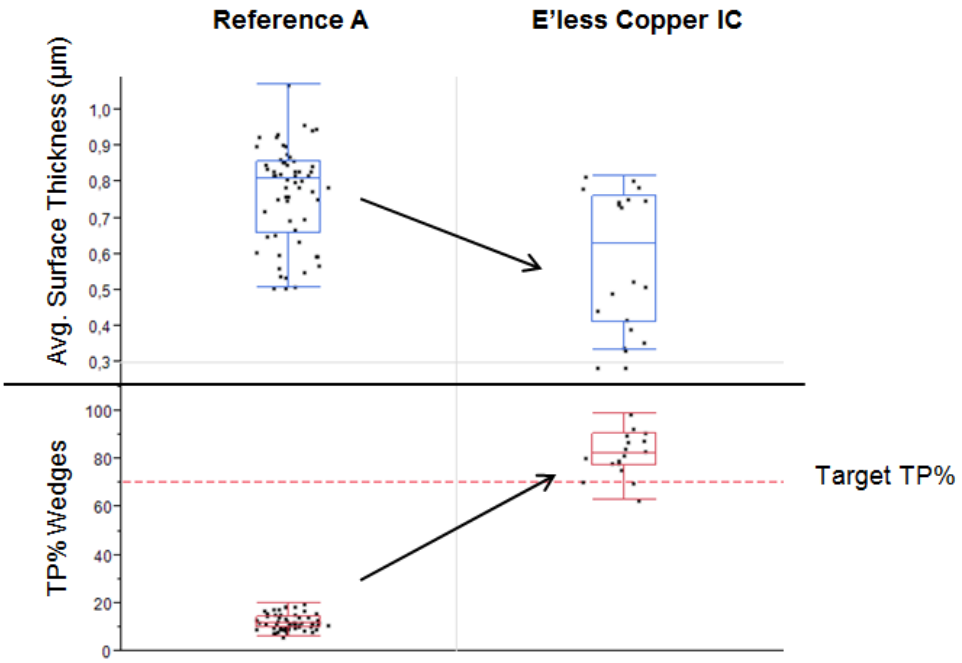

Figure 7: Statistical evaluation of a comparison line test of E'less Copper IC and the reference bath

Figure 7 illustrates a statistical evaluation of a throwing power comparison line test of the new *E'less Copper IC* and a reference bath established in mass production at several IC substrate manufacturers. The throwing power was evaluated using *method A* according to TPW_S. As can be seen in the lower part of the chart, the new electroless copper bath outperforms the reference system in terms of throwing power. The new electroless bath achieved a significantly higher absolute and relative deposition in the BMV wedges which leads to a throwing power of approx. 70 – 80 %, whereas the reference achieves a throwing power of about 20%.

Throwing power measurements and comparison tests for the recently developed horizontal *E'less Copper HDI* are shown in figures 8 and 9. The new electrolyte was compared with two horizontal reference systems using analysis *method A* with

throwing power evaluation TPB_E in horizontal mass production equipment, which is the standard production environment for high-end HDI manufacturing. Reasons for this are the constant process conditions for each panel and the excellent fluid exchange especially in BMVs. During the test, the electroless copper thickness at the top or entrance of the BMVs was comparable for all three candidates thereby fluctuating around 350 nm whereas the absolute thickness at the bottom of the BMVs was significantly higher for the new bath *E'less Copper HDI* compared to the reference systems. As a consequence, the calculated throwing power (approx. 73%) is higher for the new bath.

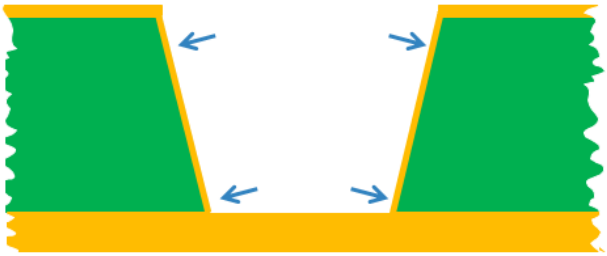

Figure 8: Throwing power measurement method A according to TPB_E and the test vehicle

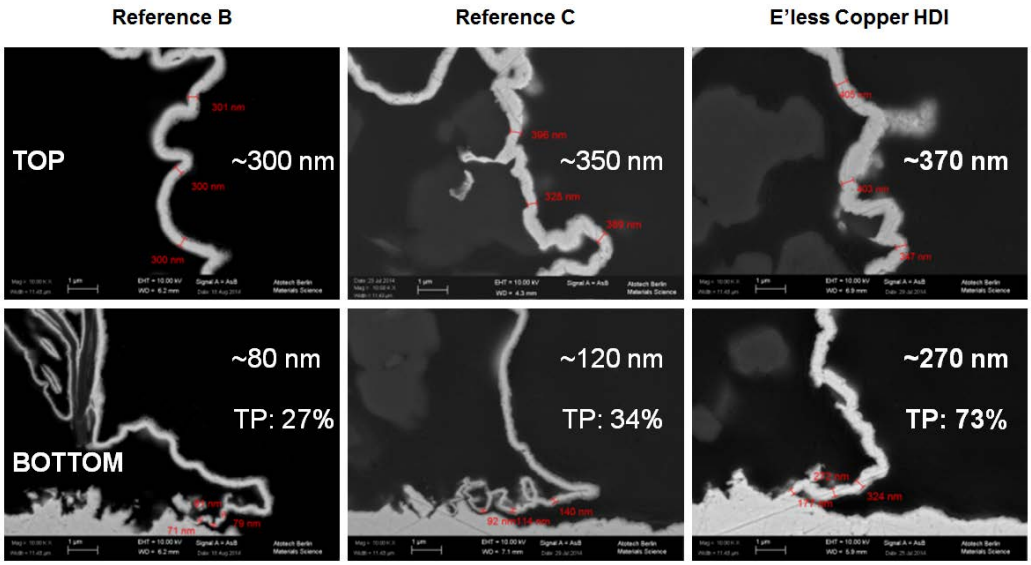

Figure 9: Throwing power comparison of E'less Copper HDI and two reference systems

In another test throwing power measurement *method B* was applied to evaluate the throwing power directly on the capture pad. The electroless copper layer of *E'less Copper HDI* in between the electrolytic copper protection layers becomes visible after electro polishing (see figure 10). A similar throwing power (approx. 74%) compared to the result using *method A* at the bottom of the BMV was achieved.

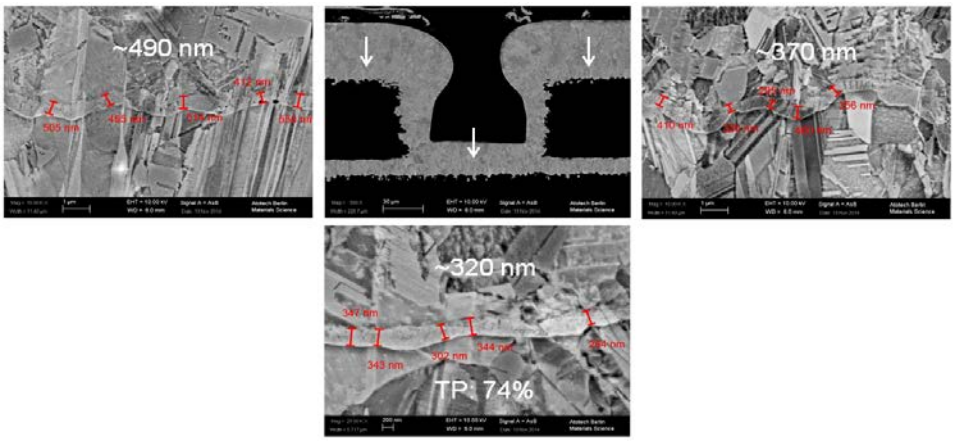

Figure 10: Throwing power measurement of E'less Copper HDI applying method B

Dry Film Adhesion Performance

The application of the dry film during pattern plating is a critical factor for the overall yield of the manufacturing process. In order to ensure an acceptable yield, the adhesion of the dry film on the electroless copper layer needs to be sufficient to survive the subsequent process steps of the pattern plating. Insufficient adhesion could otherwise lead to opens and shorts resulting in yield loss. Several parameters are influencing the dry film adhesion and need to be considered. Two of the most important factors are firstly the lamination conditions of the dry film and secondly, the surface morphology of the electroless copper layer. For an optimal result, the lamination parameters need to be optimized to the specific electroless copper deposit.

Dry film adhesion on the new *E'less Copper IC* bath is demonstrated by using the "line adhesion test" on electroless copper deposits plated on lower CTE state-to-the-art build-up film as currently used in mass production. After copper surface treatment with H_2SO_4, production series dry film line structures with a width of 6 µm respectively 8 µm are evaluated after exposure and development by a UV microscope. The percentage of dry film lines that survived the development process is an indicator for the adhesion on the tested electroless copper deposits. As illustrated in figure 11, the new electroless copper process outperforms the reference system in dry film adhesion for both repetitions of the test. Nearly all 8 µm dry film tracks are in good shape after the development process whereas the 8 µm dry film lines for the reference process are visibly damaged. The result for the 6 µm dry film tracks with *E'less Copper IC* in this test set-up is not perfect, but still significantly better than the reference that failed completely in both test runs.

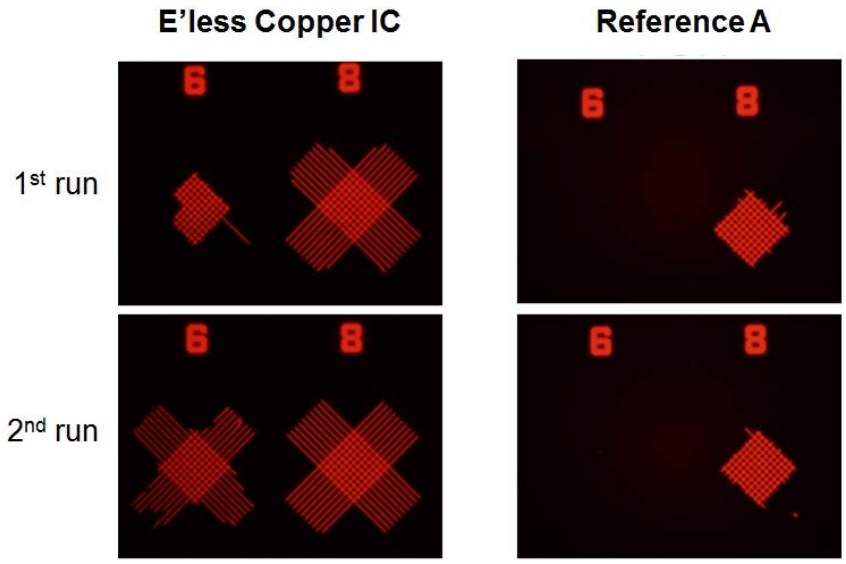

Figure 11: Production series dry film adhesion test of two different electroless copper deposits on lower CTE standard build-up film

Dry film adhesion tests for *E'less Copper HDI* generated in mass production equipment are currently in progress and therefore can not be discussed in this paper. However, all initial results showed similar excellent performance as for *E'less Copper IC.*

Electroless Copper Adhesion on the Substrate

New substrates introduced to the market for application with SAP technology are becoming increasingly smoother because of the demand for higher circuitry densities and signal frequencies. The influence of the substrate surface constitution on the adhesion of the electroless copper layer via mechanical anchoring and chemical interface bonding is significant. Weak adhesion of the copper layer could lead to spontaneous delamination failures (blistering) and line peel-offs that are not acceptable for customers in mass production. Internal stress characteristics of the electroless copper layer have been shown to significantly impact the tendency of a copper layer to delaminate from the substrate [1, 2]. The occurrence of compressive stress in the layer correlates to the probability of buckle driven delamination, namely blistering, whereas tensile stress suppresses the likelihood of blistering. The internal stress characteristics of the copper layer deriving from *E'less Copper IC* have been analyzed using the in situ X-ray diffraction method (XRD). As can be seen in figure 12 the internal stress is slightly more tensile compared to the reference electroless copper bath, one of the current standards in the market. The copper layer is therefore perfectly suited to adhere on the substrate surface without any blistering issues for a representative deposition thickness range.

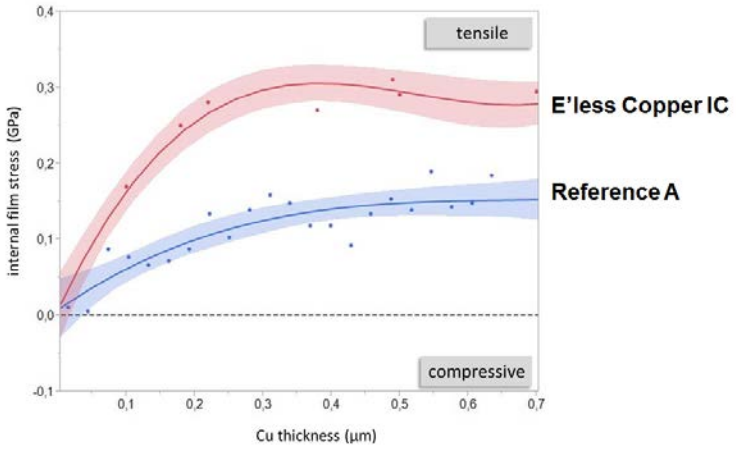

Figure 12: Plot of the internal stress of copper films deposited from two different electroless copper baths against deposit thickness, as measured by in situ XRD [Measurements in cooperation with Mt. Allison University, Canada]

The blistering tendency of the copper layer is not only related to the internal stress characteristics but also to the peel strength of the layer. The peel strength is a well-known performance criterion in the industry and can be described as the clamp force of the copper layer to the substrate. Broadly speaking, blistering occurs when the delamination force due to the internal stress characteristics exceeds the clamp force of the layer. The peel strength is dependent on the chemical bonding of the copper layer on the surface and the mechanical anchoring via the surface roughness. The latter is highly influenced by the conditions that are applied in prior process steps especially in the desmear and the lamination process of the film. Mass production comparison tests of *E'less Copper IC* with the reference system on standard build-up film showed that the peel strength performance of the new bath is on the same very good level as the reference bath (cf. figure 13). This result could be confirmed also on several other relevant laminates including low CTE laminates of latest generation.

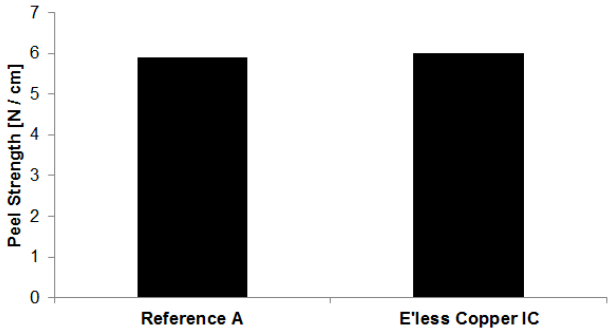

Figure 13: Peel strength results after acid copper plating on standard build-up film Annealing Parameter.: 1h at 130°C after e'less copper, 1h at 180°C after electrolytic copper

Reliability

During the development and mass production qualification, both new electroless copper baths have been intensively tested with all standard reliability tests established in the market (see table 2 below).

Table 2: Summary of reliability tests for E'less Copper IC and E'less Copper HDI

Test	Conditions	Result
Solder shock test (SST)	6 × 288°C solder float	Passed
Interconnect stress test (IST)	From RT up to 150°C, resistance increase in the power circuit < 3%	2000 cycles passed
"Comfort 40" online temperature cycle test (TCT)	-40°C / 125 °C, 15 min / 15 min, resistance increase in the power circuit < 3 %	1000 cycles passed
Quick Via Pull (QVP)	75, 100, 125 and 150 µm diameter BMVs	Passed

The following figure illustrates the detailed IST and TCT test results for *E'less Copper HDI* as achieved at a mass production test.

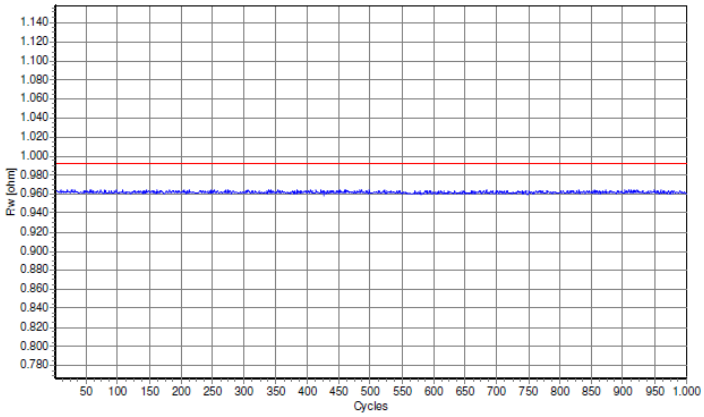

Figure 14: TCT result (1000 cycles passed) of E'less Copper HDI

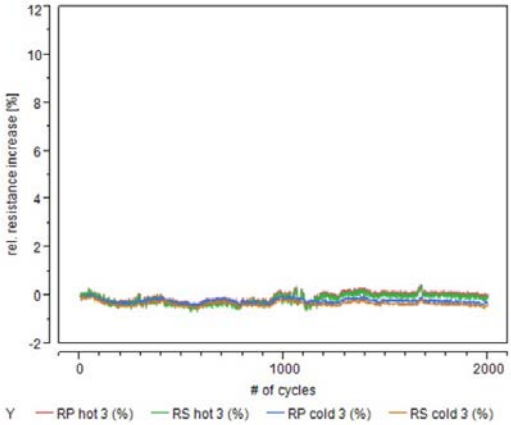

Figure 15: IST result (2000 cycles passed) of E'less Copper HDI

Summary

Two new electroless copper baths have been developed to cope with upcoming miniaturization challenges in the high-end IC substrate segment as well as in the evolving HDI board market. The main challenge to be overcome is the reduction of the differential etch in the pattern plating process by decreased electroless copper thickness on the surface of the build-up layer. To this end, several requirements need to be fulfilled to ensure a safe and high yield production.

First of all, the throwing power performance of *E'less Copper IC* and *E'less Copper HDI* especially in the wedges respectively at the bottom of the BMVs is crucial for the via-filling performance due to conductivity requirements. Two reliable throwing power measurement methods have been introduced and throwing power results presented in this paper show that the new electroless copper baths constantly achieve significantly better throwing power performance compared to the reference systems that are industry standards in the respective markets.

A minimum target thickness of the electroless copper layer in the BMV (wedges) is therefore ensured while the thickness on the surface can be reduced for improved L/S resolution. Secondly, the adhesion of the copper layer on the bare laminate is a basic requirement for the high-end IC substrates manufacturing process. Favorable internal stress characteristics of the copper layer of the *E'less Copper IC* bath combined with excellent peel strength results ensure a reliable and strong adhesion of the copper layer on the resin surface. Thirdly, dry film adhesion and differential etching are key process steps for high yield manufacturing. The surface morphology of the *E'less Copper IC* layer enables improved mechanical anchoring of the dry film compared to the reference system and dry film adhesion data for *E'less Copper HDI* is under evaluation. Both electroless copper baths were thoroughly tested for industry standard reliability requirements and achieved excellent results.

References

[1] Simon Bamberg et al. "Stress/strain in electroless copper films: analysis by in-situ X-ray diffraction and curvature methods", 9th International Conference on Device Packaging, Arizona USA, 2013.

[2] Tobias Bernhard, Simon Bamberg, Frank Brüning, Ralf Brüning, Laurence J. Gregoriades, Tanu Sharma, Delilah Brown, M. Klaus, Christian Genzel "Analysis of stress/strain in electroless copper films", 46th International Symposium of Microelectronics, Orlando, 2013.

High Throw Electroless Copper – Enabling new Opportunities for IC Substrates and HDI Manufacturing

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Agenda

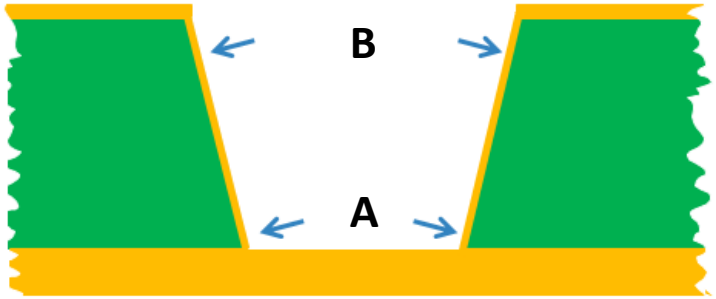
- Motivation: Miniaturization in the PCB industry
- Electroless Copper Performance Criteria
  - Throwing Power Measurement Method
  - Throwing Power Performance
  - Dry Film Adhesion
  - Copper Adhesion on the Substrate
  - Reliability
- Summary

What's Throwing Power?

http://www.theole

http://www.rantsports.com/nfl/files/20

http://p5.focus.de/img/fotos/origs4276660/7865445128-w630-h354-o-q75-p5/neuer-abwurf.jpg

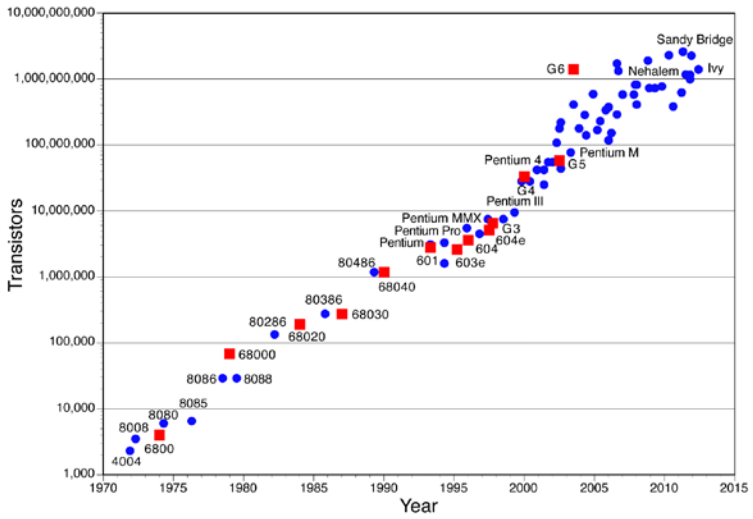


$$TP = \frac{Avg.\ Cu\ Thickness\ A}{Avg.\ Cu\ Thickness\ B}$$

Miniaturization in the PCB Industry

Miniaturization

Moore's Law (1975): *"The number of transistors on a chip will double every two years"*

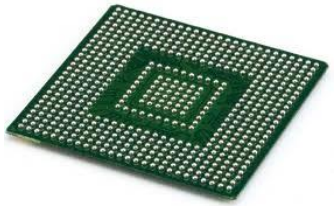


http://education.mrsec.wisc.edu/SlideShow/images/computer/Moores_Law.png

Implications for PCB

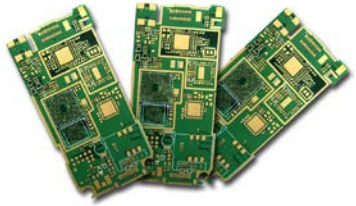
Lines and Spaces

IC Substrates



9 / 12 µm → **below 10/10 µm**

High-end HDI



35 / 35 µm → **20 / 20 µm**

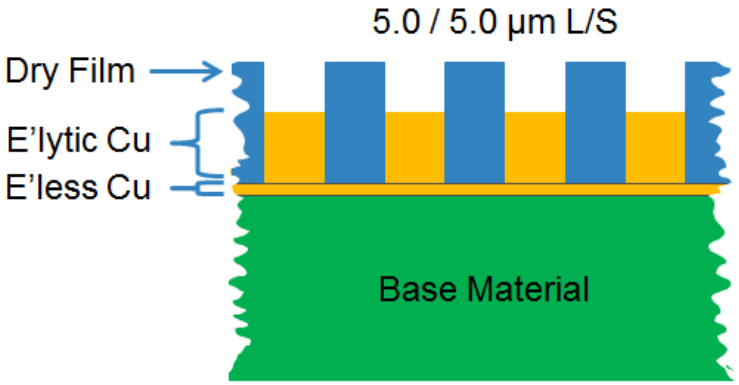
Finer Lines and Spaces

Reduced Differential Etch

- **Reduced copper thickness** (Cu Clad, e'less Cu, e'lytic Cu)
- **Reduced surface roughness** (especially R_z) of the base materials

Simulation of 5/5 Lines and Spaces (SAP)

State of the Art (1 µm E'less Copper Deposition)



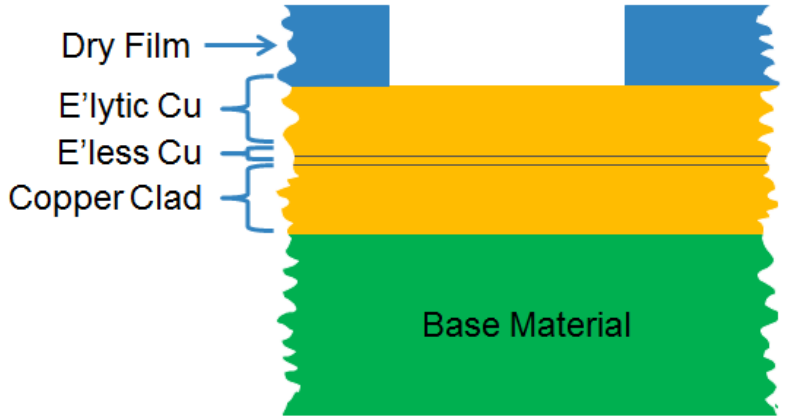
Assumptions: 3.0 µm Etch for ≤ 2.0 µm R_z + 1µm E'less Cu; zero Undercut and 2:1 E'less : E'lytic etch rate

- **Main contributors for reduced differential etch**
  - Reduced e'less Cu thickness (1.0 µm to 0.5 µm)
  - Reduced surface roughness (2.0 µm to 1.0 µm R_z)
- **Inevitable requirements**
  - Increased throwing power of the e'less Cu
  - New laminates

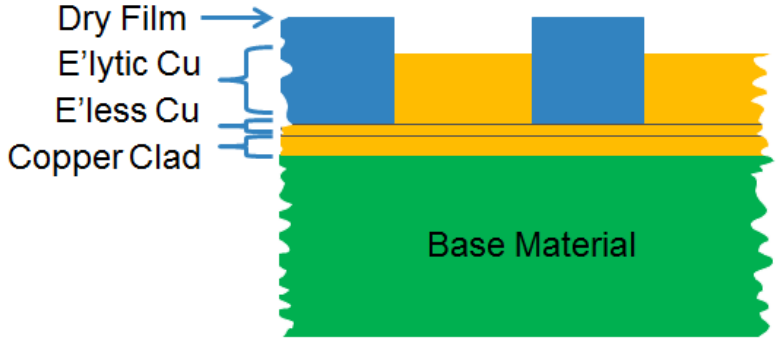
*SAP = Semi-Additive Process

Panel Plating vs. Advanced Modified SAP

Panel Plating

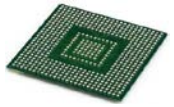


AMSAP Technology



- **Main contributors for reduced differential etch**
  - Technology change (panel plating to AMSAP)
  - Reduced copper clad thickness
- **Inevitable requirements**
  - New base materials
  - Increased throwing power of the e'less Cu

Electroless Copper Performance Criteria

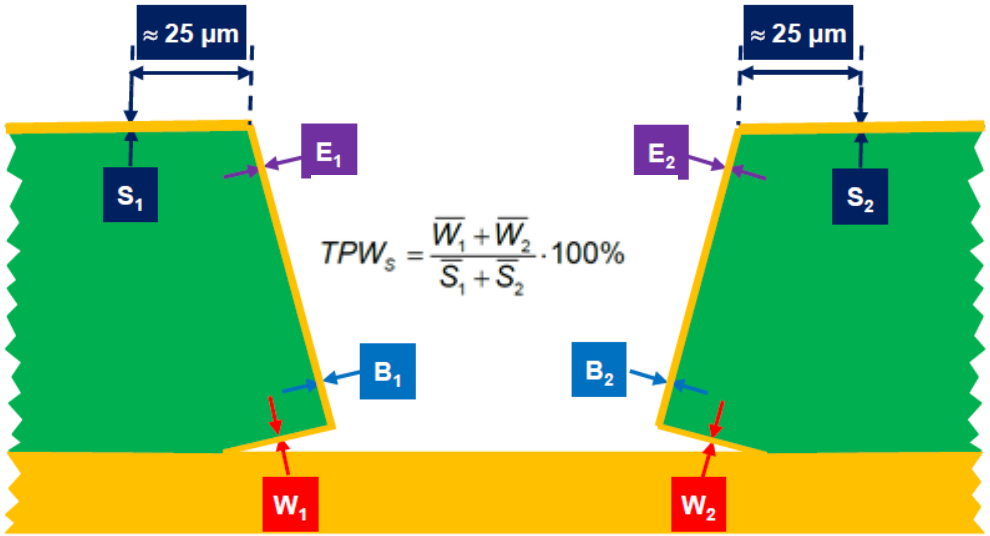
Selected Performance Criteria	Impact on IC Substrates (SAP) 	Impact on HDI PCB (AMSAP) 
Throwing Power	**Fine line capability, yield**	**Fine line capability, yield**
Dry Film Adhesion	Fine line capability, yield	Fine line capability, yield
Copper Adhesion on the Substrate (Internal Stress and Peel Strength)	Yield	-
Reliability	Yield	Yield

E'less Copper IC

E'less Copper HDI

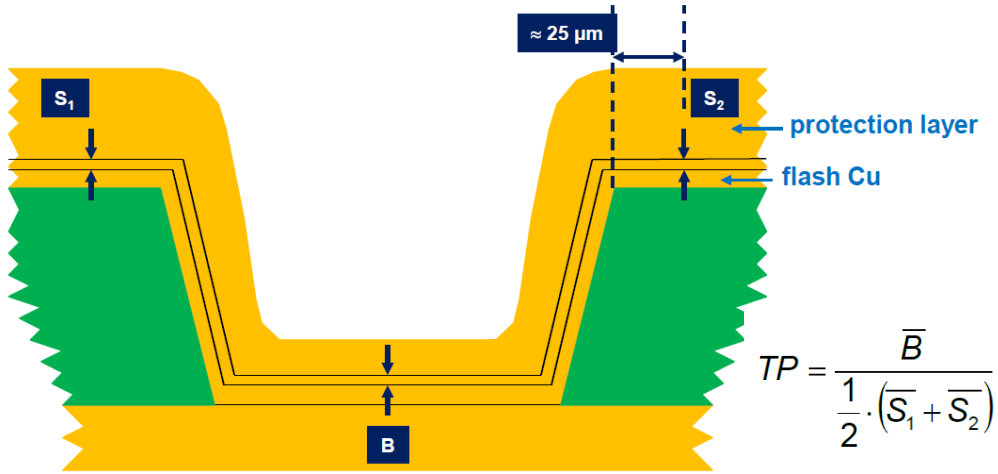
Throwing Power of Electroless Copper: Measurement Methods

Method A



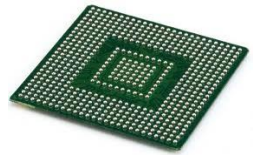
- **E'less Cu directly on base materials**
- No etching or electro polishing
- Measurement by SEM (standardized)
- Special embedding resin

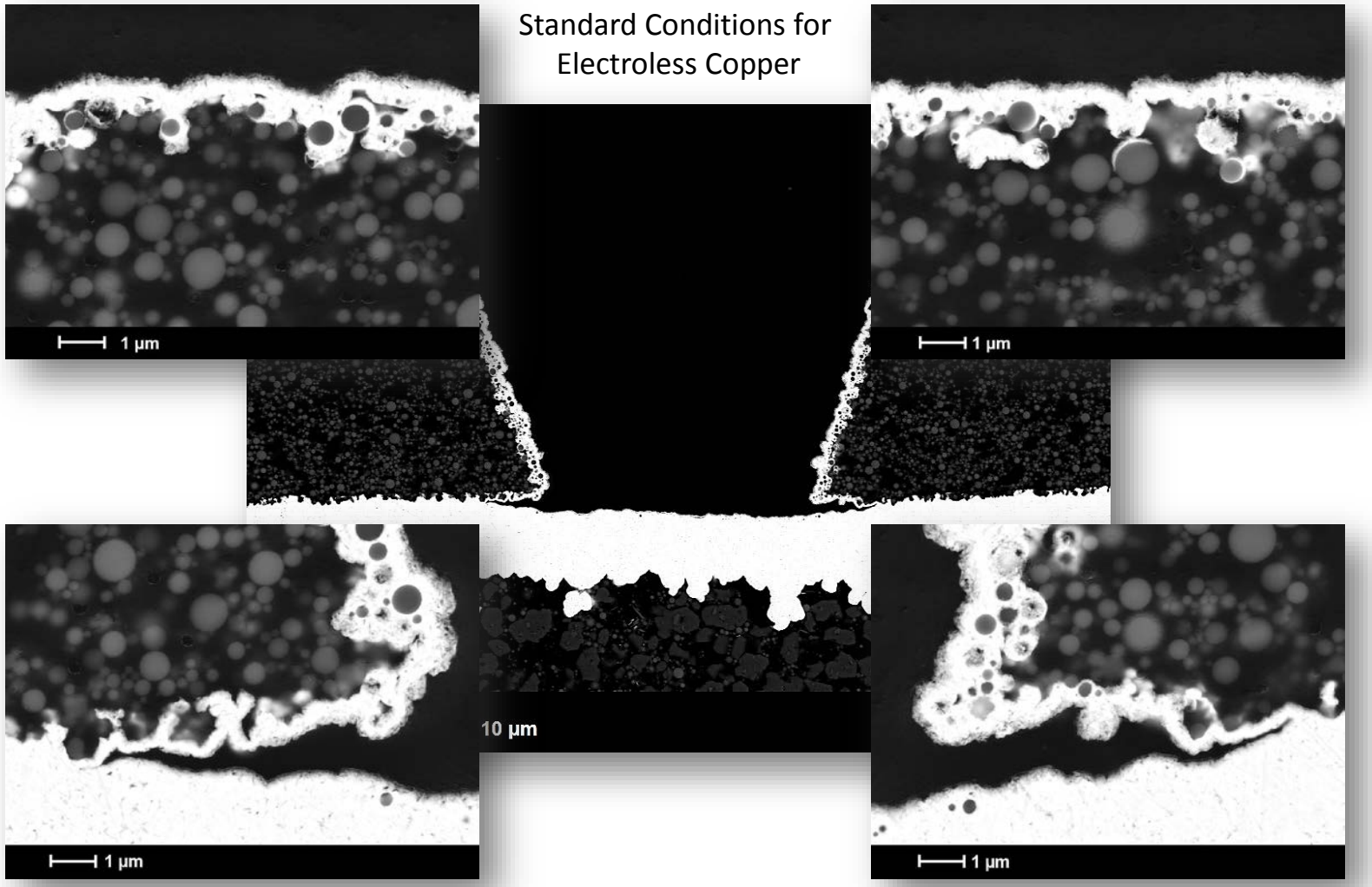
Method B



- **E'less Cu on Cu clad or capture pad**
- Etching and electro polishing possible
- Measurement by SEM (standardized)

Throwing Power Performance (IC)





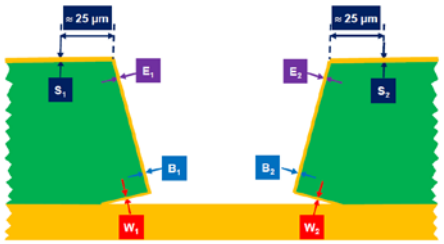
Throwing Power:

- Surface: 0.30 µm Abs.
- Wedge: 0.25 µm Abs.

TP: >80%

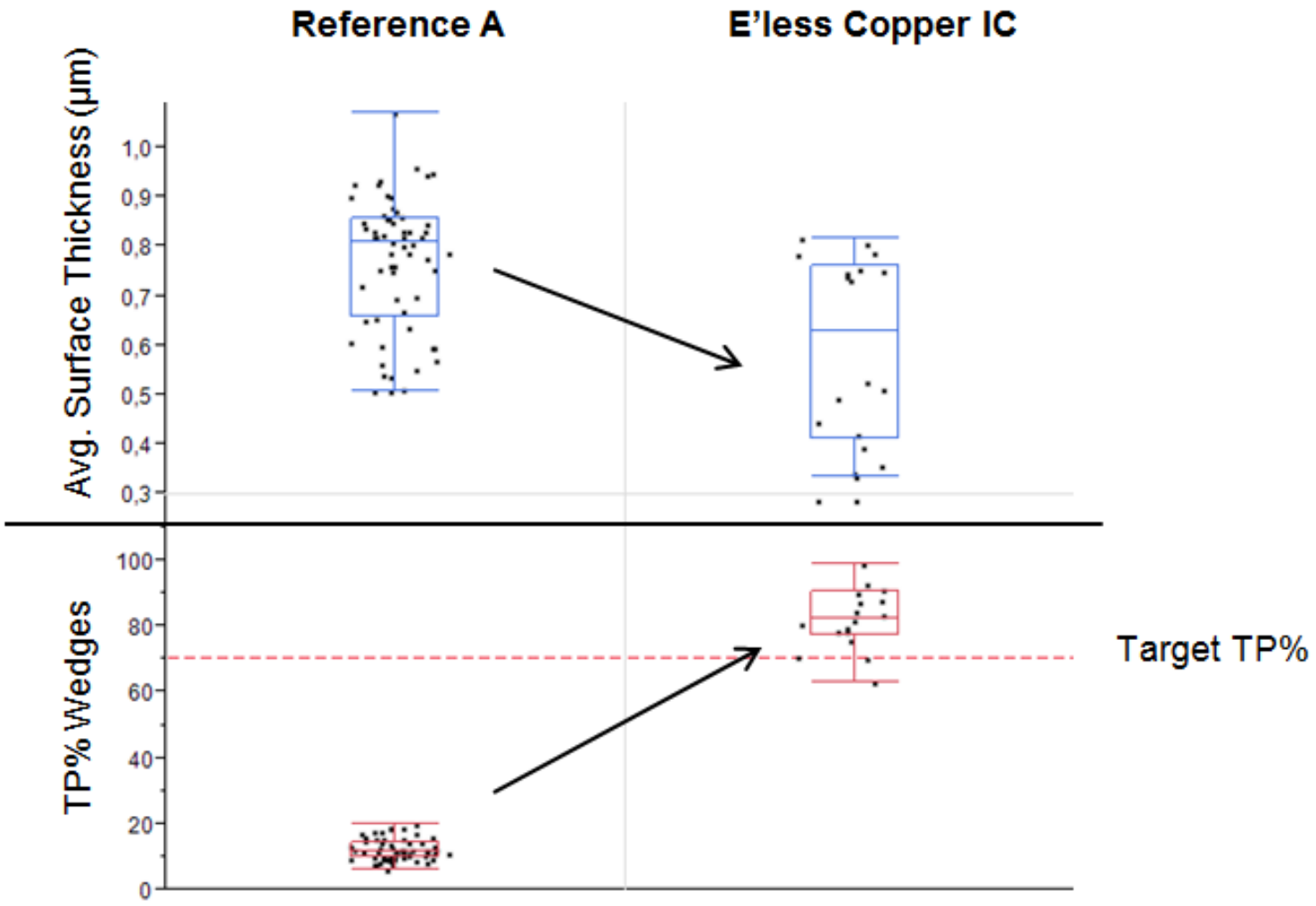
Throwing Power measurement on standard build up film 60:40 µm BMV
Customer Qualification

$$TPW_S = \frac{\overline{W_1} + \overline{W_2}}{\overline{S_1} + \overline{S_2}} \cdot 100\%$$



FORWARD THINKING
FOR TOMORROW'S TECHNOLOGY

Throwing Power Performance (IC)

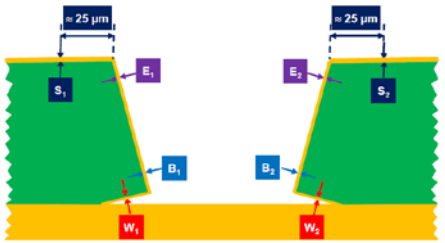


Throwing Power:

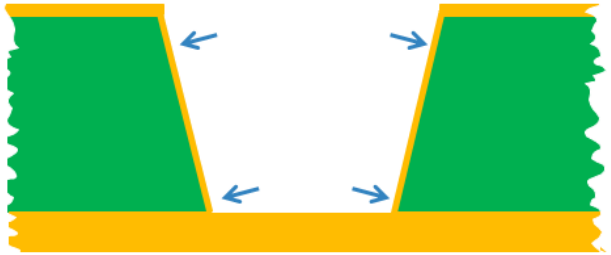
- The new E'less Cu IC outperforms the reference system **(~80% TP vs. ~20%)**

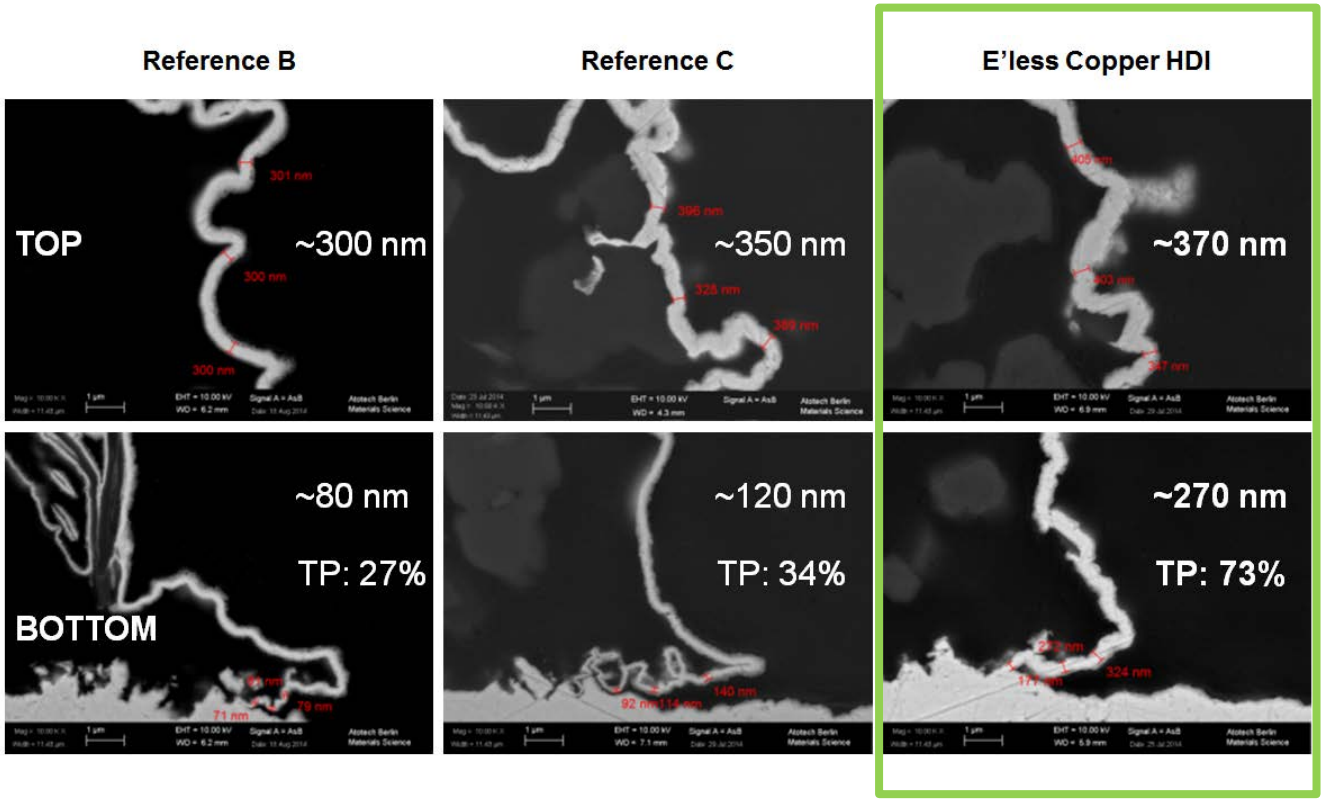
Throwing Power measurement on standard build up film 60:40 µm BMV Company TechCenter, Japan

$$TPW_S = \frac{\overline{W_1} + \overline{W_2}}{\overline{S_1} + \overline{S_2}} \cdot 100\%$$



Throwing Power Performance (HDI)



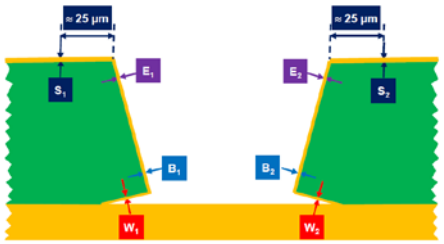


Throwing Power:

- The new E'less Cu HDI outperforms both reference systems **(~70% TP vs. ~30%)**

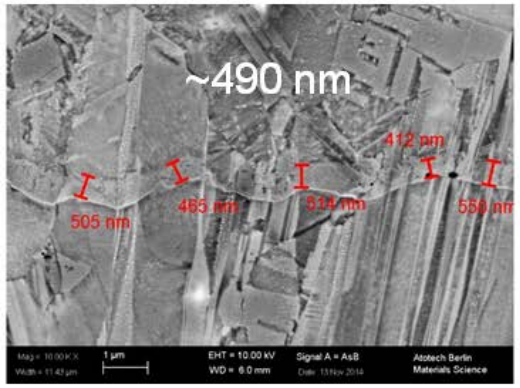
Throwing Power measurement on
110:60 µm BMV
Company TechCenter, Korea

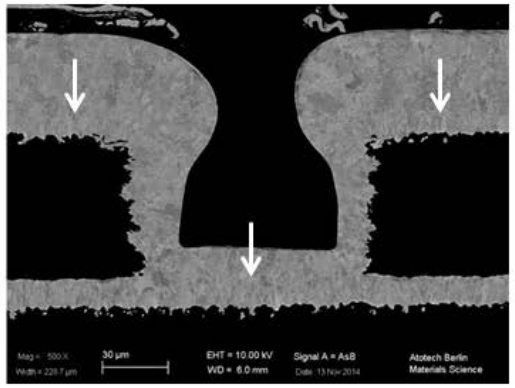
$$TPB_E = \frac{\overline{B_1} + \overline{B_2}}{\overline{E_1} + \overline{E_2}} \cdot 100\%$$

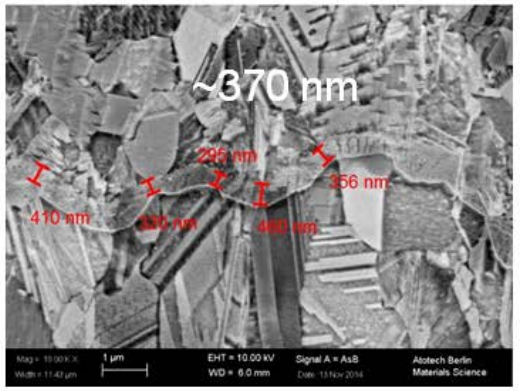


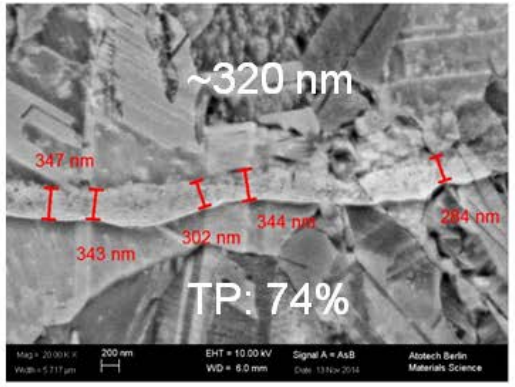
FORWARD THINKING
FOR TOMORROW'S TECHNOLOGY

Throwing Power Performance (HDI)







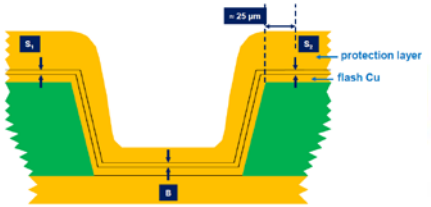


Throwing Power:

- Good throwing power results achieved on BMV sidewalls (method A) can be repeated on the capture pad (method B)

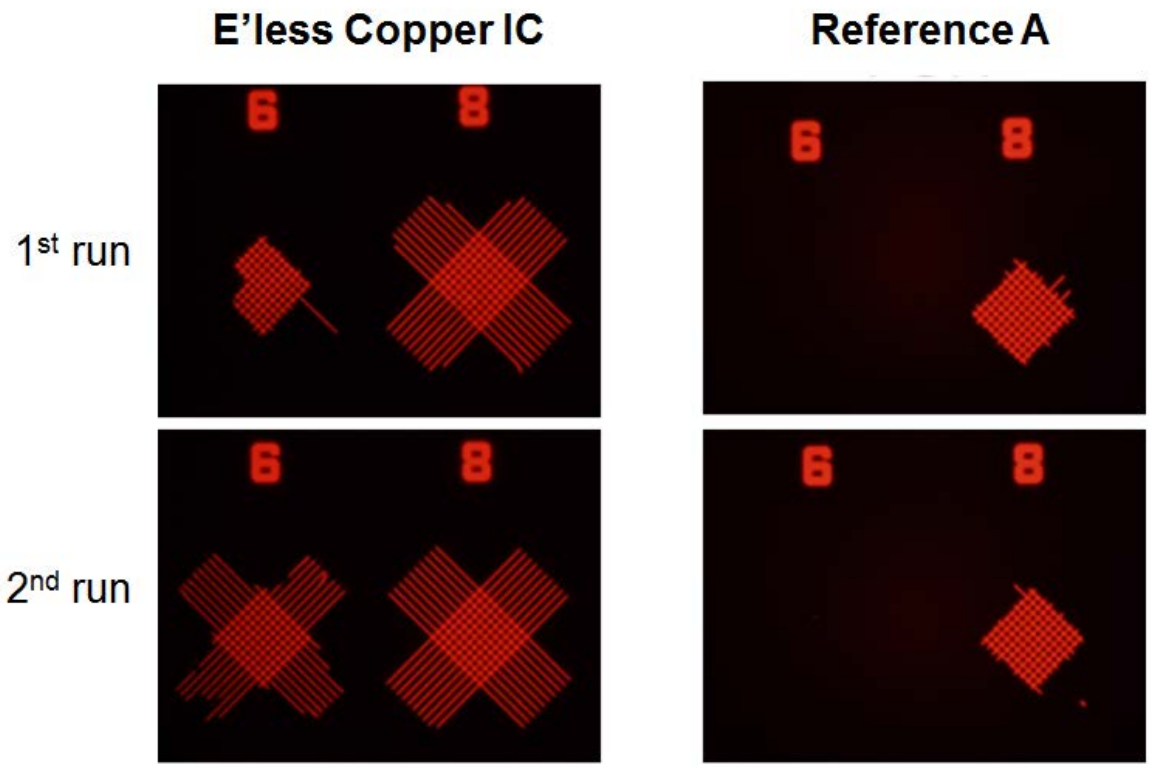
Throwing Power measurement on 100:60 µm BMV
Company TechCenter, Korea

$$TP = \frac{\overline{B}}{\frac{1}{2}\cdot\left(\overline{S_1}+\overline{S_2}\right)} \times 100\%$$



Dry Film Adhesion – Line Test (IC)

Evaluation by UV microscope



Dry Film Adhesion:

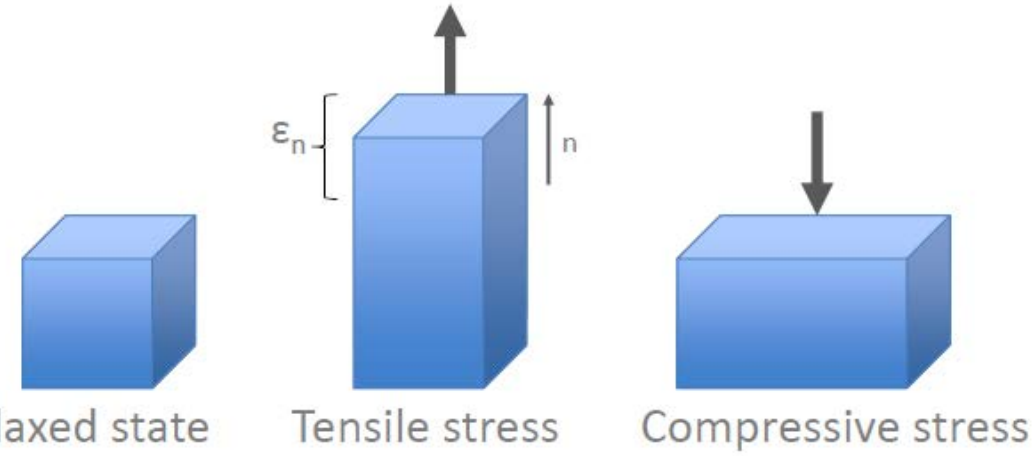
- E'less Copper IC significantly outperforms reference A in dry film adhesion performance

Substrate = Lower CTE State-of-the-Art Build-Up Film
Production series Dry film
Cu thickness: 0.8 µm
Copper surface treatment with H_2SO_4

Copper Adhesion on the Substrate (IC)

Internal Stress Evaluation by in-situ XRD-Measurement*

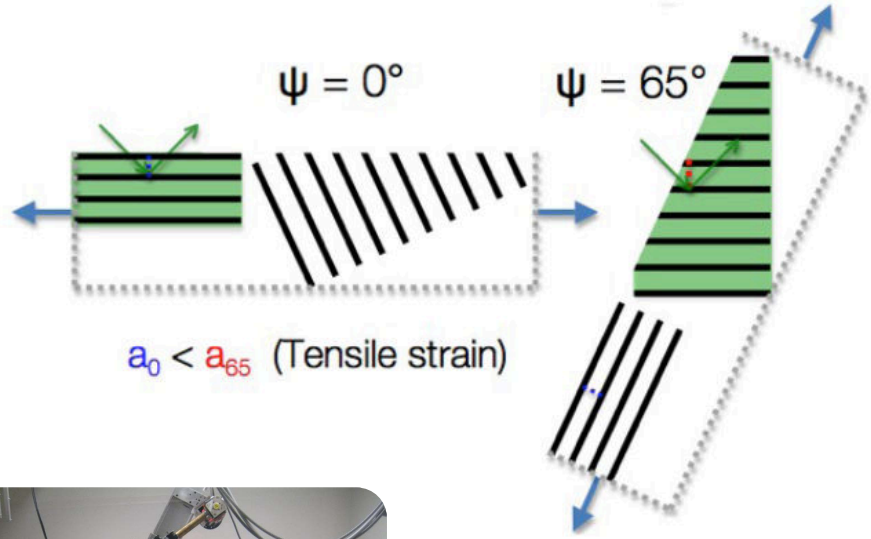
Strain and Stress in Polycrystalline Materials

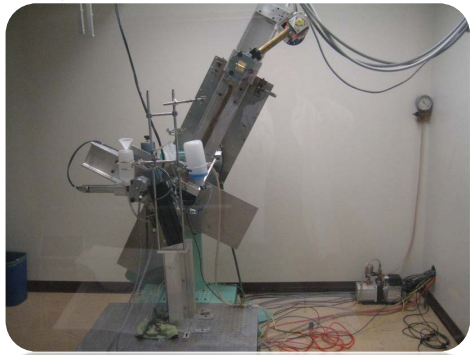


Elastic strain along axis n is, $\epsilon_n = \frac{d_n - d_0}{d_0}$ where

d_n is lattice spacing in n direction under stress and

d_0 is lattice spacing in absence of stress

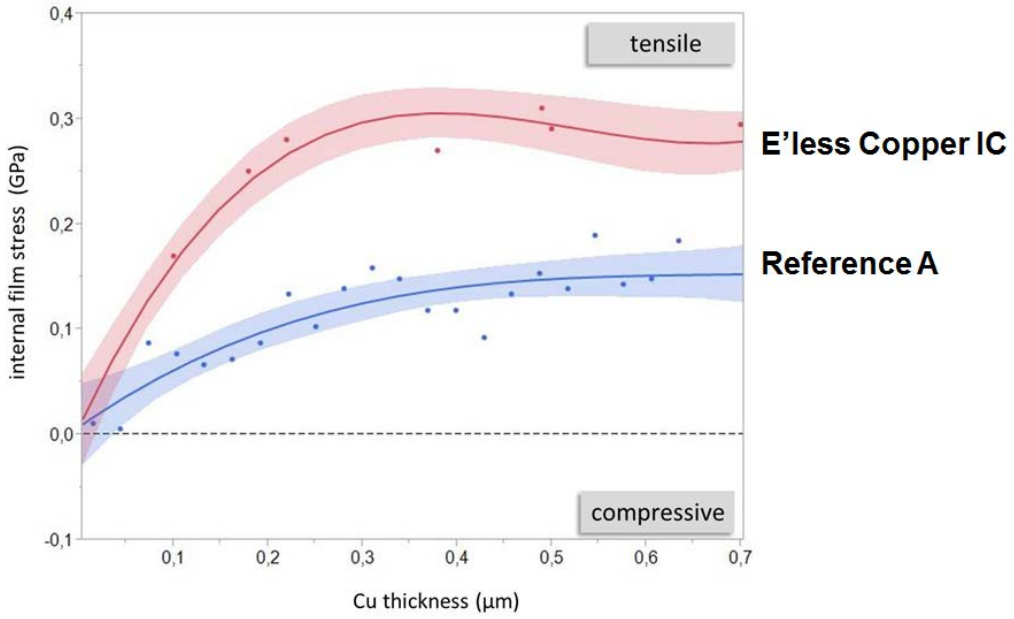




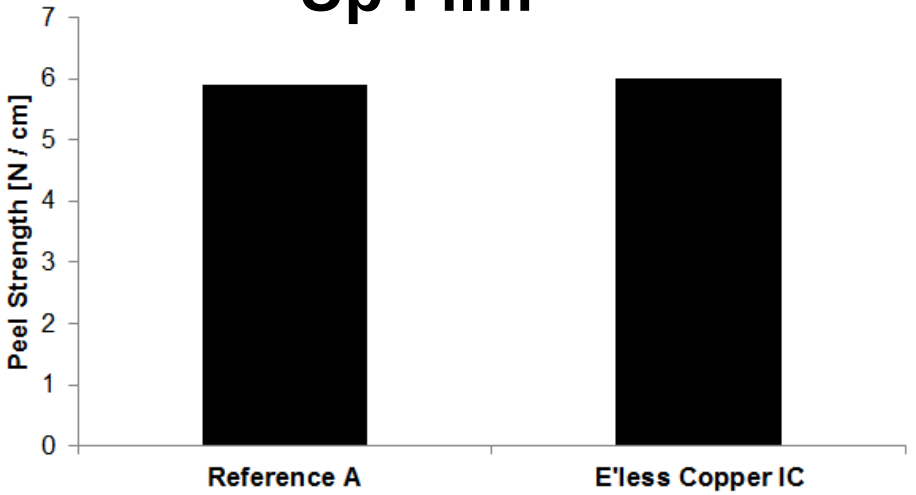
*XRD = X-Ray Diffraction

Copper Adhesion on the Substrate (IC)

Internal Stress Evaluation



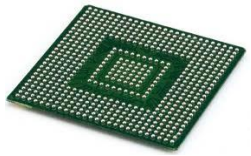
Peel strength results on Standard Build-Up Film



Copper Adhesion on the Substrate:

- Deposited Cu layers of the new e'less Cu bath exhibit moderately tensile stress suppressing the formation of blisters

Reliability Requirements (IC / HDI)

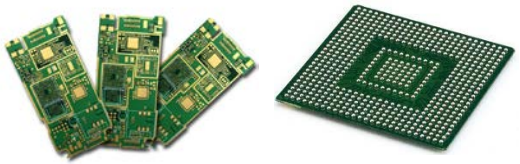


Test	Conditions	Result
Solder shock test (SST)	6 × 288°C solder float	Passed
Interconnect stress test (IST)	From RT up to 150°C, resistance increase in the power circuit < 3%	2000 cycles passed
“Comfort 40” online temperature cycle test (TCT)	-40°C / 125 °C, 15 min / 15 min, resistance increase in the power circuit < 3 %	1000 cycles passed
Quick Via Pull (QVP)	75, 100, 125 and 150 µm diameter BMVs	Passed

Reliability:

- Both new e’less Cu processes have passed all standard reliability requirements including 2.000 cycles IST testing

Summary



- The main miniaturization challenge to be overcome is the reduction of the differential etch in the pattern plating process by decreased electroless copper thickness on the surface of the build-up layer
- Two new electroless copper baths have been developed to cope with these challenges in the high-end IC substrate segment as well as in the evolving HDI board market
- Both new electroless copper processes fulfil the requirements, namely:
  - **Throwing Power**
  - Dry Film Adhesion
  - Copper Adhesion on the Substrate
  - Reliability

Thank you for your attention!

Q&A

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