Development of a Design & Manufacturing Environment for Reliable and Cost-Effective PCB Embedding Technology

M. Brizoux, A. Grivon, W. C. Maia Filho, Thales Corporate Services
Meudon-la-Forêt, France

J. Stahr, M. Morianz
AT&S
Leoben, Austria

Hemant Shah, Ed Hickey
Cadence Design Systems Inc.
Chelmsford, MA USA

Key Words : 3D packaging, Embedded chips, SiP, CAD tool, Thermo-mechanical, Strain gage, Torsion test, Reliability, 3D laser scan

Abstract

The desire to have more functionality into increasingly smaller size end products has been pushing the PCB and IC Packaging industry towards High Density Interconnect (HDI) and 3D Packaging (stacked dies, embedded packaged components). Many companies in the high-end consumer electronics market place have been embedding passive chip components on inner PCB and IC Packages for a few years now. However, embedding packaged components on inner layers has remained elusive for the broader market due to lack of proper design tools and high cost of embedding components on inner layers. Many more companies worldwide now have development projects, prototypes or first series of embedded products that are starting to be produced from several manufacturing sources. Miniaturization and 3D integration are clearly the drivers for PCB embedding technology to support new silicon packages and modules with active and passive components. Environmental issues around the technology are becoming important and need to be properly managed to generate an error free path from the generation of the design data through the production line to the functional test. The standardization on the embedding technology has been started years ago and this year the activities for functional test have begun.

This paper will highlight several key industrialization aspects addressed in the frame of the European funded FP7 HERMES* project to build a manufacturing environment for products with embedded components. The program entered its third year and is now dealing with the manufacturing of functional demonstrators as an introduction to industrialization.

The focus of the paper will be placed on three critical activities:

- The development of a PCB CAD design solution that supports embedding packaged components.
- The thermo-mechanical activities performed to support the definition of design rules. The latter has been achieved through FEA simulations supported by a comprehensive test program based on strain gage measurements under torsion which will be detailed. The work enabled to characterize the mechanical behavior of embedded PCBs taking into account the build-up as well as the effect of soldered components, which ensures reliable and highly functional embedded PCBs and modules.
- The high production yields in order to achieve a cost effective technology driven by process control and using advanced tools like high definition 3D laser scanning.

Notes :

(*) HERMES : High density integration by Embedding chips for Reduced size Modules and Electronic Systems.

Introduction

The mega trends in the electronic industry driven by handheld products are showing up in dramatic improved performances and better human interfaces. Product design and the access to all of the Internet services like HD videos and social networks are demanding miniaturization and circuit integration. Consumer products like smart phones are driving the technology and their hype has just started. Today, they are relying on state-of-the-art 4 – N – 4 HDI printed circuit boards, but for the next generation new technologies are needed to achieve higher interconnection densities. In this field, PCB embedding technology has the potential to play “the” important role, with the possibility to build a variety of very dense SiP (System in Package) modules or SiB (System in Board). Moreover, the technology offer additional benefits in terms of IP protection (anti-tamper) which makes it attractive for a wide range of security applications. The figure below shows a projection of how PCB embedding is likely to penetrate the electronic component packaging market.

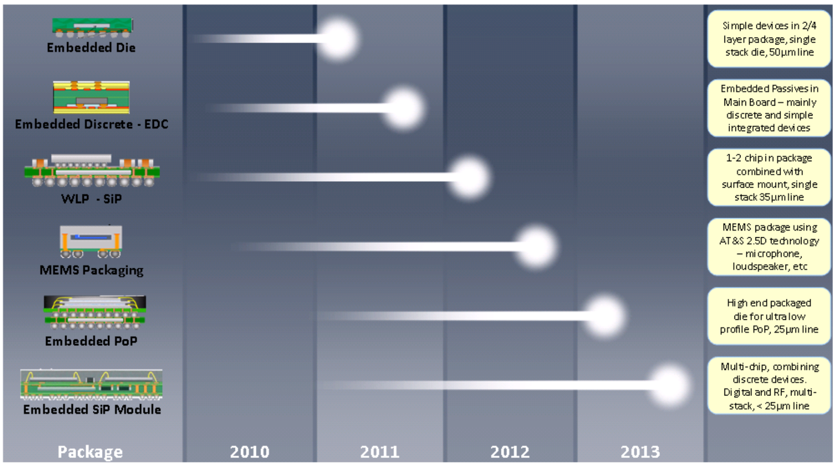

Embedded Die
Embedded Discrete - EDC
WLP - SiP
MEMS Packaging
Embedded PoP
Embedded SiP Module
Package
2010
2011
2012
2013
Simple devices in 2/4 layer package, single stack die, 50µm line
Embedded Passives in Main Board – mainly discrete and simple integrated devices
1-2 chip in package combined with surface mount, single stack 35µm line
MEMS package using AT&S 2.5D technology – microphone, loudspeaker, etc
High end packaged die for ultra low profile PoP, 25µm line
Multi-chip, combining discrete devices. Digital and RF, multi-stack, < 25µm line

Figure 1 – PCB embedding projected roadmap for component packages.

The industrialization of PCB embedding technology has been prepared through the HERMES program which is now reaching its last stage of development. During the current year, HERMES focused on design rules, process maturity and reliability, and is ready for demonstration on 3 types of fully functional demonstrators : a power module, a motor control module and an embedded PCB for a security application. The initial process evaluation cell has been upgraded to a dedicated production line monitored by efficient quality tools and able to manufacture embedded products in a semiconductor condition controlled environment. Important developments have also been engaged on both the material side and the production plating equipment to achieve high yields at the ultra fine line semi additive process stage required for the HERMES targeted 25 µm design rule.

In parallel, significant efforts have been deployed with silicon suppliers to overcome the identified supply-chain hurdles regarding the wafer post-processing operations required for PCB embedding. Actions have been undertaken to find a contractual agreement to access required documentation in order to bridge the gap between silicon and PCB makers.

Last, the HERMES consortium invited the most important EDA tool suppliers to collaborate with them in order to dispose of a consistent data flow and design data generation with the full set of design checks. Cadence – one of the supporting partners of HERMES – has developed a tool set for embedded technology that closes these gaps and ensures a reliable design output.

CAD design tool development

CAD/EDA tools have always to keep up with the fast evolutions of component packaging and PCB fabrication technologies while ensuring efficiency and productivity. With the recent proliferation of 3D packaging approaches, tools have more than ever to be adaptive in order to accommodate the variety of technological bricks and in parallel address multi-physics constraints : physical (place and route), electrical (signal integrity), thermal… Today, most of the popular CAD tools in use provide some level of support for embedding component within the inner layers of a PCB. However, the methods currently used are mostly referred to as “work-arounds” in the industry, meaning they are not fully integrated within the workflow and requires user manual interventions, hence major risks. An overview of some design tools current compatibility with the HERMES PCB embedding technology is given below.

Functionality for EC (Embedded Component)	Cadence	Vendor 2	Vendor 3	Vendor 4
EC placement between Cu layers	🟩	🟥	🟥	🟩
EC pads available for via interconnect	🟩	N/A	N/A	🟩
EC with pads on top & bottom sides	🟧	🟧	🟩	🟨
Possibility to flip and/or rotate each EC separately	🟨	🟥	🟥	🟨
Component span over several Cu layers	🟩	🟩	🟩	🟩
Additional layers for EC assembly, adhesive pads, cavities	🟩	🟩	🟧	🟩
Via-in-pad technology	🟩	🟩	🟩	🟩
Filled/stacked via support for sequential build-up	🟩	🟩	🟩	🟨
Separate assembly output for EC	🟩	🟩	🟩	🟩
ODB++ support for EC	🟨	🟧	🟥	🟨
Gerber/Excellon support for EC	🟨	🟧	🟧	🟨

🟩 Supported
🟧 Work-around
🟨 Planned in the next release
🟥 Not supported

Figure 2 – Support of functionalities for embedded components for various CAD tools.

In the following section, some considerations are given on functionalities that have been implemented to reliably achieve the place and route of an embedded PCB design.

Embedded component attachment and layer stack-up considerations

When considering an embedded PCB design, the designer needs first a way to specify if a component must be embedded ("Required"), may be embedded ("Optional") or must not be embedded ("External_only"). This has been managed through a dedicated attribute attached to the component and consistently integrated in the existing use model.

Then, the designer needs to easily place components on internal layers of the PCB stack-up. PCB CAD tools typically have an interface that describes the cross-section of the PCB in terms of layer ordering, layer types, thickness of materials and various electrical parameters. When considering an embedded component design, it is necessary to understand what layer(s) is (are) targeted for embedded placement and which ones are not. The use model should be seamless, no different than swapping the side from Top to Bottom but it must be intelligent so not to permit the placement on non-embedded layers. The stack-up form should provide the legal layer(s) to the drop down mechanism used during interactive or semi-automatic placement. Placement tools must understand the attachment method used and filter out component data as necessary. To that end, the terms Direct and Indirect attach have been introduced and defined as follows :

- Direct Attach - The manufacturing technology where the components are soldered directly to an internal layer. One way to visualize this is to think of assembling a traditional PCB with the components on the external surface(s) and then laminating more layers on top of the components.

- Indirect Attach - The manufacturing technology where the components are suspended in the dielectric material between the layers. The electrical connections are made by creating holes through the layers to the component pins and then plating those holes (HERMES technology).

With direct attach, the component and its relevant pad data are transferred to the internal layer; similar to surface layer assembly. If the indirect attach method is used, pad data is filtered from the embedded layer in favor of a single layer microvia. The microvia serve the purpose of a logical connection point in the CAD database. An illustration of the two supported attachment types for a passive chip are given on the figure xx.

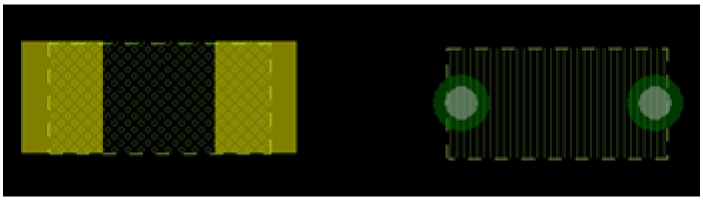
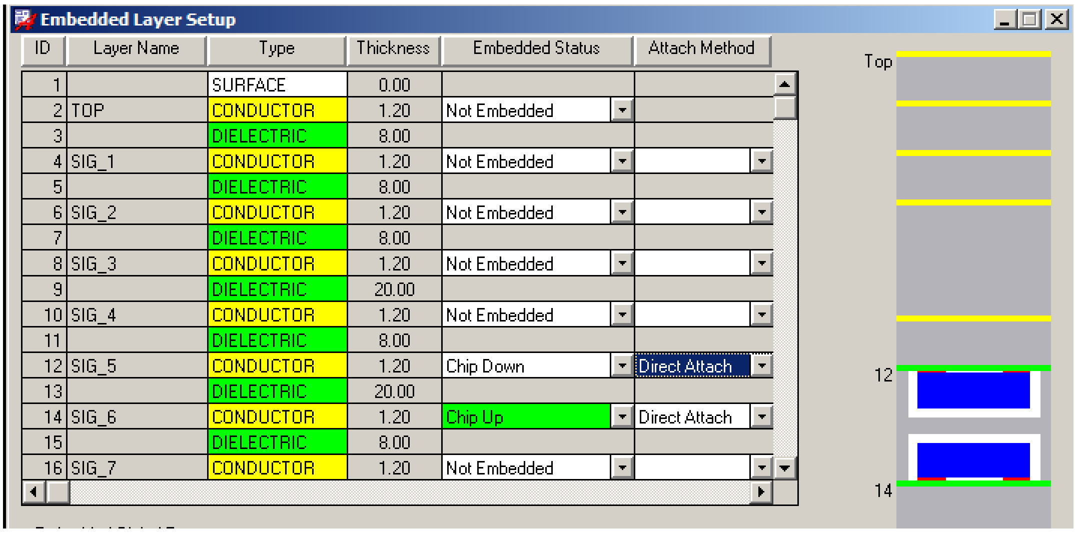


Figure 3 – Direct (soldered connections) and indirect (microvia connections) attachment methods.

The following picture gives a view of the stack-up form which includes the features specifically developed to accommodate the embedding of components on PCB inner layers.



ID	Layer Name	Type	Thickness	Embedded Status	Attach Method
1		SURFACE	0.00		
2	TOP	CONDUCTOR	1.20	Not Embedded	
3		DIELECTRIC	8.00		
4	SIG_1	CONDUCTOR	1.20	Not Embedded	
5		DIELECTRIC	8.00		
6	SIG_2	CONDUCTOR	1.20	Not Embedded	
7		DIELECTRIC	8.00		
8	SIG_3	CONDUCTOR	1.20	Not Embedded	
9		DIELECTRIC	20.00		
10	SIG_4	CONDUCTOR	1.20	Not Embedded	
11		DIELECTRIC	8.00		
12	SIG_5	CONDUCTOR	1.20	Chip Down	Direct Attach
13		DIELECTRIC	20.00		
14	SIG_6	CONDUCTOR	1.20	Chip Up	Direct Attach
15		DIELECTRIC	8.00		
16	SIG_7	CONDUCTOR	1.20	Not Embedded	

Figure 4 – Embedded layer definition in the CAD tool.

Design Rule Checks

At the heart of every physical design tool is a system responsible for validating the design data against physical, spacing, electrical and manufacturing specifications. Rule sets, often leap forward faster than EDA vendors can react. Some CAD systems provide application interface language support such as Skill that allows customers to write their own custom routines. Advanced CAD systems may offer constraints based on user defined formulas and predicates. Requirements are expected to vary between the vendors making the support of a robust DRC system quite the challenge for CAD suppliers. Components placed on internal layers should have the support of all geometrical checks that exist with conventional surface layer placement. This includes DFA rules that govern spacing between component package types. Other items that should be considered for embedded component designs include:

- Height checks – gap between component in cavity to adjacent metal layer
- Conflicts between chip up/chip down methodologies
- Component to cavity separation
- Max cavity area
- Max number of components in cavity
- Vias within cavity area
- Metal to cavity area
- Extended cavity support based on component height

Thermo-mechanical design rules

In the frame of the HERMES project, numerous simulations and experimental validations have been conducted in order to establish robust design rules and support the industrialization of the PCB embedding technology. Various key design aspects have been taken into consideration, namely signal integrity, thermal management, thermo-mechanical behavior and reliability. In this paper, the focus is set on the work carried out to characterize the thermo-mechanical behavior of embedded PCBs.

The methodology followed has been already presented [1]: it relies on the development of a FEA (Finite Element Analysis) strain distribution model supported by actual strain gage measurements under torsion and accurate PCB base material physical property characterizations [2], [3].

The whole simulation and torsion test programs have been rolled out on specifically designed 260x125 mm² test vehicle PCBs including embedded daisy-chain silicon dies of 3x3 mm², 5x5 mm² and 10x10 mm² dimensions. For each die size, both full array and peripheral interconnect configurations have been integrated, making a total embedded chip count of 6 per board. Different build-up constructions and PCB materials have been considered that can be broken down in two groups : single core 4-layers and dual core 6-layers.

For strain measurements, 3-axis rosettes have been bonded to the external sides of the test vehicle PCBs over the chip locations. Strain gages of small active length (0.8mm) have been selected to avoid the effects of the strain gradient on measurements. In addition, dedicated gages with Cu terminations have been also embedded in some constructions in order to have accurate in-situ strain measurements at the chip level. An overview of an instrumented test vehicle board with strain gages is given on the figure below.

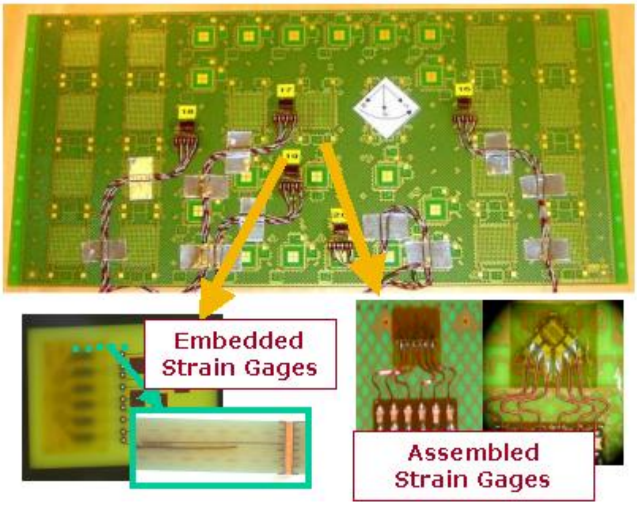


Figure 5 – Test vehicle board with embedded and assembled strain gages.

For the simulation activities, a FE model capable of reproducing each torsion test case has been developed. The model has been created for the entire board as torsion generates a homogeneous strain zone in the centre of the board whose size depends on the PCB thickness. The target being to analyze the incidence of various geometrical and material parameters, the selected approach favoured a large number of configurations and loading conditions over a complex model.

In order to facilitate the comparison between strain maps corresponding to different simulations, a single color scale has been defined to represent strains from 0 up to 3600ppm. Strain maps have been restricted to the central PCB zone, because board edges typically undergo higher stresses under torsion. An example of strain map analysis is illustrated on Figure 6.

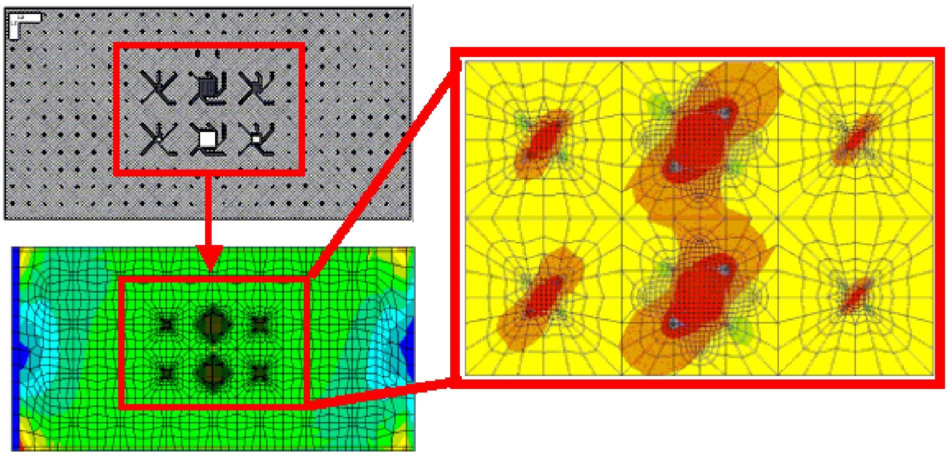


Figure 6 – Strain map zone description

The FE model has been calibrated and validated by direct comparison between :

- Simulated and measured strain on test boards submitted to torsion cycles between –7° and 7° angles.
- Calculated and measured $CTE_{X,Y}$ values between 25°C-100°C.

Generally speaking, the mismatch between simulation and experimental measurements have been found to be low. One significant difference has been however noted for the largest 10x10 mm² dies where the $CTE_{X,Y}$ values were systematically about 60% lower than the measurements on board. This variation probably originates from an improper representation of the adhesive layer covering the chip.

With the generic FE model and strain maps defined, a sensitivity analysis has been conducted to analyze the incidence of various PCB design parameters. This analysis has been carried out through an extensive DoE (Design of Experiment) including numerous simulation cases as well as torsion test runs.

As an example, the figure xx compares the estimated strain distributions in the layers of 4-layer embedded PCBs of 0.8mm – 1.6mm – 2mm thicknesses. In this case, PCBs have been manufactured with the same base material and pre-preg type using a 0.4mm embedded core.

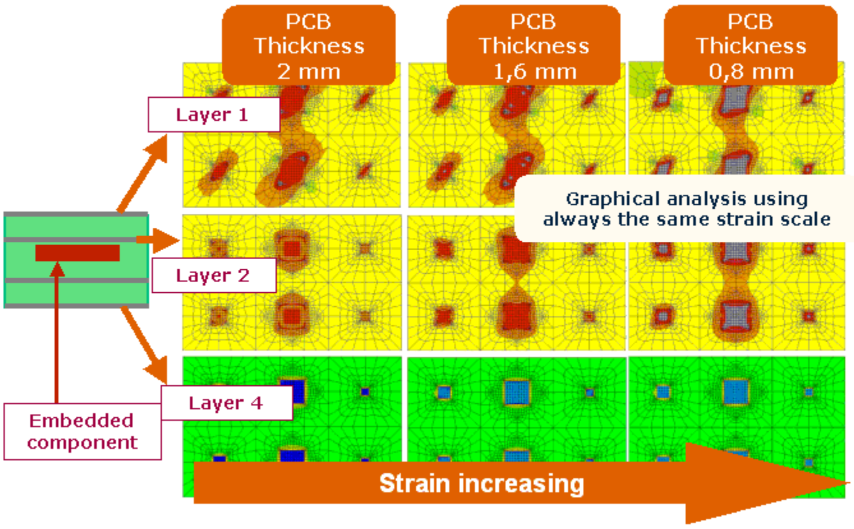


Figure 7 – PCB thickness incidence on embedded component strain.

In this example, the effect of PCB thickness is clearly highlighted : when PCB thickness decreases, strain in the corners of embedded silicon dies increases significantly especially for the larger 10x10 mm² dies. Moreover, lesser strain is seen by the chips when located near the middle of the PCB thickness.
Other design parameters investigated and their qualitative effect on embedded components are summarized in the table hereafter.

Table 1 – Embedded component sensitivity analysis summary

Design parameter	**Conditions**	**Results**
PCB base material	Material A vs. Material B Halogen free high performances FR-4s	**Material A yields better performances than material B**
Resin content	1080 vs. 2116 pre-preg type	**Pre-preg-style 2116 yields better performances.**
PCB thickness	0.8mm vs. 2mm	**Higher thickness yields better performances**
Embedded core thickness	0.2mm vs. 0.4mm	**0.4mm core thickness yields better performances for thin boards (<1mm)** No significant effect for thick boards
Interaction between embedded and assembled component	Overlap vs. No overlap	**Strain on silicon die increases when BGA overlaps silicon die for thick boards**

The analysis enabled to determine the impact of various design variants on the thermo-mechanical behavior of PCBs with embedded active dies. With the results obtained, it has been possible to generate a first set of important design rules which will be implemented in the future reliability test vehicles as well as in the functional modules and PCB demonstrators. For the reliability characterization upcoming work, a special care has been taken in terms of base material selection and build-up definition. Various overlapping conditions will also be introduced in order to confirm the mutual incidence between embedded and external assembled components on reliability. For embedded passive chips, a complementary study has been undertaken to evaluate the reliability under various test conditions in comparison to usual equivalent soldered chips [4].

Industrialization

The industrialization of an embedding process flow requires an excellent process control to achieve high manufacturing yields, meaning 99% and more. Cleanliness of the production environment, product handling and ESD protection are key influencing factors on yield which have already been discussed and implemented [1]. At the process level, hot spots like adhesive printing, embedded component assembly and fine line structuring need in addition to be placed under strict process monitoring.

Adhesive printing

PCB embedding is a chip-first technology starting with the chip attachment to a copper foil (face-down process flow). In this operation, pads of non-conductive adhesive are screen printed on the matte side of an electrolytic ultra-thin Cu foil at the embedded component sites. The chips are then assembled over the adhesive pads with the active die side contacting the polymer.

In a face-down process flow, the microvia connections to the die are conditioned by the adhesive thickness and therefore the volume of the adhesive material under the embedded chips has to be tightly controlled. To achieve consistent and stable adhesive deposits, the shape and the volume of the adhesive pad is systematically checked before component placement and assembly (see figure 8). This is carried out with a so called 3D laser scanning equipment, which is a high resolution non-contact tool enabling fast and accurate volume measurements.

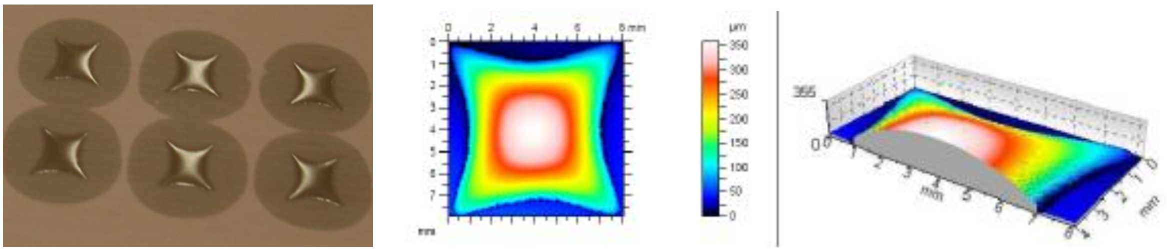


Figure 8 –Shape of adhesive pad and 3D-scanning measurement

Embedded component assembly

Contrarily to conventional surface mount device assembly, embedded components do not benefit from the self-alignment brought by the solder. Hence, PCB embedding pushes the envelope in terms of placement accuracy all the more than large panel sizes of 18” x 14” (609 x 457 mm²) and high assembly speeds are used.

Active and passive chip placement is achieved with latest generation SMD pick&place machines capable of handling devices from tape and reels, trays or diced wafers. To meet the demanding accuracy requirements, several strategies may be used.

The achievable accuracy is first influenced by the placement tool itself. For example, using a “twin head” system offers better performances compared to a “20 nozzle head”, but at the detriment of speed. Actual measurements have shown that placement accuracies even exceed values from the equipment supplier (see table below).

Table 2: Placement accuracy

	20 Nozzle head	**Twin head**
Max. speed	20000 comp/h	3700 comp/h
Accuracy specified	+/- 55 µm, +/- 0,7°	+/- 30 µm, +/- 0,07°
Accuracy measured	+/- 20 µm, +/- 0,035°	+/- 11 µm, +/- 0,025°

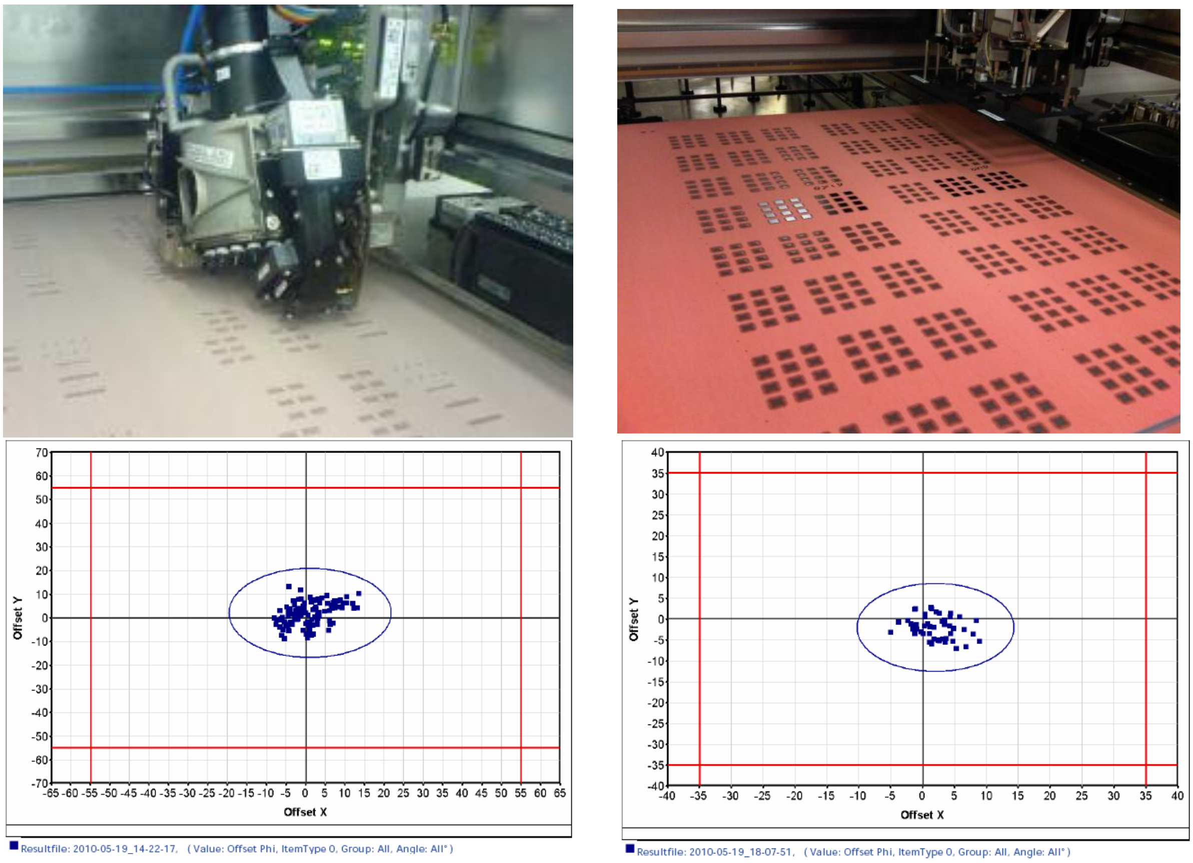


Figure 9 - Placement tool and corresponding measured accuracies for the “20 nozzle head” (left) and the “twin head” (right).

Placement accuracy is also impacted by the component registration. Enhanced accuracies can be obtained when a chip pad design recognition system is used instead of edge recognition which is affected by chipping or component dimensional tolerances. The pad recognition system relies on a high resolution camera (~10 µm per pixel) capable of detecting the individual pads of a chip to calculate the X, Y and θ values for placement. In most cases, oxidation may be also detected except when pads are too close together for an individual analysis (white circles in the picture hereafter).

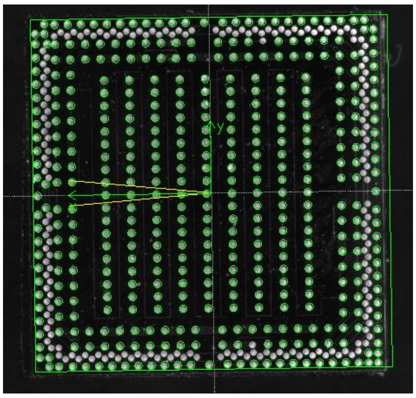


Figure 10 – Chip recoginition system (pad size:150 µm, chip size 7 x 7 mm)

Fine line structuring

Highly integrated embedded PCB/modules often requires high density structures with lines/spaces down to 25µm/25µm. For such resolution, a semi-additive technology (SAT) needs to be used in lieu of conventional subtractive etching processes. Among others, SAT relies on ultra-thin copper foils as well as a dedicated single board processor equipment for copper plating (see figure xx).

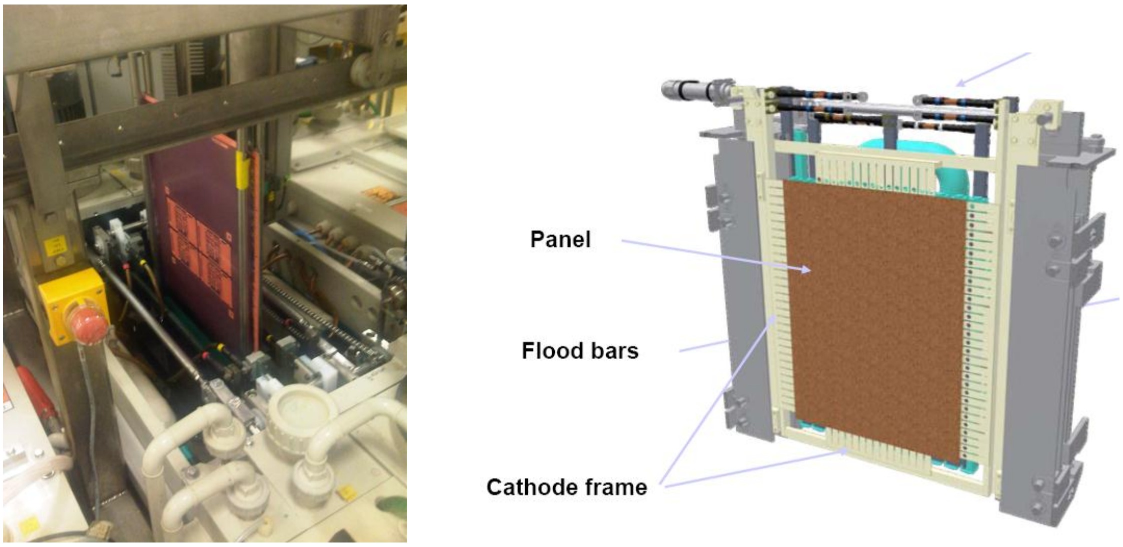


Figure 11 – **Copper plating single board processor**

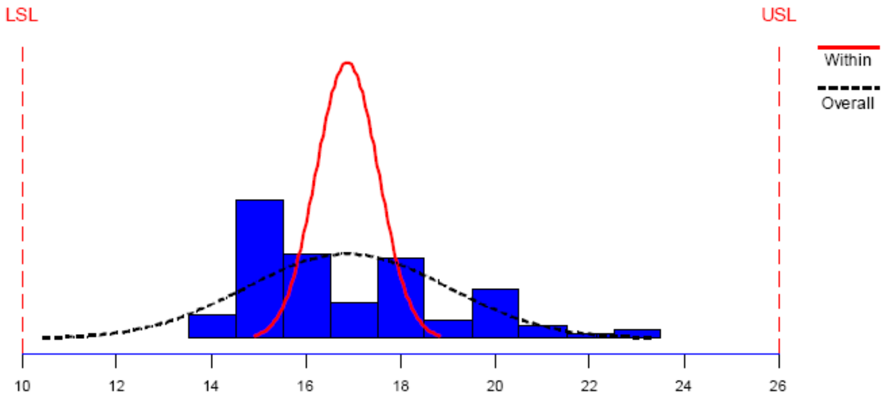
During the plating process, maintaining an equal copper thickness distribution over the whole panel is key. This distribution depends on the positioning of the panel in the copper bath. Therefore the distance between panel and the anodes is directly influencing the copper thickness on the panel. The standard distance of the anode to the panel is 20 mm.

Figures 11 and 12 illustrate the achieved copper thickness and line width distribution. The mean value of the copper thickness is around 17 µm with a standard deviation of 2,1 µm. This result shows a stable copper distribution over the whole panel of a size of 18” x 24” (457 x 609 mm²).

For line width, the results show a mean value of around 25 µm and a standard deviation of 1,7 µm. It is important to mention that the line width depends on the accuracy of the resist structuring during the imaging process before.

Process Data	
USL	26,0000
Target	*
LSL	10,0000
Mean	16,8691
Sample N	102
StDev (Within)	0,65787
StDev (Overall)	2,13869

Potential (Within) Capability	
Cp	4,05
CPU	4,63
CPL	3,48
Cpk	3,48
Cpm	*



Overall Capability	
Pp	1,25
PPU	1,42
PPL	1,07
Ppk	1,07

Observed Performance	
PPM < LSL	0,00
PPM > USL	0,00
PPM Total	0,00

Exp. "Within" Performance	
PPM < LSL	0,00
PPM > USL	0,00
PPM Total	0,00

Exp. "Overall" Performance	
PPM < LSL	659,44
PPM > USL	9,80
PPM Total	669,24

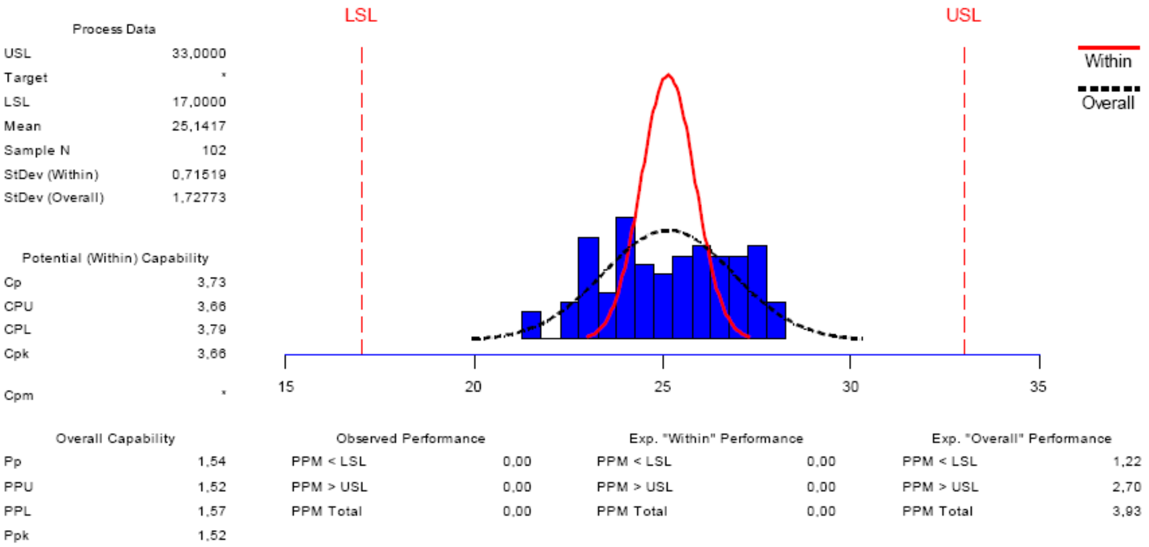


Figure 12 – Copper thickness (top) & line width (bottom) for a 25 µm line/space design

To minimize the risk of failures like opens/shorts, quality gates like high-resolution AOI and 100% continuity test have been implemented.

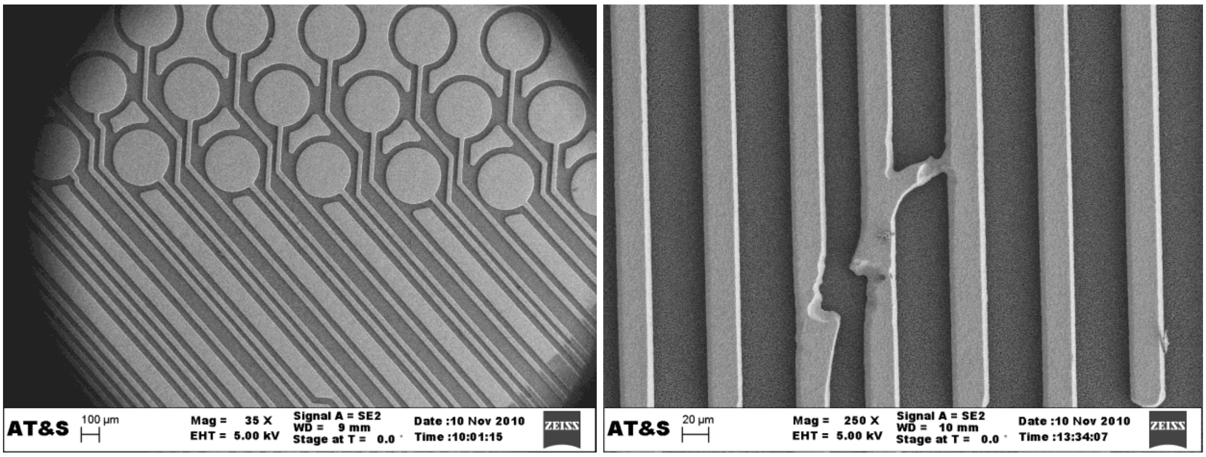


Figure 13 – 25µm line/space structures (left) and shorting failure due to a scratch (right)

Synthesis

The 3-year HERMES program is reaching its final stage before the industrialization of this advanced technology can take place : the demonstration phase on fully functional highly integrated SiP/SiB demonstrators. The manufacturing processes have been upgraded and placed under quality control at critical steps like adhesive printing, embedded component assembly and fine line structuring. In the frame of the design/reliability activities, design rules have been generated to optimize the PCB build-up and the embedded component placement in combination with the external SMD components.

. For the next step, the multilayer build-ups have been specified and the material selection has been done. All demonstrators will use low-CTE high-Tg materials to fulfill the reliability requirements for temperature cycle tests up to 3000 and multiple lead free soldering processes.

The design of the embedded modules has been done with operational CAD/EDA tools integrating functionalities specific to PCB embedding technology. The release of a new full set of tools is planned for 2011 to avoid the hand work which is still necessary to bring the files in a usable form for the CAM.

Conclusion and perspectives

HERMES has done a significant progress in process development towards ultra fine line technology (25µm) for realizing high density interconnects (up to 15000 pts/dm²) of the functional demonstrators with silicon dies with more than 400 I/Os. The manufacturing cell as been upgraded to comply with all the requirements for handling ESD sensitive dies under clean room conditions.

The design rules obtained from dedicated reliability test vehicles have been implemented in the design (layout) of the several functional demonstrators.

The exploitation of PCB embedding has started on a bilateral base beside the technology development in HERMES. HERMES is the European spear head to drive the development of the customer base and the business by implementing the technology on the actual development into customer projects. This direct implementation of technology into products with lower complexity enabled a good progress in bringing these products to industrialization. Customers from the silicon industry are the early adopters using chip embedding for new packaging solutions. Tthe ramp up to volume production has started and the products for the mobile phone and handheld industry have been launched on the market. It was an important milestone to proceed with the implementation of the HERMES technology in more and more complex modules and to exploit the embedding technology in additional business fields.

Acknowledgements

The authors would like to express their thanks to the European Commission for their funding of the HERMES project (FP7-ICT-224611).

References

[1] M. Brizoux et al., " Industrial PCB Development Using Embedded Passive & Active Discrete Chips Focused on Process and DfR ", *Proceedings of IPC APEX Conference*, Las Vegas, USA, April 2010.

[2] W. C. Maia Filho et al., “Influence of build-up construction and resin-content on mechanical behavior of printed circuit boards”, *Proceedings of 10th IEEE Eurosime*, International Conference on Thermal, Mechanical and Multi-Physics Simulation and Experiments in Micro-Electronics and Micro-Systems, Delft, Netherlands, April 2009.

[3] W. C. Maia Filho et al., “Optimization of PCB build-up layer configuration for electronic assemblies with active embedded components in the board”, *Proceedings of 11th IEEE Eurosime*, International Conference on Thermal, Mechanical and Multi-Physics Simulation and Experiments in Micro-Electronics and Micro-Systems, Bordeaux, France, April 2010.

[4] C. Ryder et al., " Embedded Component : A Comparative Analysis of Reliability”, *Proceedings of IPC APEX Conference*, Las Vegas, USA, April 2011.

Development of a Design & Manufacturing Environment for Reliable and Cost-Effective PCB Embedding Technology

AT&S

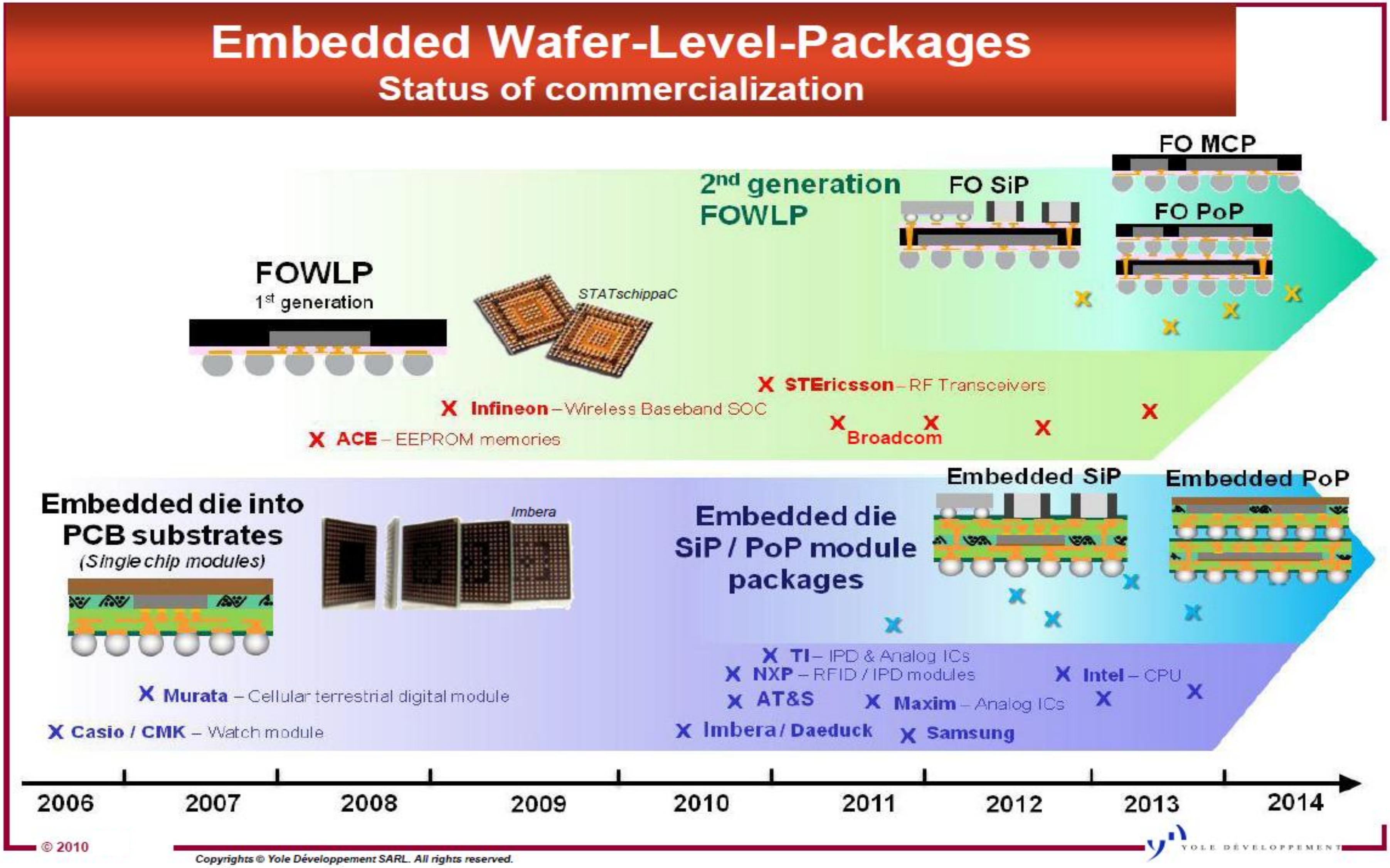
cadence®

THALES

Outline

- Introduction
- CAD design tools for embedded components
- Thermo mechanical design rules
- The industrialisation of chip embedding
- Outlook and business

Development of chip embedding technology



Embedded Wafer-Level-Packages

Status of commercialization

FOWLP
1st generation

STATschippaC

2nd generation FOWLP

FO SiP

FO MCP

FO PoP

X STEricsson – RF Transceivers

X Infineon – Wireless Baseband SOC

X ACE – EEPROM memories

X X **Broadcom**

Embedded die into PCB substrates
(Single chip modules)

Imbera

Embedded die SiP / PoP module packages

Embedded SiP

Embedded PoP

X TI – IPD & Analog ICs

X NXP – RFID / IPD modules

X AT&S

X Maxim – Analog ICs

X Imbera / Daeduck

X Samsung

X Intel – CPU

X Murata – Cellular terrestrial digital module

X Casio / CMK – Watch module

© 2010

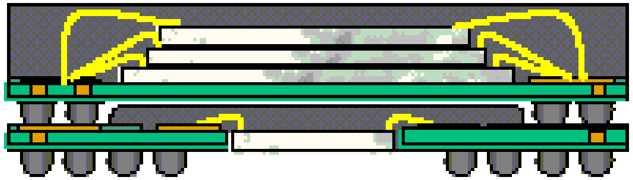
Copyrights © Yole Développement SARL. All rights reserved.

Miniaturization Approaches

- Technology drivers that create large pin count devices
  - SoC – more functional density
  - SiP – mixed technologies with memory
- Miniaturization approaches used on PCB systems
  - Mezzanine boards
  - Rigid Flex circuits
  - High Density Interconnect
    - Shrinking pin pitch (< 0.4mm)
    - Large pin count devices
  - Embedded Passives
  - Low pin Actives

2008:
- 2G / 3G / 2 MP
- GPS / WiFi
- Memory
- Slim

2009:
- 3G / 3.2-MP
- GPS / WiFi
- More Memory
- Slimmer profile
- Battery life



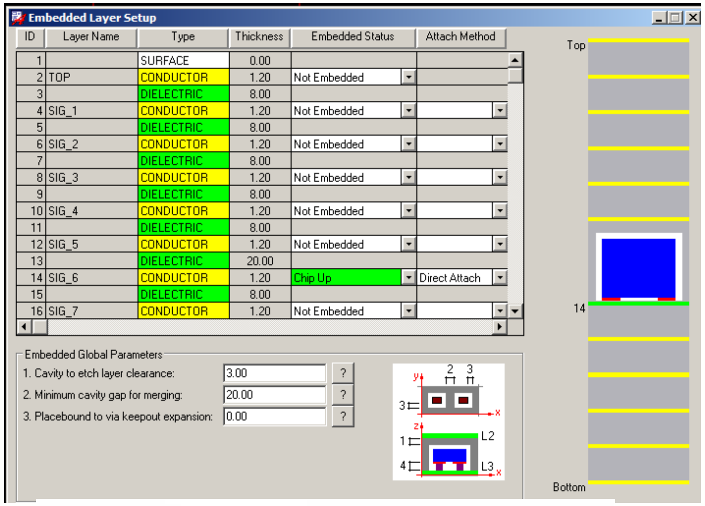
PCB / IC-Packaging design tool requirements
1) Component, layer stack selections

Engineers specify

- Components to be embedded
  - "Embed Required" (Hard) or "Embed Optional" (Soft)
  - Ensures only qualified components get embedded
- Layers to be used

Embedding concept

- Chip-up, Chip-down
- Face-up, Face-down
- Direct (SMD), Indirect (embedded)

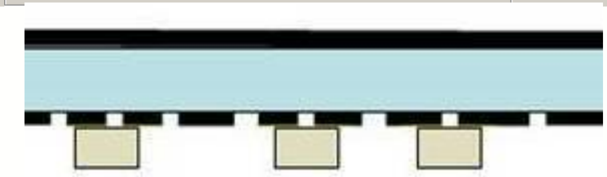


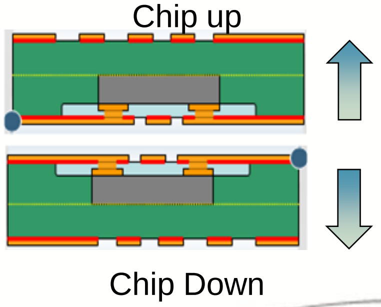
Embedded Layer Setup

ID	Layer Name	Type	Thickness	Embedded Status	Attach Method
1		SURFACE	0.00		
2	TOP	CONDUCTOR	1.20	Not Embedded	
3		DIELECTRIC	8.00		
4	SIG_1	CONDUCTOR	1.20	Not Embedded	
5		DIELECTRIC	8.00		
6	SIG_2	CONDUCTOR	1.20	Not Embedded	
7		DIELECTRIC	8.00		
8	SIG_3	CONDUCTOR	1.20	Not Embedded	
9		DIELECTRIC	8.00		
10	SIG_4	CONDUCTOR	1.20	Not Embedded	
11		DIELECTRIC	8.00		
12	SIG_5	CONDUCTOR	1.20	Not Embedded	
13		DIELECTRIC	20.00		
14	SIG_6	CONDUCTOR	1.20	Chip Up	Direct Attach
15		DIELECTRIC	8.00		
16	SIG_7	CONDUCTOR	1.20	Not Embedded	

Embedded Global Parameters

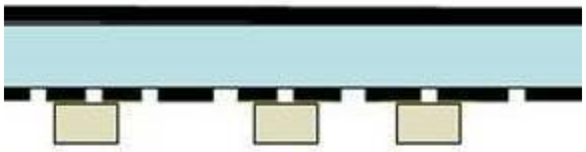
1. Cavity to etch layer clearance: 3.00
2. Minimum cavity gap for merging: 20.00
3. Placebound to via keepout expansion: 0.00

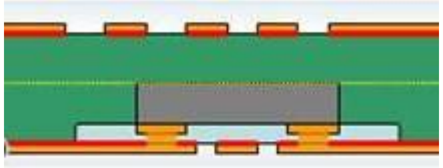


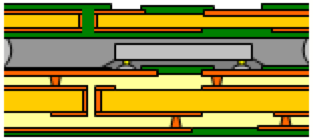


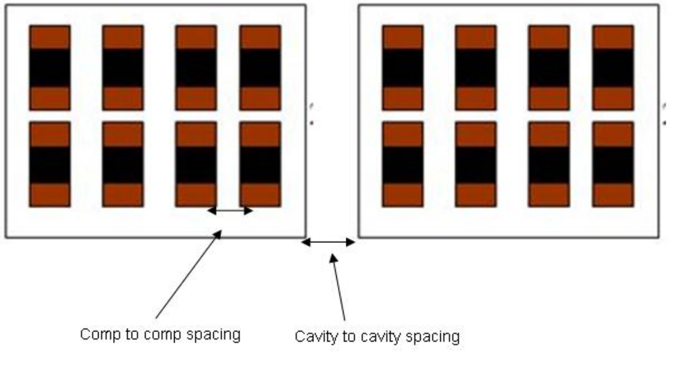
PCB / IC-Packaging design tool requirements
2) Design Rule Checks

- Component to Component / Cavity
- Height checks – gap between component in cavity to adjacent metal layer
- Max cavity area
- Max number of components in cavity
- Vias within cavity area
- Metal to cavity area
- Extended cavity support based on component height
- etc



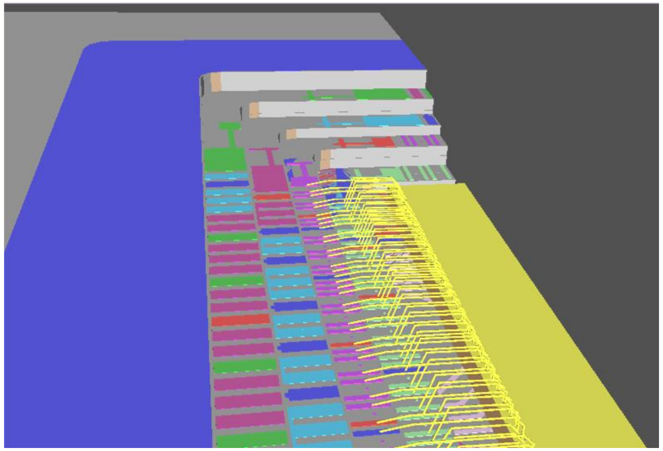




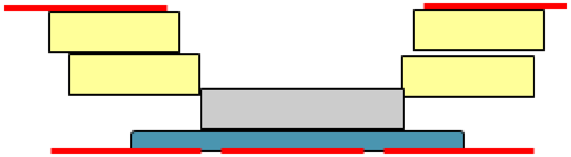

Comp to comp spacing
Cavity to cavity spacing

PCB / IC-Packaging design tool requirements
3) Cavity Support

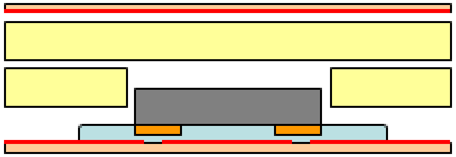
- Package driven
  - Keep-out properties
- User Defined Cavities
  - Manually created
  - Span multiple layers
  - Merge capability
  - Design Rule Checks
    - Max cavity area
    - Max comps within cavity



Open Cavity

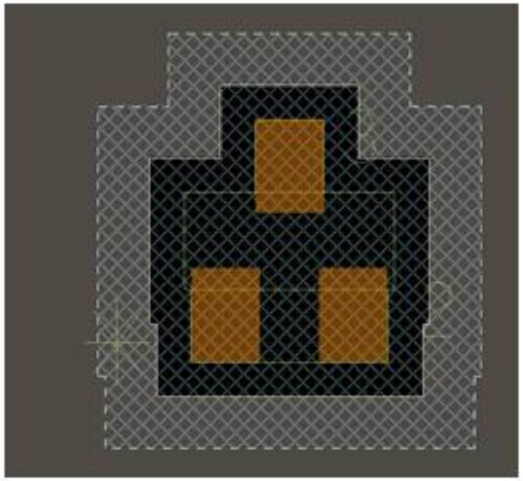


Closed Cavity



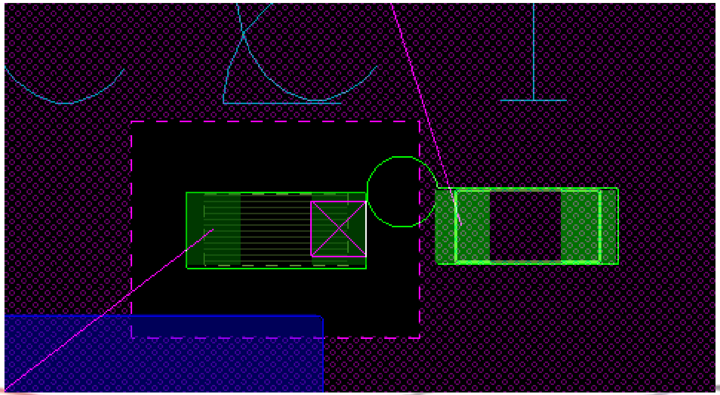
PCB / IC-Packaging design tool requirements
4) Constraint-Driven Place & Route, Mfg outputs

- Constraint driven place and route
  - Move components to inner layers
    - Don’t put a via through the component!
  - Route to embedded components adhering to electrical, physical and manufacturing constraints



Expanded Route Keepout area on protruding layer(s)

- Manufacturing outputs for layers with embedded devices
  - ODB++
  - etc



Dynamic Design for Assembly guided placement

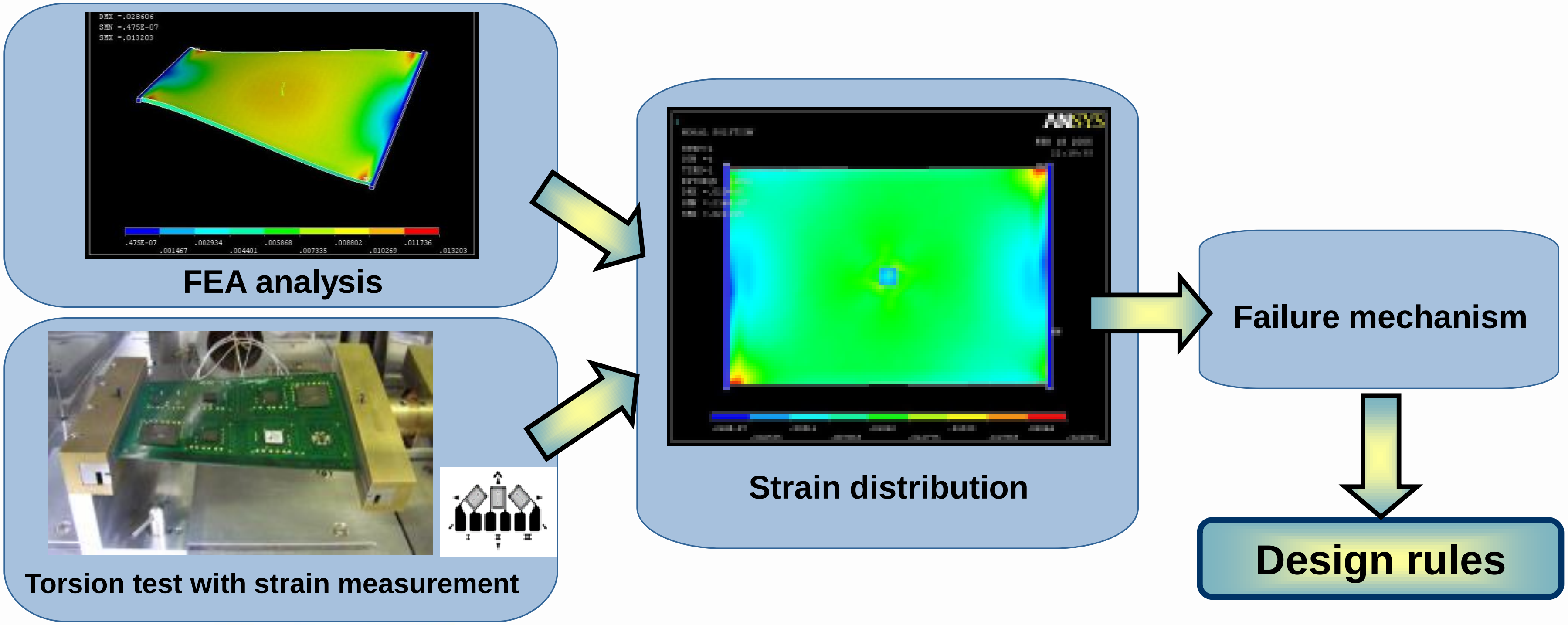
Checklist for EDA ECP Capability

🟩 Supported 🟨 Planned 🟧 Workaround

	Cadence
	Version: Allegro Beta 16.4
	HERMES Support Partner: THALES
Functionality for ECP®	**Release: Planned Q2, 2011**
ECP® component placement between copper layers	🟩
ECP® component pads available for via interconnect	🟩
ECP® component with pads on top and bottom side	🟧
Possibility to flip and/or rotate each ECP® component separately	🟨
Component span over several copper layers	🟩
Additional layers for ECP® - assembly, glue spots, cavities	🟩
Separate assembly output for ECP® components	🟩
ODB++ support for ECP®	🟨
Gerber/Excellon support for ECP®	🟨
Via-in-pad technology	🟩
Filled/stacked via support for sequential buildup	🟩

Thermo-Mechanical Assessment Methodology

Modelling of stress & strain in embedded structures


DMX =.028606
SMN =.475E-07
SMX =.013203
.475E-07
.001467
.002934
.004401
.005868
.007335
.008802
.010269
.011736
.013203
ANSYS

FEA analysis

Torsion test with strain measurement

Strain distribution

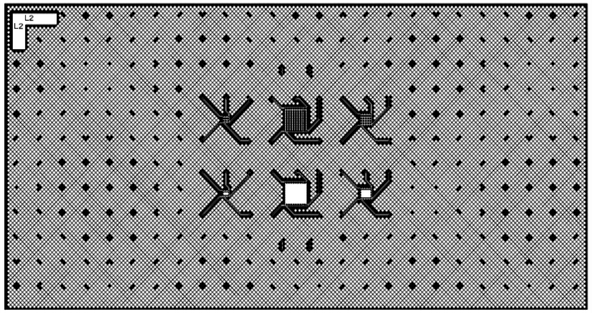
Failure mechanism

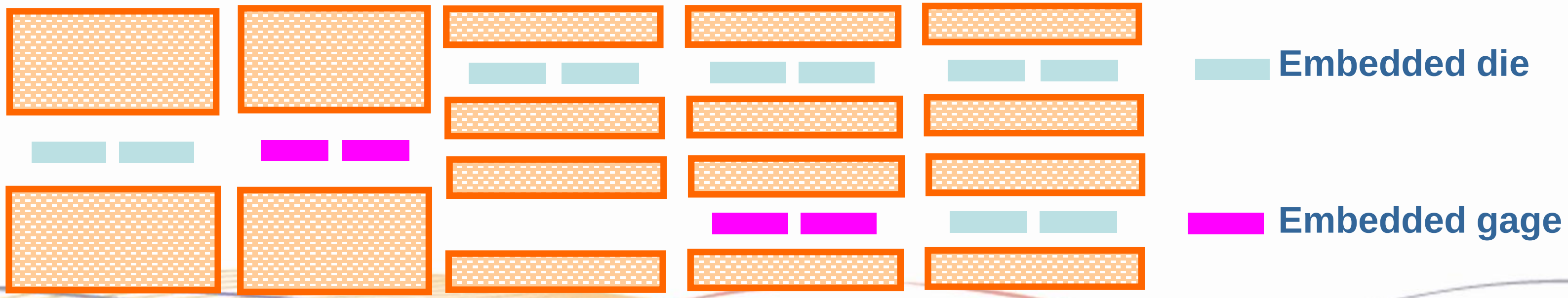
Design rules

Test Vehicle Overview

Various 4-6 layer PCBs embedding daisy-chain dies

- Total thickness : 0.8mm – 1.6mm – 2.0mm
- 2 halogen-free base materials




Embedded die
Embedded gage

Daisy-Chain Embedded Dies

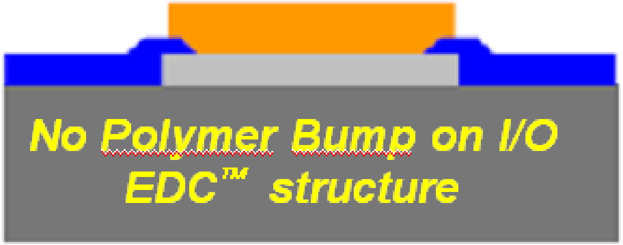
Thinned down to 150µm, Cu pad plating (FCI)

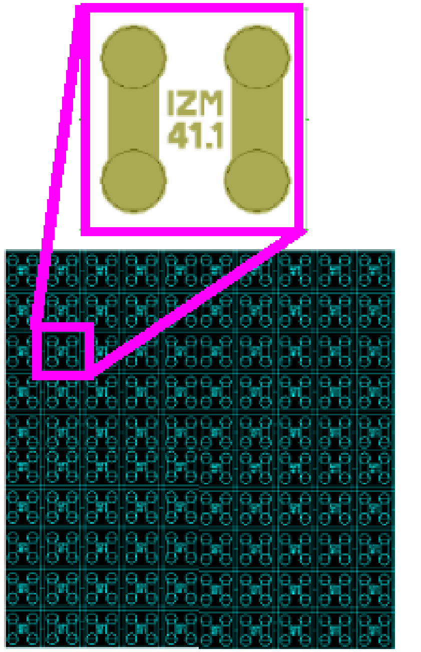
3 sizes : 3x3, 5x5, 10x10mm²

Up to 400 pads/microvia connections

Peripheral & full array configurations

Pad size : 270µm, 0.5mm pitch

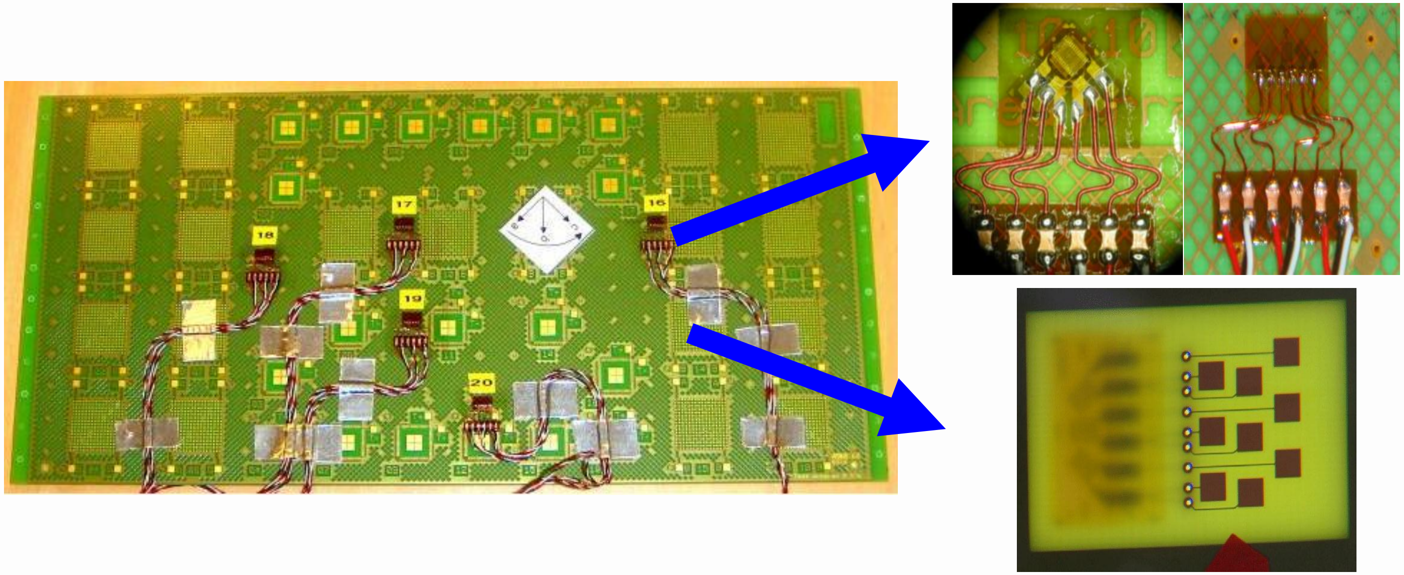

No Polymer Bump on I/O
EDC™ structure



Torsion Testing

Strain gage measurements under repeated torsion cycles

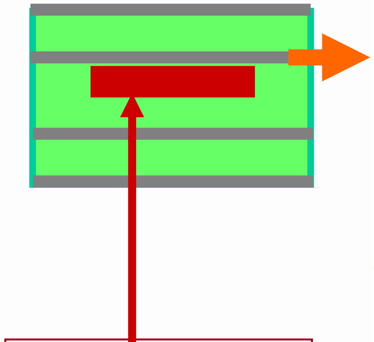
- Angle : -7° / +7°
- Temperature : up to 100° C



Assembled Strain Gages

Embedded Strain Gages

Findings

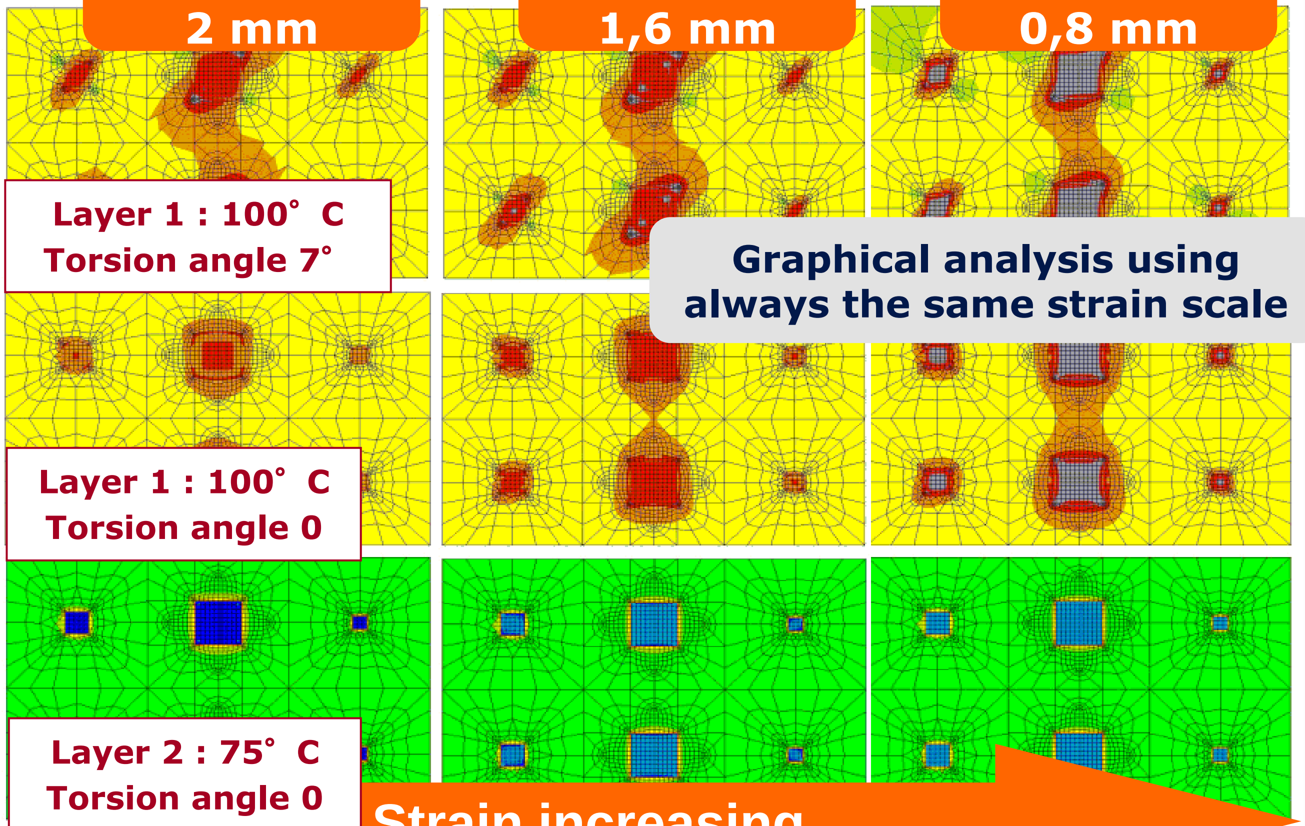


Embedded component

PCB Thickness 2 mm

PCB Thickness 1,6 mm

PCB Thickness 0,8 mm



Layer 1 : 100° C
Torsion angle 7°

Layer 1 : 100° C
Torsion angle 0

Layer 2 : 75° C
Torsion angle 0

Graphical analysis using always the same strain scale

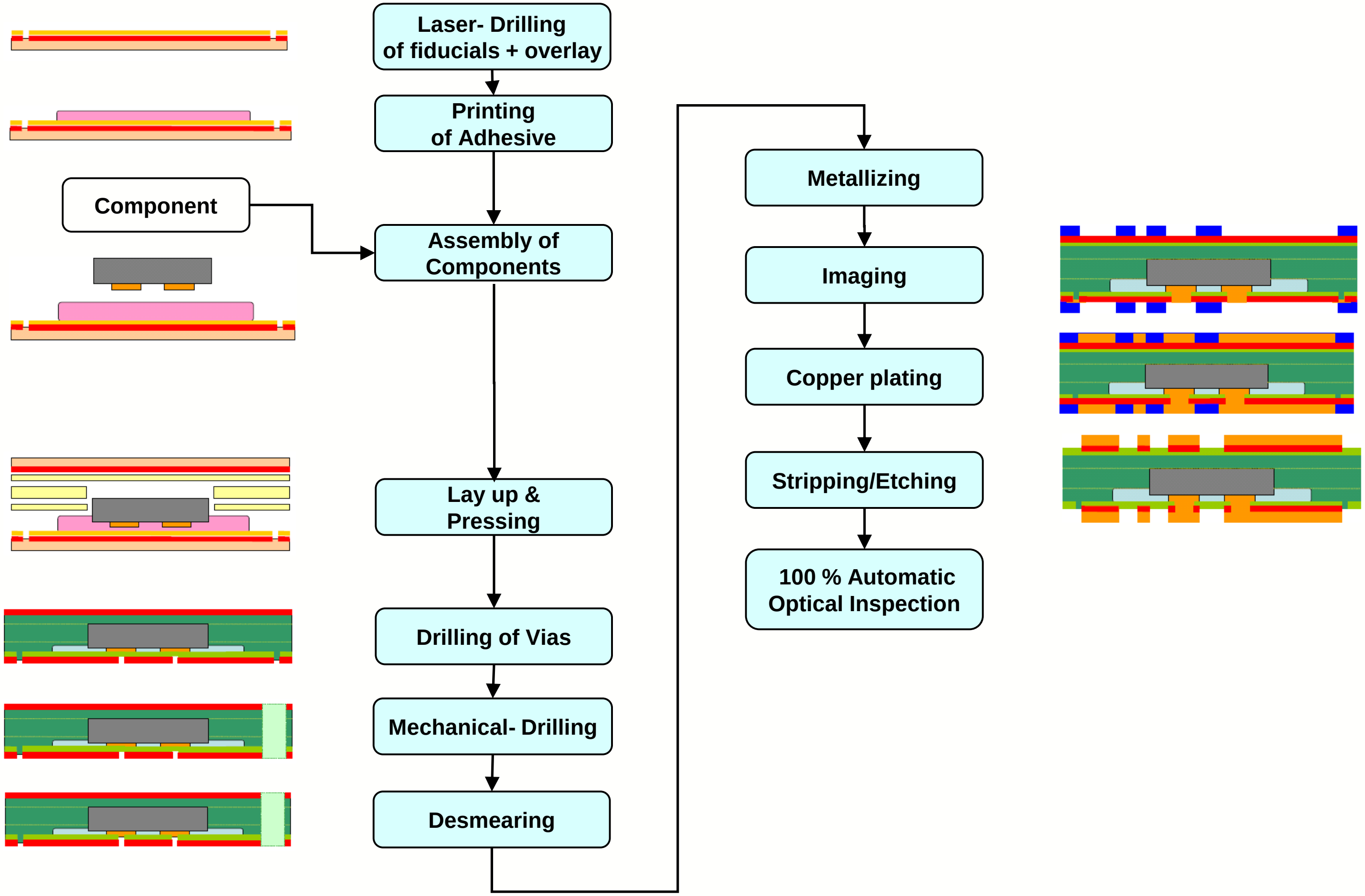
Strain increasing

Sensitivity Analysis

Incidence of various design parameters on strain for embedded components

Design parameter	Conditions	Results
PCB base material	Material A vs. Material B Halogen-free high performances FR-4s	**Material A gives lower strain in inner layers**
Resin content	1080 vs. 2116 pre-preg type	**2116 pre-preg gives lower strain in inner layers**
PCB thickness	0.8mm vs. 2mm	**Higher thickness gives lower strain in inner layers**
Embedded core thickness	0.2mm vs. 0.4mm	**0.4mm gives lower strain in inner layers for thin boards (<1mm)** **No significant effect for thicker boards**
Interaction between embedded and assembled components	Overlap vs. No overlap	**Increased strain on Si dies with overlapping**

Process Flow Embedded Core



Laser- Drilling of fiducials + overlay

Printing of Adhesive

Component

Assembly of Components

Lay up & Pressing

Drilling of Vias

Mechanical- Drilling

Desmearing

Metallizing

Imaging

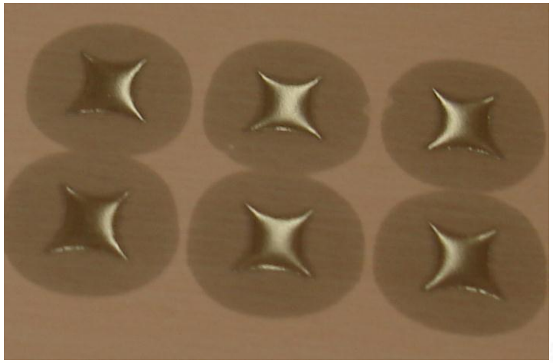
Copper plating

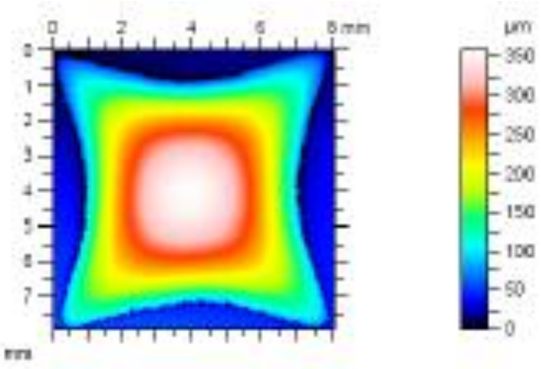
Stripping/Etching

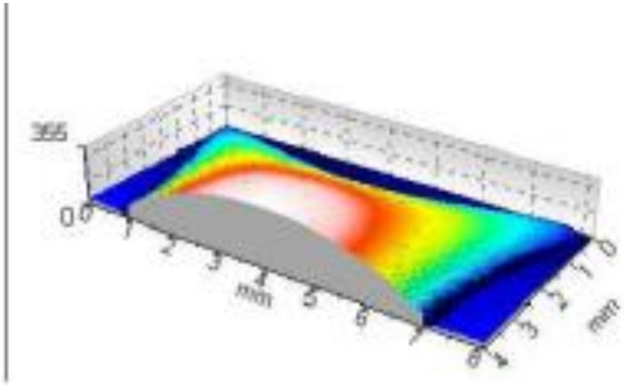
100 % Automatic Optical Inspection

Adhesive Printing

- Control of
  - feature size, shape and volume
  - By novel 3D scanner for large panels





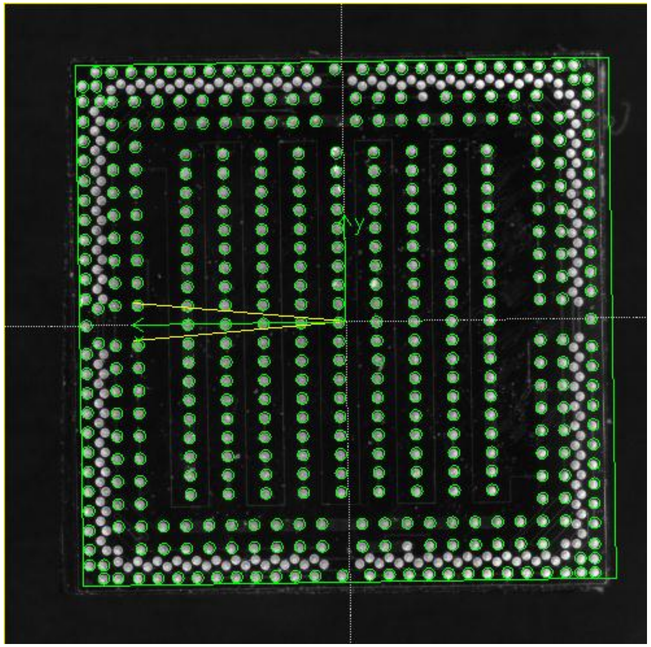


  - determines the thickness and uniformity of the dielectric

Component Assembly

- Optical alignment of Flip Chip component
  - Requires high resolution cameras
  - Pattern recognition of pad design

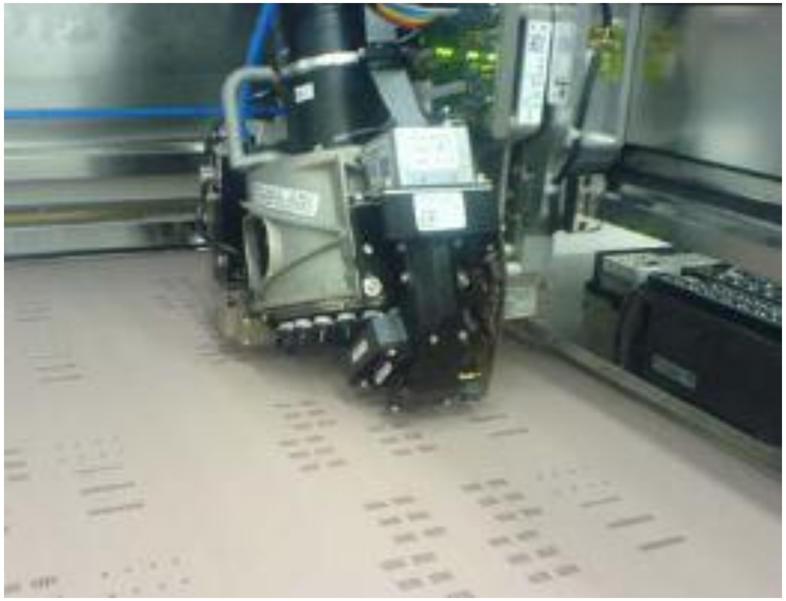
- Design
  - Pad diameter: 150 µm
  - Minimum pitch : 200 µm
  - Chip size : 7 x 7 mm

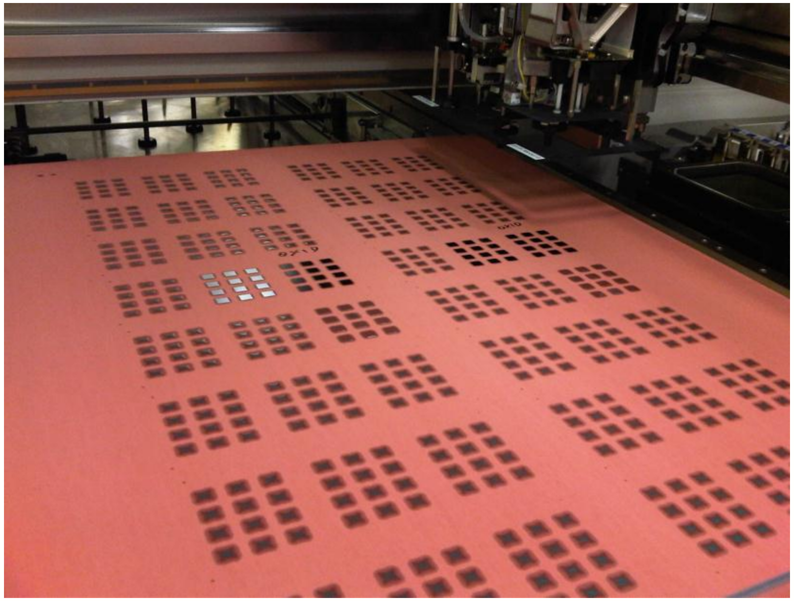


Component Assembly

- Siemens X2 machine has two assembly heads
  - 20 nozzle head
  - For high throughput

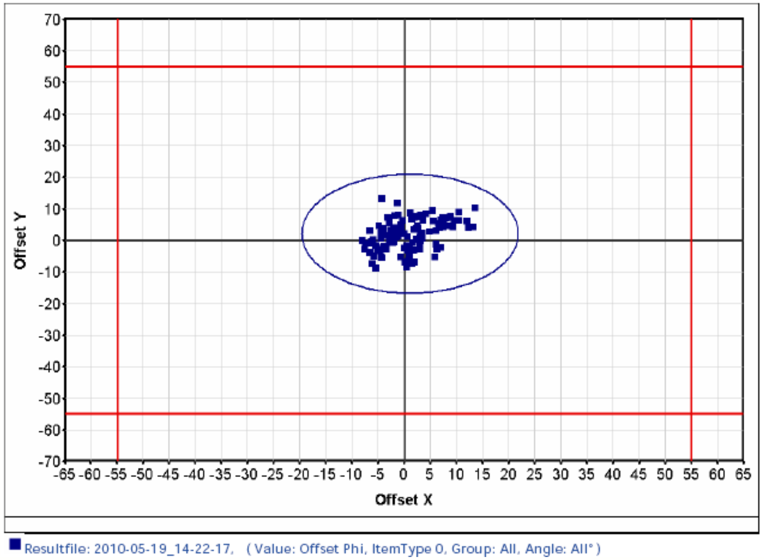
- twin head
- for high accuracy

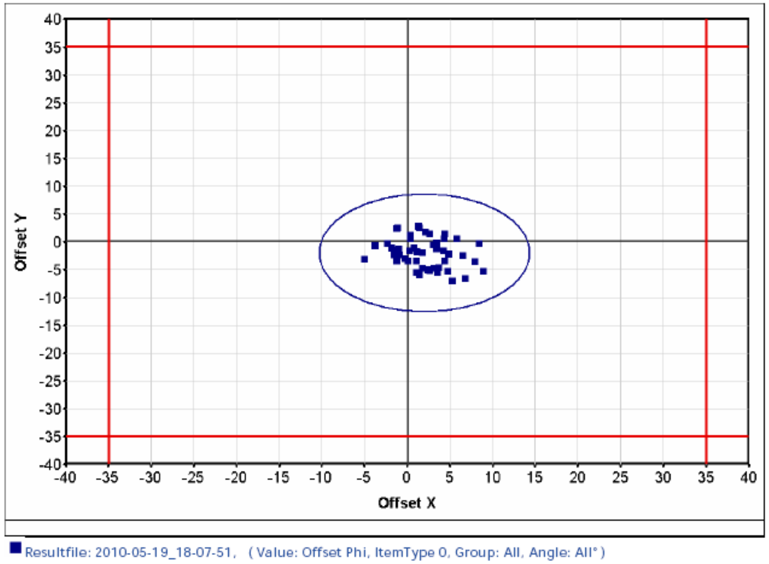




Component Assembly

- Component placement accuracy
  - 20 Nozzle head   - twin head

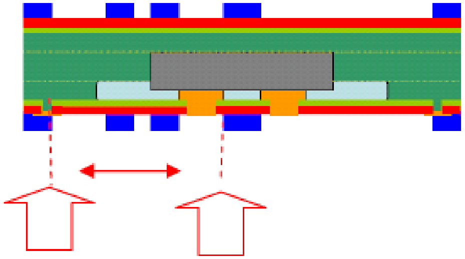


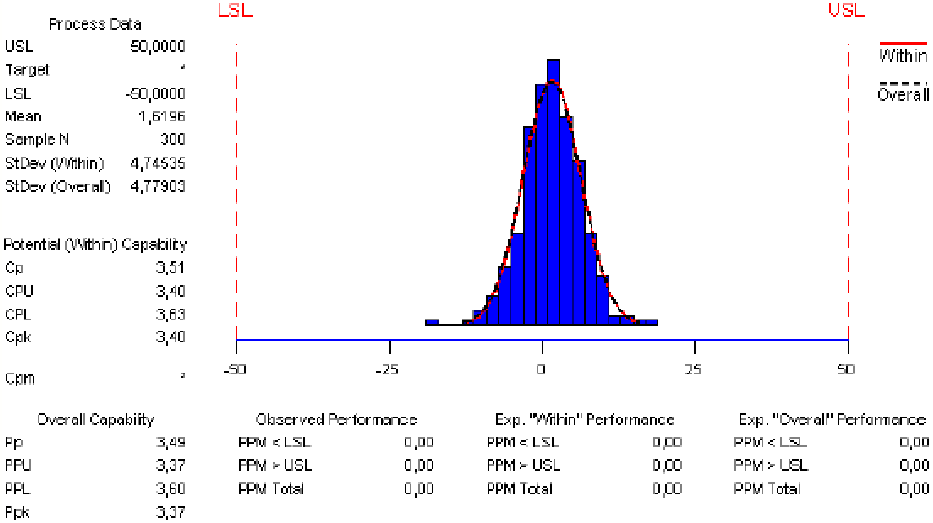


	20 Nozzle head	**Twin head**
Max. speed	20000 comp/h	3700 comp/h
Accuracy specified	+/- 55 µm, +/- 0,7°	+/- 30 µm, +/- 0,07°
Accuracy measured	**+/- 20 µm, +/- 0,035°**	**+/- 11 µm, +/- 0,025°**

25 µm technology

- Exposure with LDI – registration fiducial to pattern





Process Data	
USL	50,0000
Target	*
LSL	-50,0000
Mean	1,6196
Sample N	300
StDev (Within)	4,74535
StDev (Overall)	4,77903

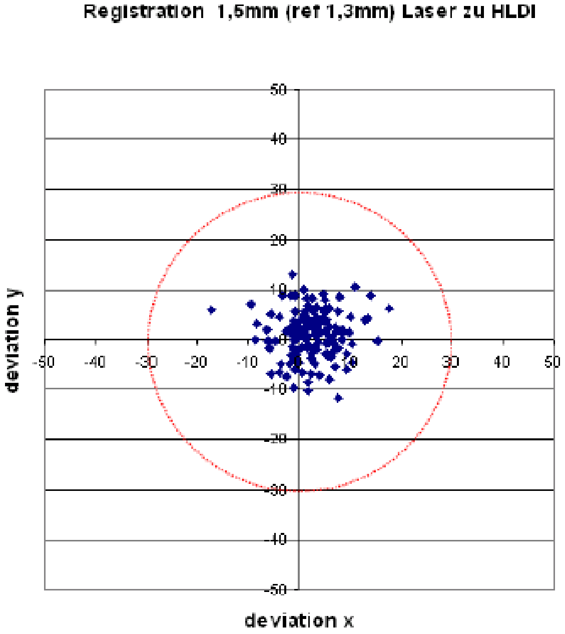
Potential (Within) Capability	
Cp	3,51
CPU	3,40
CPL	3,63
Cpk	3,40
Cpm	*

Overall Capability	
Pp	3,49
PPU	3,37
PPL	3,60
Ppk	3,37

Observed Performance	
PPM < LSL	0,00
PPM > USL	0,00
PPM Total	0,00

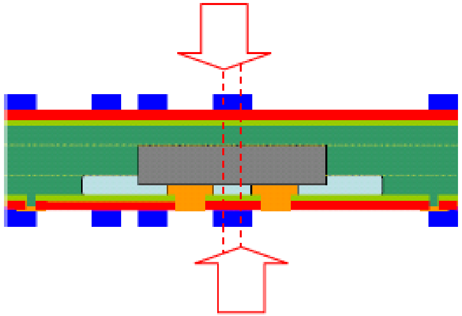
Exp. "Within" Performance	
PPM < LSL	0,00
PPM > USL	0,00
PPM Total	0,00

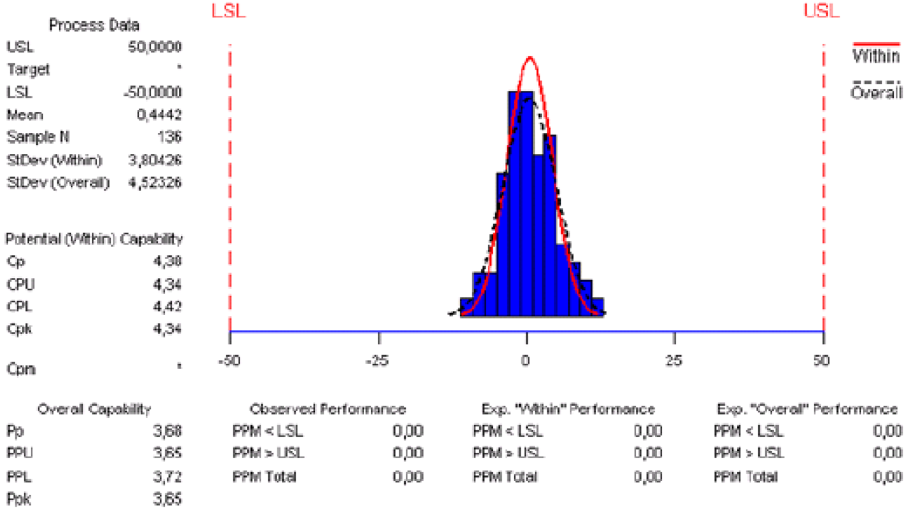
Exp. "Overall" Performance	
PPM < LSL	0,00
PPM > USL	0,00
PPM Total	0,00



25 µm technology

- Exposure with LDI – registration front to back





Process Data	
USL	50,0000
Target	*
LSL	-50,0000
Mean	0,4442
Sample N	136
StDev (Within)	3,80426
StDev (Overall)	4,52326

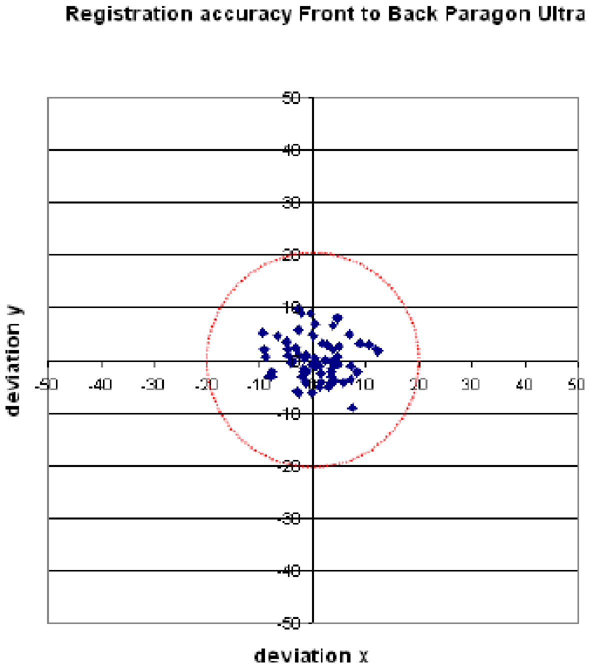
Potential (Within) Capability	
Cp	4,38
CPU	4,34
CPL	4,42
Cpk	4,34
Cpm	*

Overall Capability	
Pp	3,68
PPU	3,65
PPL	3,72
Ppk	3,65

Observed Performance	
PPM < LSL	0,00
PPM > USL	0,00
PPM Total	0,00

Exp. "Within" Performance	
PPM < LSL	0,00
PPM > USL	0,00
PPM Total	0,00

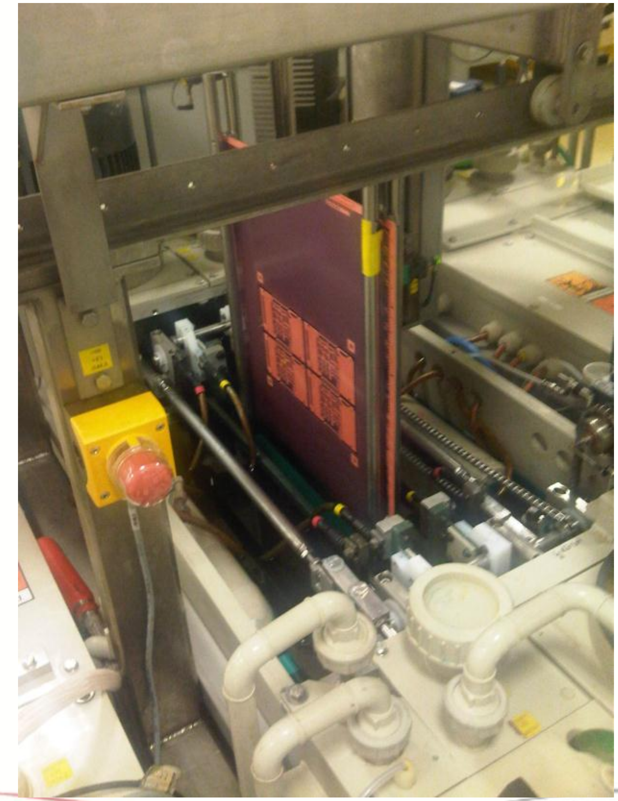
Exp. "Overall" Performance	
PPM < LSL	0,00
PPM > USL	0,00
PPM Total	0,00



Registration accuracy Front to Back Paragon Ultra

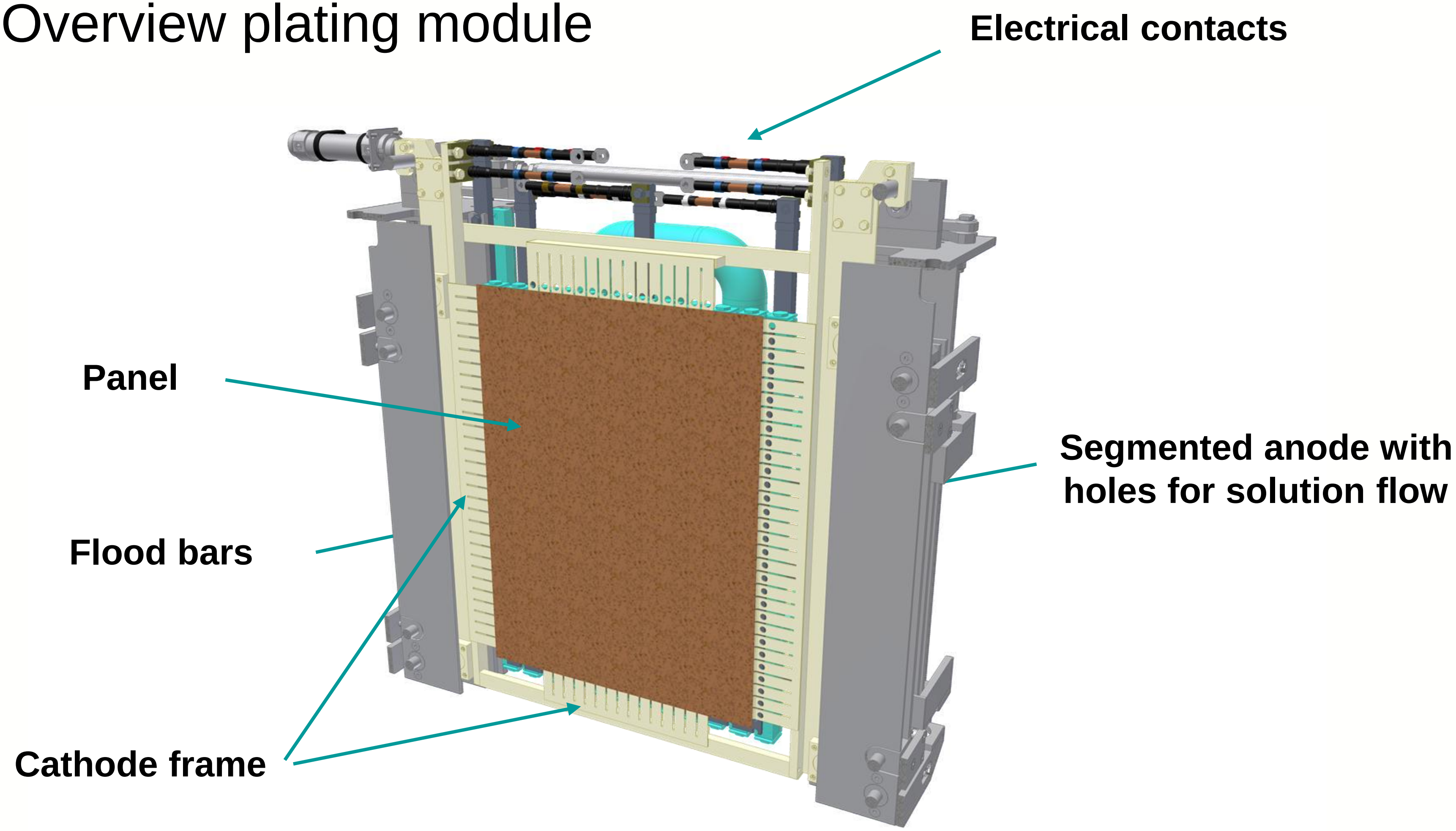
25 µm technology

- Semi-additive technology – single board plater
  - Individual control of parameters of each panel
  - Handling of thin cores
  - Unique flow system
  - Pulse plating for via filling
  - Full traceability of process data
  - Single piece flow for improved
    - Flexibility
    - Risk management

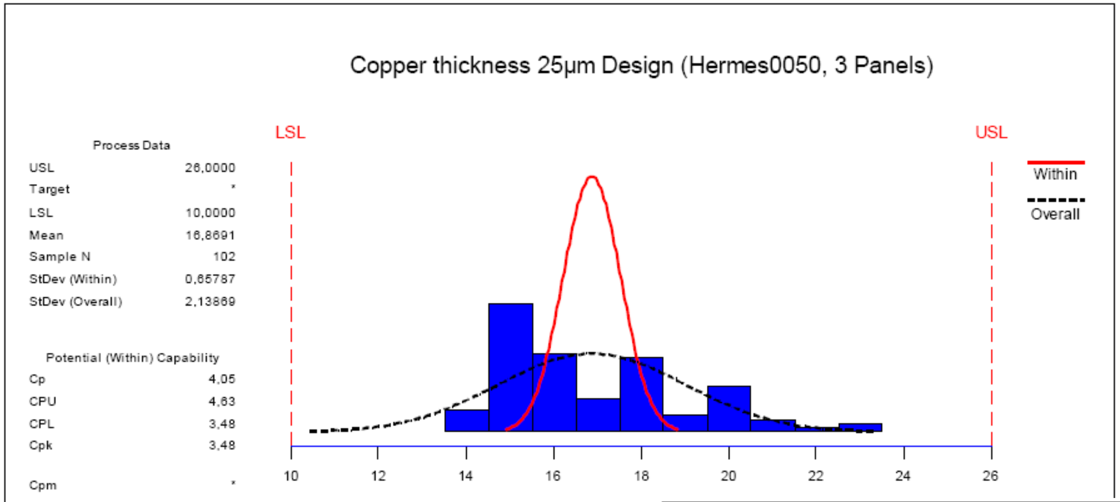


Single Board Processor Plating Module for PCB

- Overview plating module


Electrical contacts
Panel
Segmented anode with holes for solution flow
Flood bars
Cathode frame

25 µm technology



Process Data	
USL	26,0000
Target	*
LSL	10,0000
Mean	16,8691
Sample N	102
StDev (Within)	0,65787
StDev (Overall)	2,13869

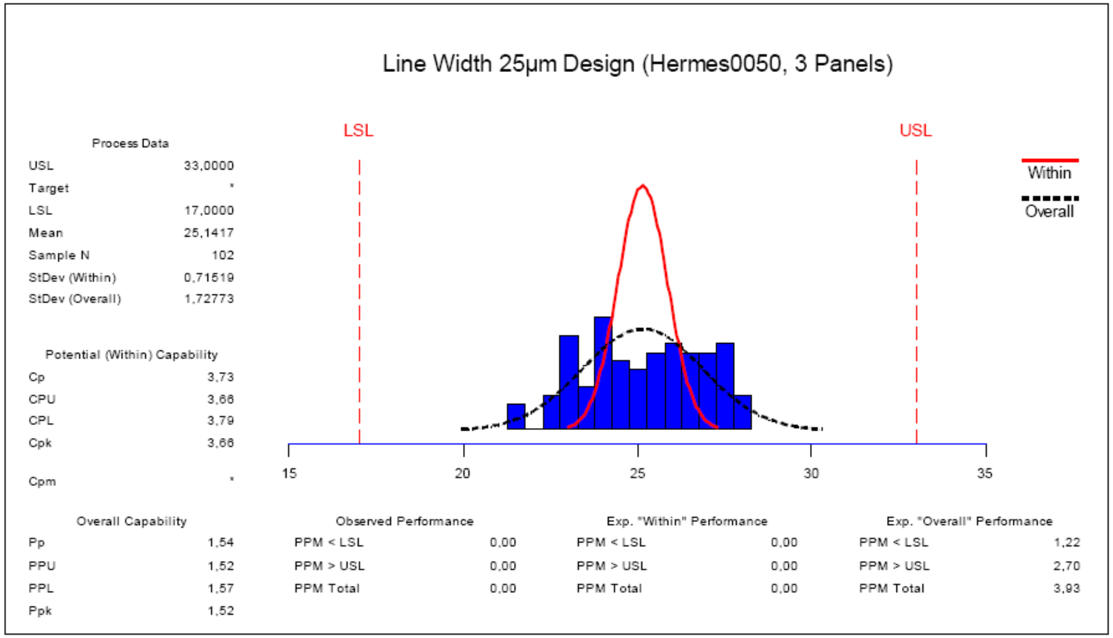
Potential (Within) Capability	
Cp	4,05
CPU	4,63
CPL	3,48
Cpk	3,48
Cpm	*

Overall Capability	
Pp	1,25
PPU	1,42
PPL	1,07
Ppk	1,07

Observed Performance		Exp. "W	
PPM < LSL	0,00	PPM < LSL	
PPM > USL	0,00	PPM > USL	
PPM Total	0,00	PPM Total	

Copper thickness ▲

Final line width ▼



Process Data	
USL	33,0000
Target	*
LSL	17,0000
Mean	25,1417
Sample N	102
StDev (Within)	0,71519
StDev (Overall)	1,72773

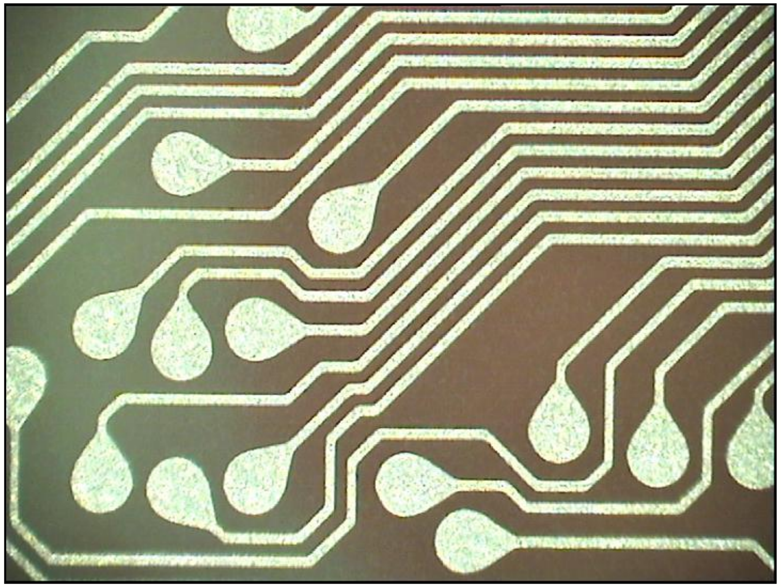
Potential (Within) Capability	
Cp	3,73
CPU	3,66
CPL	3,79
Cpk	3,66
Cpm	*

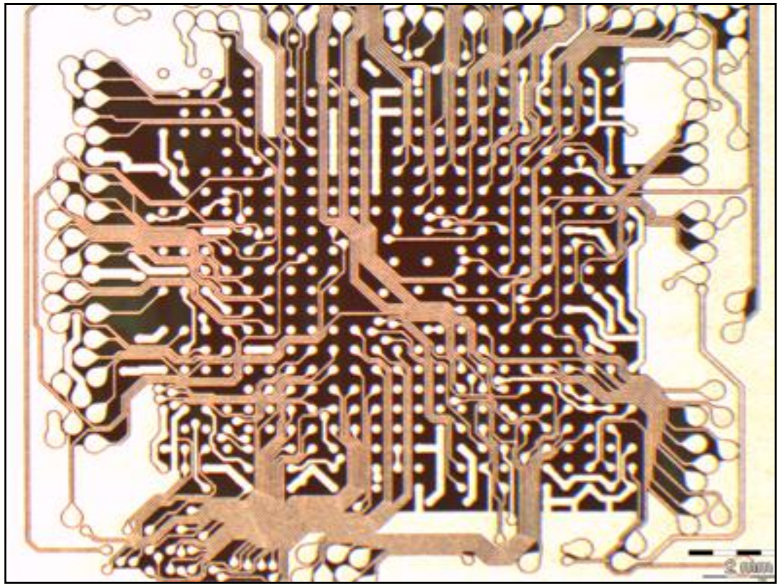
Overall Capability	
Pp	1,54
PPU	1,52
PPL	1,57
Ppk	1,52

Observed Performance		Exp. "Within" Performance		Exp. "Overall" Performance	
PPM < LSL	0,00	PPM < LSL	0,00	PPM < LSL	1,22
PPM > USL	0,00	PPM > USL	0,00	PPM > USL	2,70
PPM Total	0,00	PPM Total	0,00	PPM Total	3,93

25 µm technology

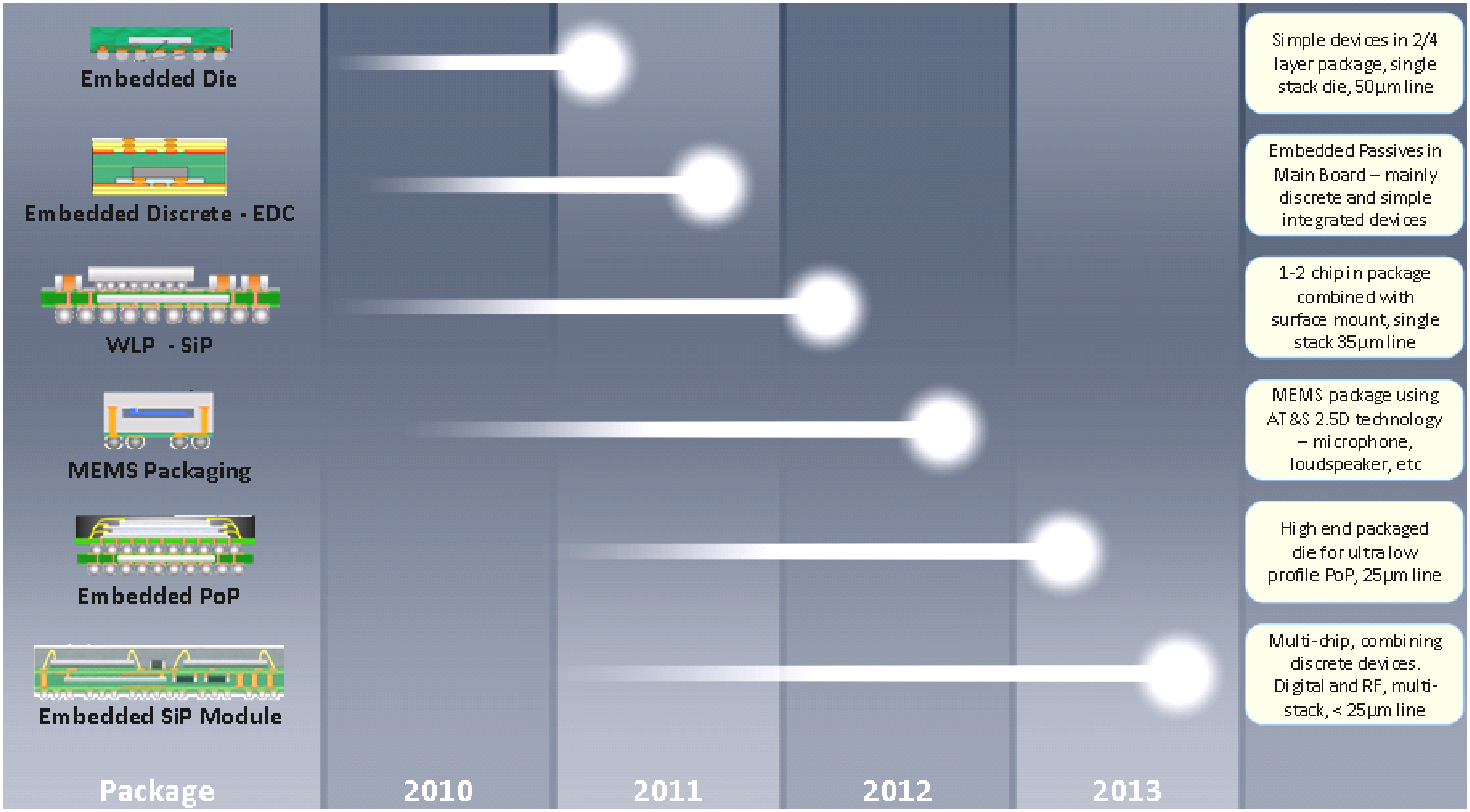
Design of motor management module





500 µm
500 µm
500 µm

Outlook for embedded modules
Industrialization Roadmap



Embedded Die

Embedded Discrete - EDC

WLP - SiP

MEMS Packaging

Embedded PoP

Embedded SiP Module

Package

2010

2011

2012

2013

Simple devices in 2/4 layer package, single stack die, 50µm line

Embedded Passives in Main Board – mainly discrete and simple integrated devices

1-2 chip in package combined with surface mount, single stack 35µm line

MEMS package using AT&S 2.5D technology – microphone, loudspeaker, etc

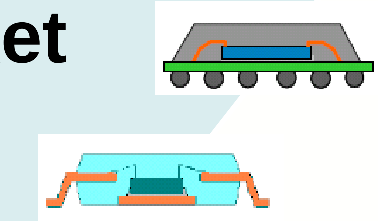
High end packaged die for ultra low profile PoP, 25µm line

Multi-chip, combining discrete devices. Digital and RF, multi-stack, < 25µm line

Embedding Business

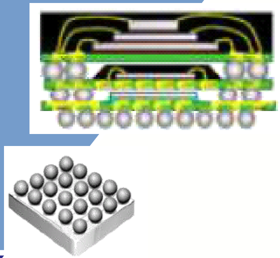
GLOBAL IC Packaging market

~ 270 Bunits by 2013



TAM for «Embedding Ready» Components

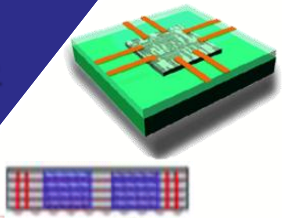
~ 20 Bunits by 2013



SAM for Embedded Components

~ 3 Bunits

by 2013



TAM = Total Available Market for Embedded Components

SAM = Served Available Market

Thank you for your attention

For more information, go to our Hermes website

http://www.hermes-ect.net