Organic Flip Chip Packages for Use in Military and Aerospace Applications

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Contents

Reliability needs of High End Commercial Products

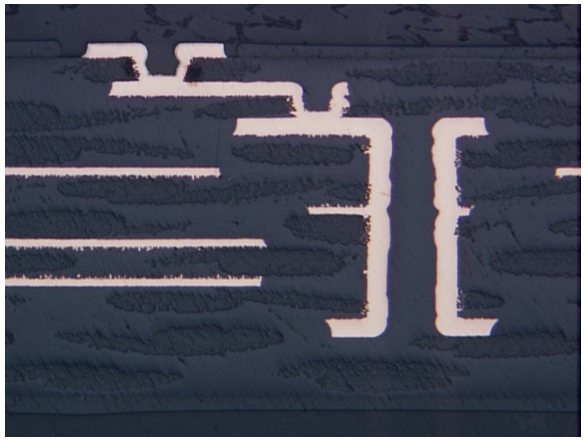
- Server & Telecom (Servers, Routers, Hubs & High Speed Switches)
  - High reliability requirements
    - Minimum 10 years life
      - Component on PCB stressing from 0 to 100C and 3,600 cycles to first failure
      - Component only stressing from -55 to +125C and 1000 cycles to first failure
  - High power requirements, 50 to 100 watts are common
  - High signal densities, > 1700 signals in a 52.5mm BGA
  - High electrical performance, 12.5 GB/s
  - Companies in these markets are building equipment for satellite applications
  - Stringent Shock and Vibration requirements

- High End Commercial Applications have driven development of technologies that can bridge to Military / Aerospace

Wire Bond Packaging: Aerospace

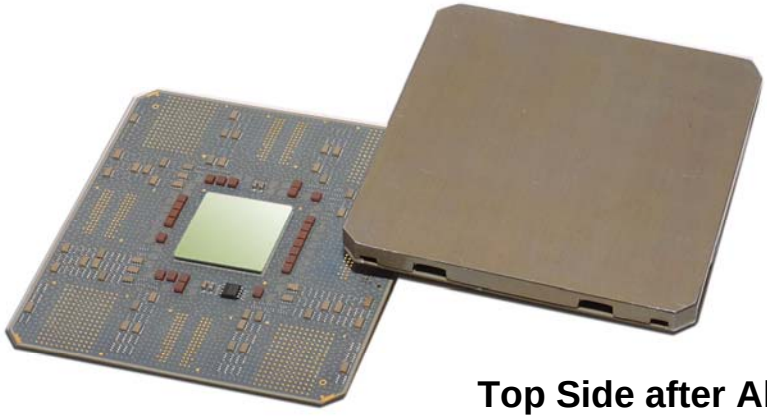
- Aerospace : 1st plastic BGA for Satellite
  - Chip Up
  - > 700 BGA I/O, 42.5mm body
  - > 300 signals
  - 2 signal, 4 layer Cavity PBGA
  - 75 micron lw/ls
  - 16.6mm die
  - Commercial Overmold

Wirebond Build Up Package: Military



- 35mm WB CU PBGA
  - 2-6-2 X Section (10 layer), 7 Signals, 3 Pwr/Gnd
  - 37.5mm body size
  - 864 micron total thickness
  - 69 micron thick top BU layer thickness
  - 75 micron lw, 53 micron ls
  - BU vias are 100 micron CO_2 laser drilled
    - 250 micron pads in outer most BU layers
    - 300 micron (12mil) pads on Inner BU layers
    - Stacked BU vias
  - Core vias are 200 micron dia. mechanical drilled on 400 micron pads
- Can be either WB or FC, SIP or SC
- Glass reinforced Polyimide – Nelco 7000 2HT
  - Er: 4.26 @ 1 to 2.5GHz (50% resin content)
  - Dielectric Loss: .009 @ 1GHz (50% resin content)
  - Tg: >250C

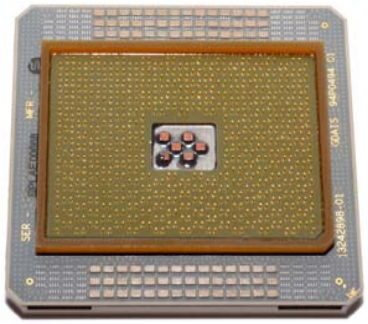
PTFE Based Flip Chip SiP's: Military



Substrate after die attach

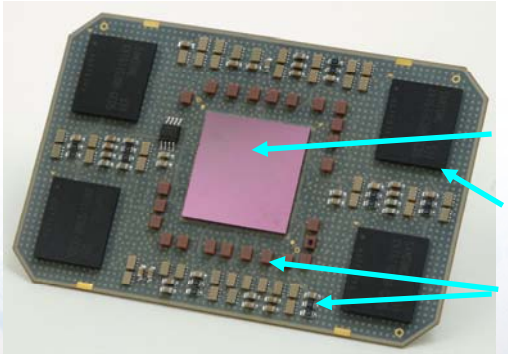
Top Side after Al lid attach

65 x 63 mm



Component Bottom side with Pinned Connector

- **System in Package (ASIC / CSP memory and decaps)**
  - ✓ **Server Processor Packages:**
    - ➢ **18 mm die size**
    - ➢ **2 signal layers, 280 signals**
    - ➢ **250 micron die pad pitch**
    - ➢ **CSP memory**
    - ➢ **Top and bottom decaps**
    - ➢ **630 I/O SMT PGA connector**



65 x 43 mm

Weight Comparisons for Plastic vs Ceramic 40mm body size

Substrate	Approximate substrate weight (gm)
Ceramic (30 layer, alumina, 10mil/layer)	48.0
Ceramic (15 layer, alumina, 10 mil/layer)	24.0
PTFE BGA 9 layer substrate	2.3
Thin core build up 10 layer substrate	2.9
Thin core build up 6 layer substrate	2.0

High End Telecom and Server Applications using Flip Chip Plastic

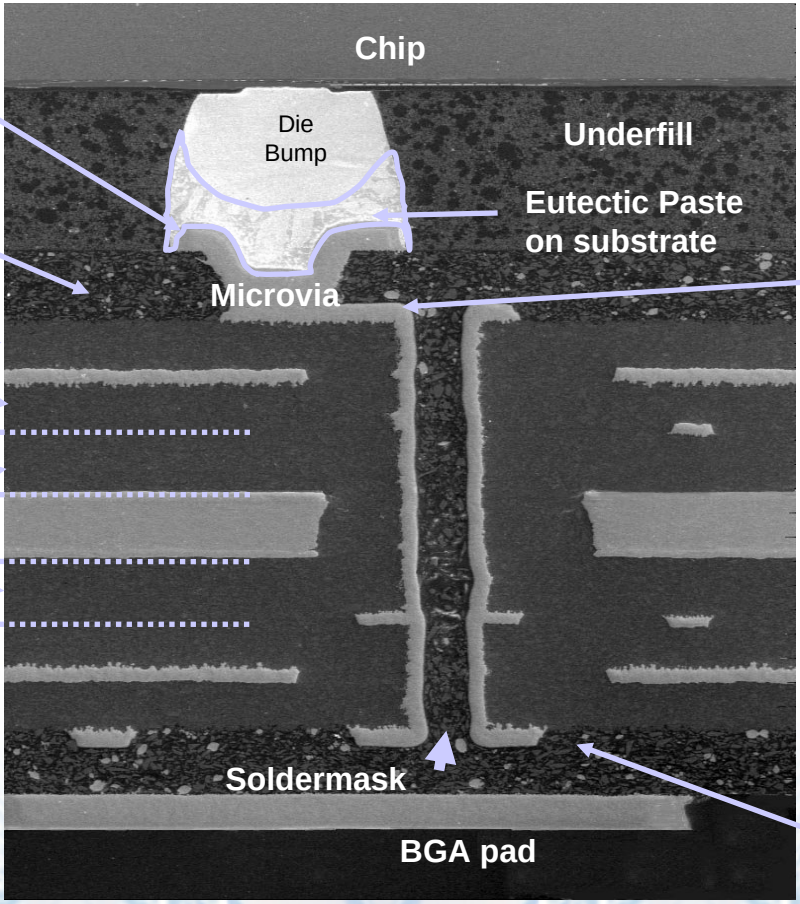
- Drivers are similar to Military/Aerospace
  - Package shrink is critical, weight not as large a concern
  - High speed signals with low noise
    - Clean eye's at 12.5 Gb/s in production
    - 600 differential pairs are common
  - High BGA/LGA/PGA I/O with min. 10 yr field life
    - 52.5 mm, 2577 BGA I/O, 1 mm BGA pitch in high frequency routers
    - 90nm Si technology
    - 25 micron lw/ls
    - 200 micron Flip Chip die pad pitch, 16 rows deep
  - Low volume applications, some need to remain on shore

Highlights of Advanced Plastic Flip Chip Packaging

- 50 micron UV laser drilled vias
  - Fine pitch (less than 200 micron), for full access to wiring planes
- 12 micron thick Copper Conductors
  - 25 micron Line Width
- Thin Core and Coreless Technologies
- Thin Substrates (0.4 to 0.6 mm thick)
- Build up dielectric layer thickness available 35 to 50 microns
- Low-stress PTFE and Particle Filled Epoxy Dielectrics
  - Low-k dielectrics: High Frequency, Low-Noise applications
  - Er = 2.7 for PTFE, Er = 3.7 for thin-core buildup
- Solder Bumped Copper Die Pads

Overview: Typical PTFE 9 layer Cross Section - HyperBGA®

Module showing die and bump



Non soldermask defined Pad

Soldermask: 40 micron thick Epoxy Based, Er = 3.2

PTFE: 35 micron thick, Er = 2.7

PTFE on CIC: 50 micron thick, Er = 2.7

Dogbone Escape (TSR): 15 micron thick Cu

V1 Power:12 micron Cu

S1 Signal: 12 micron Cu

Gnd Cu/Invar/Cu: 6/38/6 micron thick

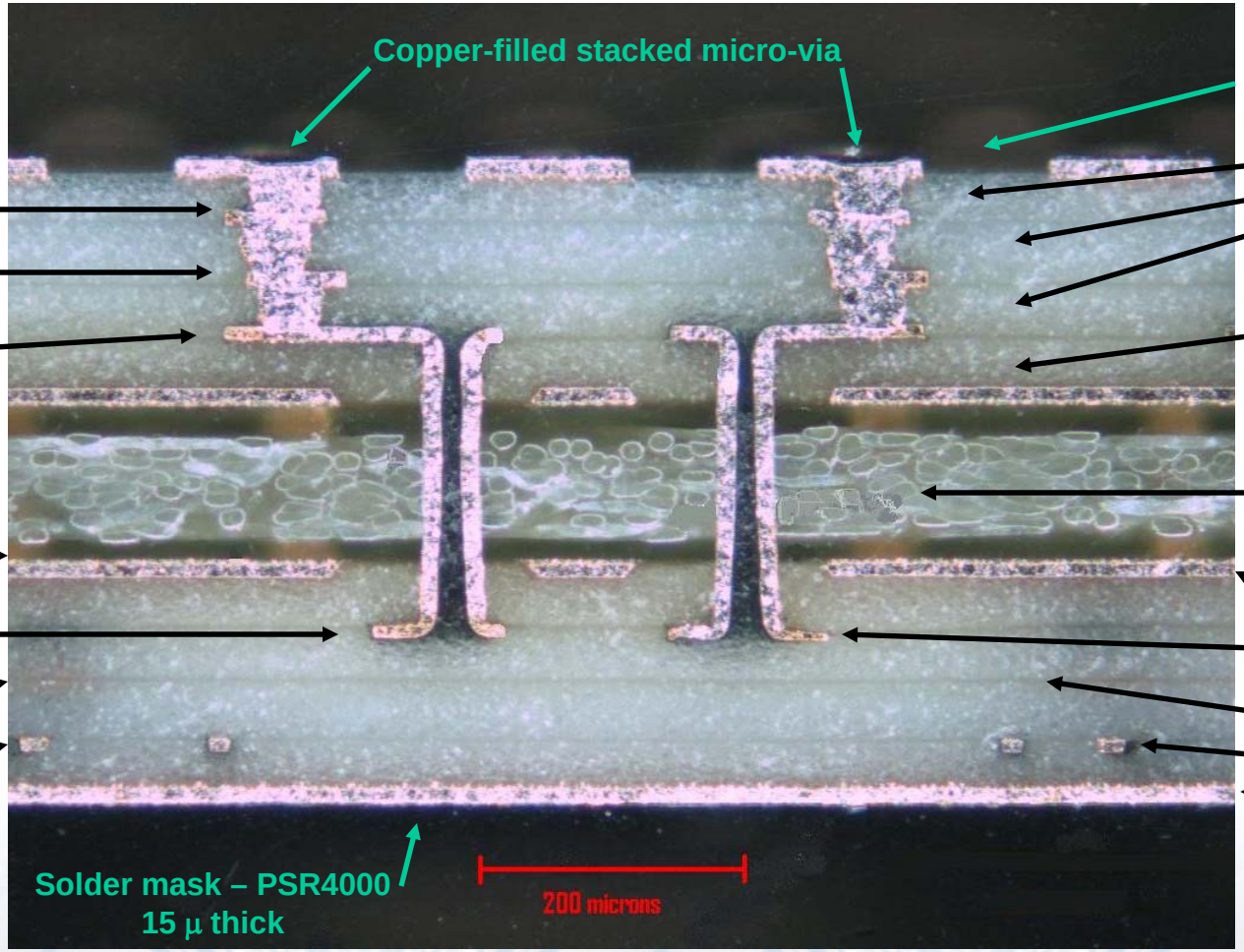
S2 Signal: 12 micron Cu

V2 Power:12 micron Cu

Escape layer (BSR): 15 micron thick Cu

Substrate thickness - .47 mm

Overview: Typical Thin Core 10 layer Cross Section - CoreEZ®



Gnd / Top
S1
Pwr / Gnd
S2
Pwr / Gnd
Pwr / Gnd
S3
Pwr / Gnd
S4
Gnd / Bot

Solder mask PSR4000
15 µ thick
Build up layer 1
Build up layer 2
Build up layer 3
DriClad, 35/50 µ thick
Outter Core dielectric
DriClad, 35/50 µ thick
Inner Core
100/150µ thick
Thermount
Core Cu
12 µ thick
Build up Cu 1
Build up Cu 2
Build up Cu 3
12 µ thick

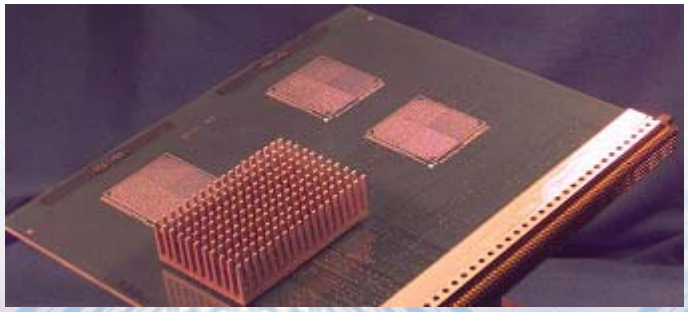
Substrate Thickness – 0.55 mm

Typical PTFE Package Reliability Performance

TEST	FORMAT	DURATION	RESULT
Preconditioning - JEDEC Level 3	Component	96H	N/A
Thermal Cycle (0/100'C)	Card	3600 Cycles	pass
Power Cycling (25/125'C)	Card	3600 Cycles	pass
DeepThermal Cycling (-55/+125C)	Component	1000 Cycles	pass
Wet Thermal Shock (-40 / +125 C)	Component	100 Cycles	pass
T. H. & B. (85 'C / 85%RH/3.7 V)	Card	1000 Hours	pass
HAST (110 'C / 85%RH/3.7V)	Card	264 Hours	pass
Pressure Pot (121 'C / 100% RH/2atm)	Component	96 Hours	pass
High Temp. Storage (150 'C)	Component	1000 Hours	pass
Low Temp. Storage (-65'C)	Component	1000 Hours	pass
Shock/Vibration JEDEC	Component	various	pass

Component level testing is die assembled to substrate with underfill, lid and BGA balls, card level testing is component assembled to PCB

Module w/ HS on 9x10 inch card



0 to 100ºC Accelerated Thermal Cycle Reliability Component Attached to PCB

Failure Mode	Ceramic BGA ATC Life (cycles)	PTFE BGA ATC Life (cycles)	Thin Core Build Up ATC Life (cycles)
Package Internal	>10,000	>10,000	>5000
Flip Chip Joint	>10,000	>10,000	>5000
BGA Corner Joint	800 to 2,000	> 10,000	>5000
BGA Chip Edge Joint	>10,000	>10,000	5000; extendable to 10,000 with optimized design

- Includes Precondition Stress as JEDEC-020C Moisture Resistance level 4 with 3x Reflows
- Package size 42-52mm; Both PTFE and Thin Core exceed ceramic package reliability

Flip Chip Package Wireability Comparison

Substrate	# of Signal layers	Signal Wiring Escapes per mm of die edge per layer
Ceramic, 30 layers	12	2.7
PTFE BGA, 9 layers	2	4.4
Thin Core Build Up 6 layers	2	5.9
Thin Core Build Up 10 layers	4	7.0

Organic Flip Chip Package Outgassing Performance

- **Materials**
  - **Rogers 2800 PTFE**
  - **Asahi APPE**
  - **Driclad Epoxy**
  - **Thermount 55LM**
  - **PSR4000**
- **Maximum of 1.0% Total Mass Loss**
  - **All materials & finished substrates < 1.0%**
- **Maximum 0.1% Collected Volatile Condensable Materials**
  - **All materials & finished substrates < 0.1%**

Evaluation of Materials Subjected to Various Radiation Levels

- **Evaluated PTFE BGA (HyperBGA®) and Thin Core (CoreEZ ®) materials radiation response**
  - **Radiation Exposure**: Co60 Gamma:
    - **Control**
    - **32, 50, 100, 300, 500, 700, 1000 and 5000 krad TID**
  - **PTFE Materials evaluated**: Rogers 2800, Asahi APPE
    - **Results**: **Many applications will be unaffected by radiation**
      - **APPE has no measurable degradation to 5 Mrad**
      - **R2800 shows gradual loss of ductility with exposure**
  - **Thin Core Build Up Materials Considered**: Thermount 55LM, Particle Filled Driclad Epoxy, PSR4000
    - **Results: No measurable change of mechanical properties through 5 Mrad**

Material Ductility Test with tensile stretch of film sample – PTFE example

Sample geometries:

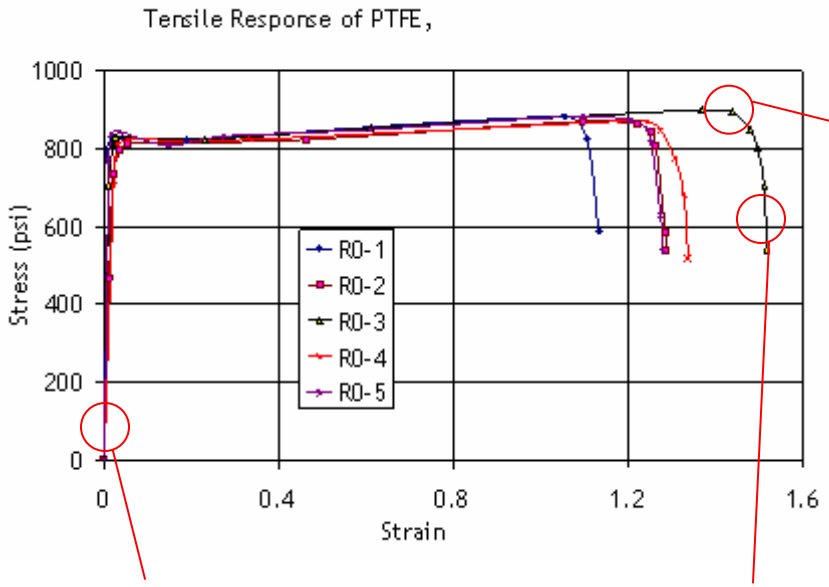
½" wide, 6" length

Thickness as used in application, <0.010"

Monotonic Stretch to Failure

Crosshead rate: 0.025"/min

5-10 samples per condition, average failure strain found



Criteria for failure – onset of load loss

Start

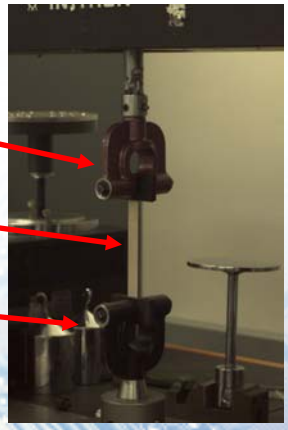
Stretch

Fracture (at ductility limit)

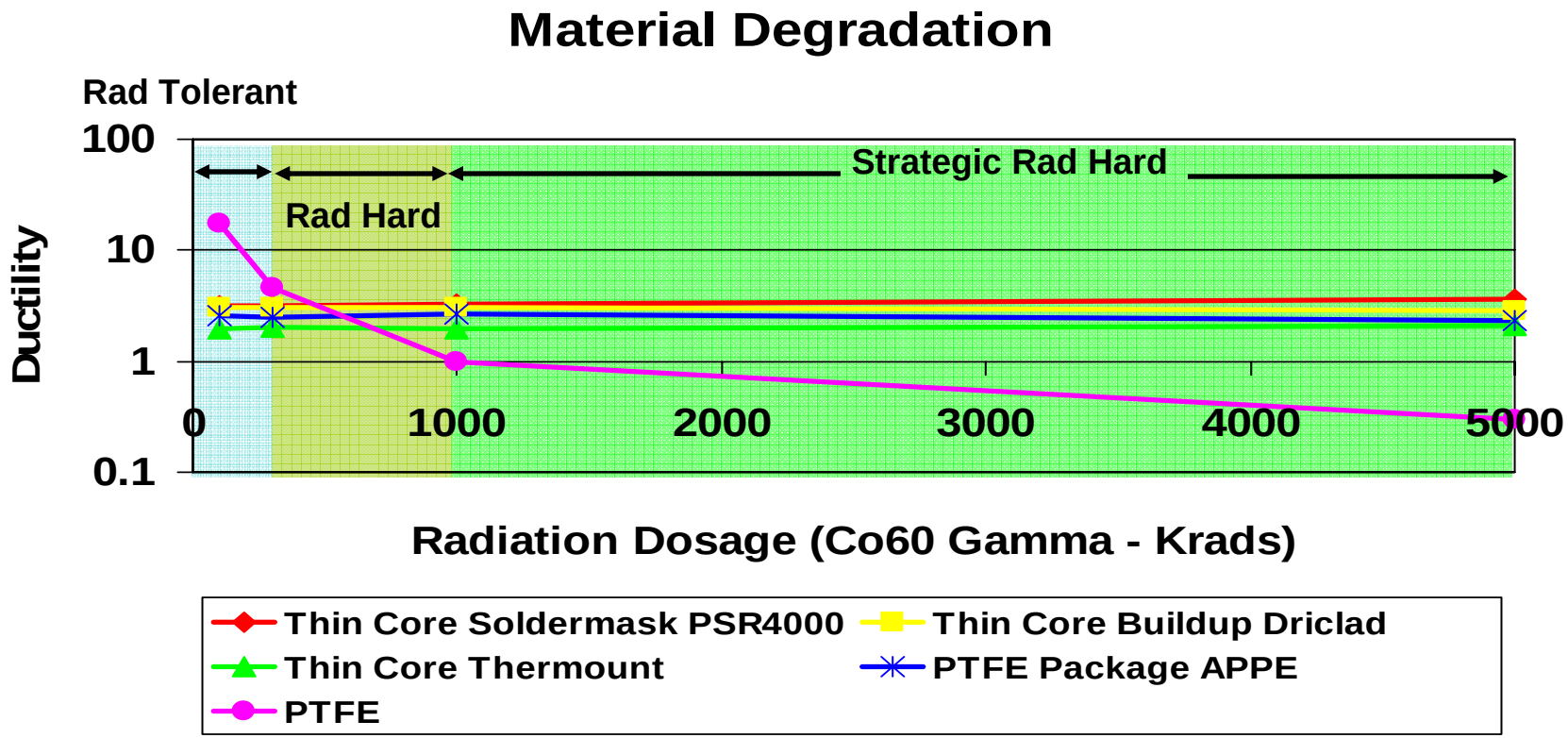
Moving Crosshead

Material Sample

Fixed Crosshead



EI's packaging performance after radiation exposure



- ✓Ductility performance indicates package performance in thermal cycling
  - ➢Thin Core Build Up appears to be a good choice for Rad Hard and Strategic apps.
    - •materials show no ductility degradation with radiation level
  - ➢PTFE appears to be best suited for Rad Tolerant applications
    - •PTFE ductility is higher then all other materials below 300K rad exposure
    - •PTFE predictably degrades significantly above 300Krad exposure levels

Conclusions

- Flip Chip PBGA Packages are Suitable for Military / Aerospace Applications
  - Reliability
  - Wireability
  - Outgassing
  - Radiation Exposure
- Significant Weight Savings Realized with PBGA Packages
- Advantage to Overall Life Costs and Performance

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