Introduction 1

1.1 Overview Of Intel Packaging Technology

As semiconductor devices become significantly more complex, electronics designers are challenged to fully harness their computing power. Transistor count in products is expected to exceed 100 million. With a greater number of functions integrated on a die or chip of silicon, manufacturers and users face new and increasingly challenging electrical interconnect issues. To tap the power of the die efficiently, each level of electrical interconnect from the die to the functional hardware or equipment must also keep pace with these revolutionary devices. Package design has a major impact on device performance and functionality.

Today, submicron feature size at the die level is driving package feature size down to the design-rule level of the early silicon transistors. At the same time, electronic equipment designers are shrinking their products, increasing complexity, setting higher expectations for performance, and focusing strongly on reducing cost. To meet these demands, package technology must deliver higher lead counts, reduced pitch, reduced footprint area, provide overall volume reduction, aid in system partitioning, and be cost effective.

Circuit performance is only as good as the weakest link. Therefore, a significant challenge for packaging is to insure it does not gate device performance. While packaging cannot add to the theoretical performance of the device design, it can have adverse effects if not optimized. Package performance, therefore, is the best compromise of electrical, thermal, and mechanical attributes, as well as the form factor or physical outline, to meet product specific applications, reliability and cost objectives.

The continuing demand for higher performance products is requiring levels of package performance unattainable by the molded plastic and ceramic packages of the past decade. These factors have driven a variety of major innovations in Intel packaging. Intel had in past years introduced organic packaging with copper interconnect for improved electrical characteristics. Intel has recently introduced flip chip between die and package as an interconnect approach to further improve performance and offer very compact packaging. This has resulted in new classes of technology using organic substrates for both surface mount (Organic Land Grid Array - OLGA) and thru-hole (Flip Chip Pin Grid Array - FCPGA). The microPGA (µPGA) was introduced to combine flip chip interconnect with a very small form factor and socketability for compact and portable systems. While these packages differ in form factor, all can provide the required electrical and/or thermal performance needed by our advanced products.

Chip scale packaging for memory applications has also been a focus of packaging innovations, with new CSP form factors including stacked die packaging. Portability is expected to continue as a strong driver of new packaging approaches.

Fit, form, and function tend to be market specific. Certain Intel devices serve more than one market need but may require different package attributes. Therefore, "one size fits all" is not a practical approach to device packaging. Packaging technology is not a single technology, but instead consists of more than 20 industry proven combinations of core technologies or core technology sets that can be categorized by package families.

In support of the growing number of Intel devices and to meet the industry demand for package-specific applications, Intel's package portfolio has more than doubled during the past ten years.

1.2 Purpose Of This Databook

Intel's Packaging Databook serves as a data reference for engineering design, and a guide to Intel package selection and availability. Each chapter provides a comprehensive and in-depth analysis of Intel packaging technology, from information on IC assembly, performance characteristics, and physical constants, to detailed discussions of surface mount technology and Intel shipping and packing.

Chapter 1 Introduction: An overview of package families, including package attributes, package types, and a package selection guide.

Chapter 2 Package / Module / PC Card Outlines and Dimensions: A detailed view of Intel package outlines and dimensions.

Chapter 3 Alumina & Leaded Molded Technology: Statistical tools used in the manufacturing process. Also included is a comprehensive analysis of Intel's IC assembly manufacturing technology and process flow.

Chapter 4 Performance Characteristics of IC Packages: Package characteristics and data for electrical, mechanical, and thermal IC package characteristics.

Chapter 5 Physical Constants of IC Package Materials: Physical constants of IC package materials. This chapter provides valuable information on mechanical, electrical, and thermal properties of case materials, lead/leadframes, and soldering material characteristics.

Chapter 6 ESD/EOS: An overview of electrical static discharge and electrical over stress.

Chapter 7 Leaded Surface Mount Technology (SMT): A review of the mass reflow soldering technologies of printed circuit board (PCB) component assembly termed SMT (surface mount technology).

Chapter 8 Moisture Sensitivity/Desiccant Packaging/Handling of PSMCs: Desiccant Packing Methods and Materials. The six levels of Moisture Sensitivity for packages is also examined.

Chapter 9 Board Solder Reflow Process Recommendations - Leaded SMT: A review of Board Solder Reflow Process Information.

Chapter 10 Transport Media and Packing: Various packing and shipping methods used at Intel. Packing media, desiccant pack materials, and shipping data are illustrated.

Chapter 11 International Packaging Specifications: A listing of international packaging specifications and a comprehensive resource library.

Chapter 12 Tape Carrier Package: A profile of the Tape Carrier Package and its uses in areas that require lightweight small footprint integrated circuits.

Chapter 13 Pinned Packaging: An overview of Plastic Pin Grid Array Package technology, and its physical structure, electric modeling and performance.

Chapter 14 Ball Grid Array (BGA) Packaging: A profile of the Intel Ball Grid Array technology detailing its physical structure, electrical modeling, performance, and other aspects of the BGA packaging.

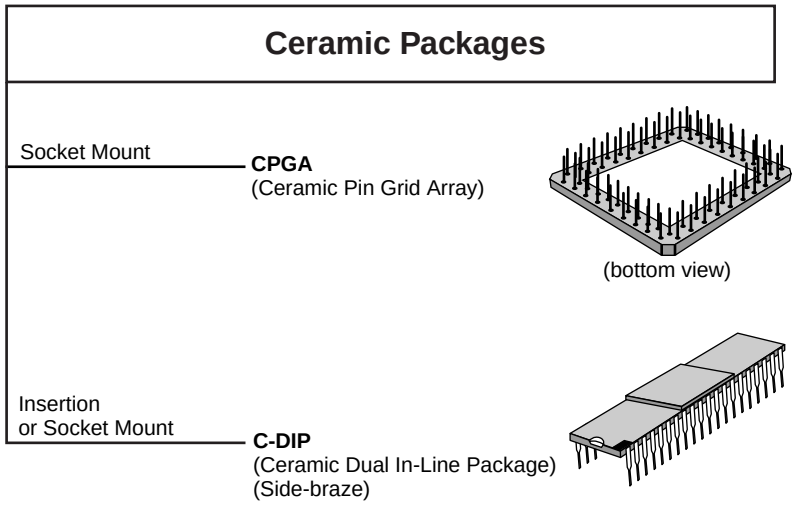
Chapter 15 The Chip Scale Package (CSP): An overview of Chip Scale Packaging, and its physical structure, electrical modeling, and performance.

Chapter 16 Cartridge Packaging: An overview of the Single Edge Contact Cartridge and its physical structure, electrical modeling, and performance.

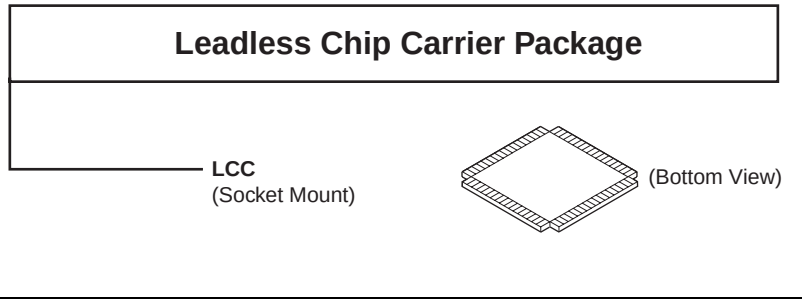
Glossary: Packaging Databook terminology defined.

1.3 Package Types

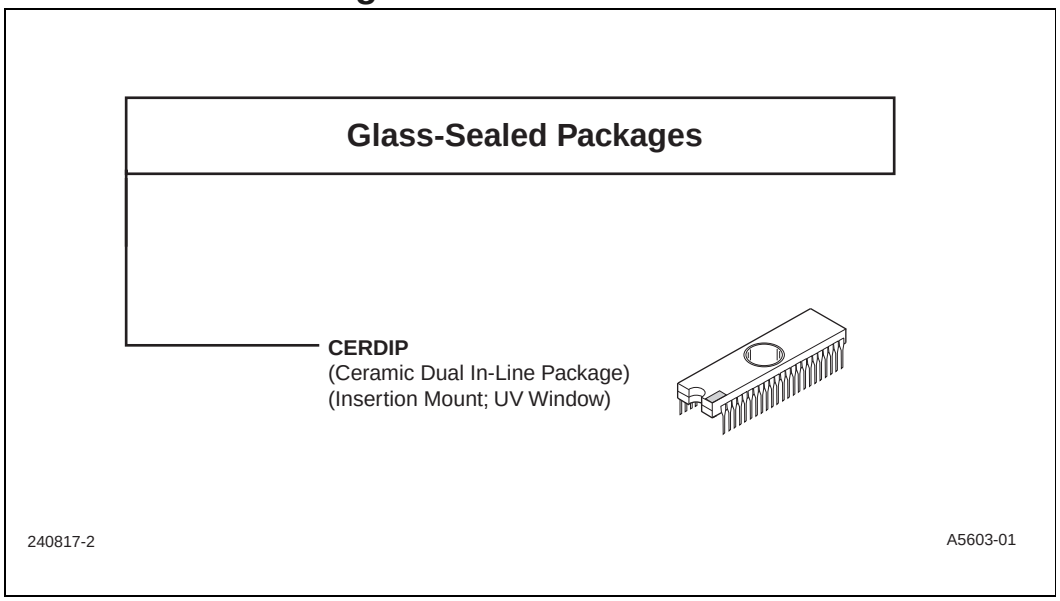
1.3.1 Ceramic Packages



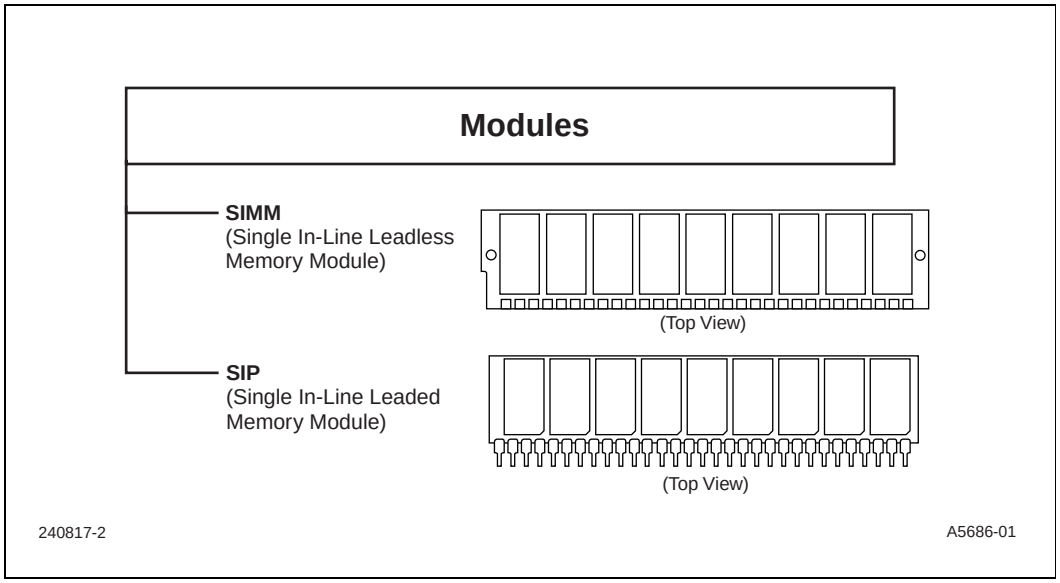
1.3.2 Leadless Chip Carrier Packages



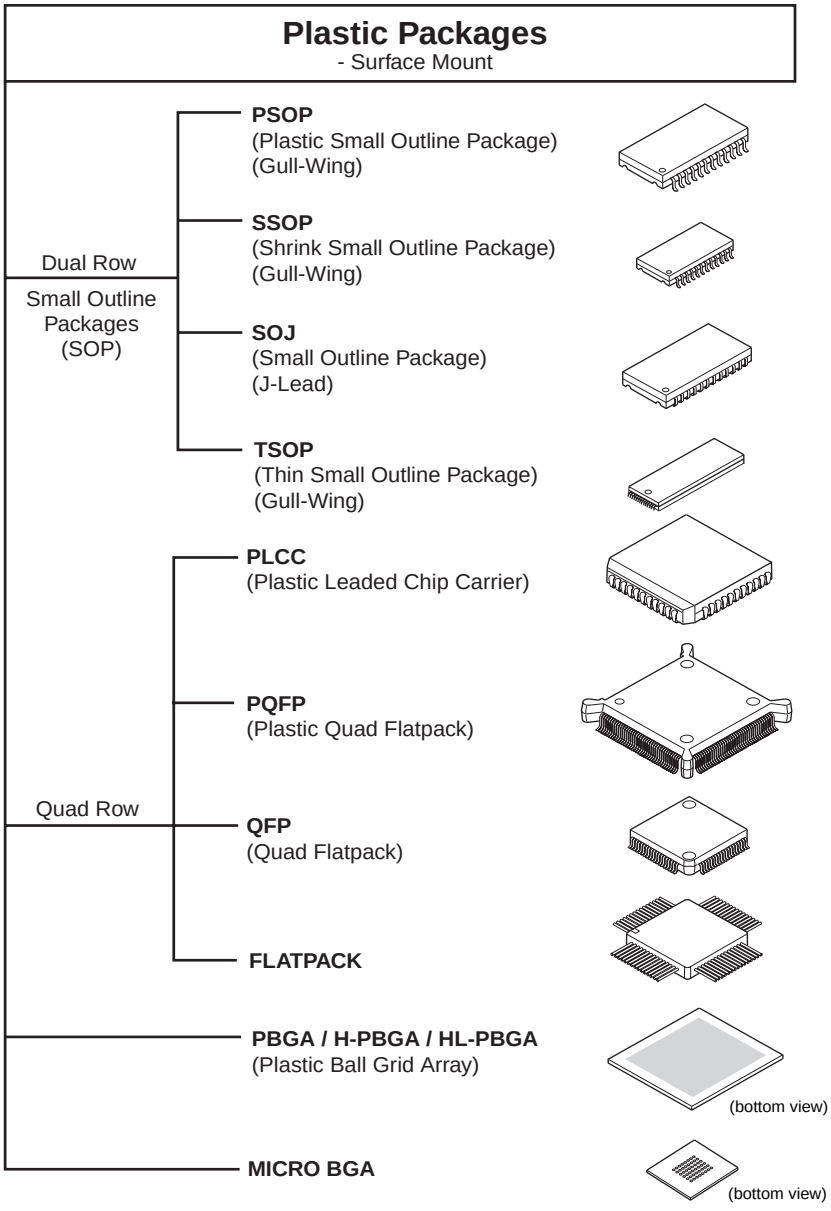
1.3.3 Glass-Sealed Packages



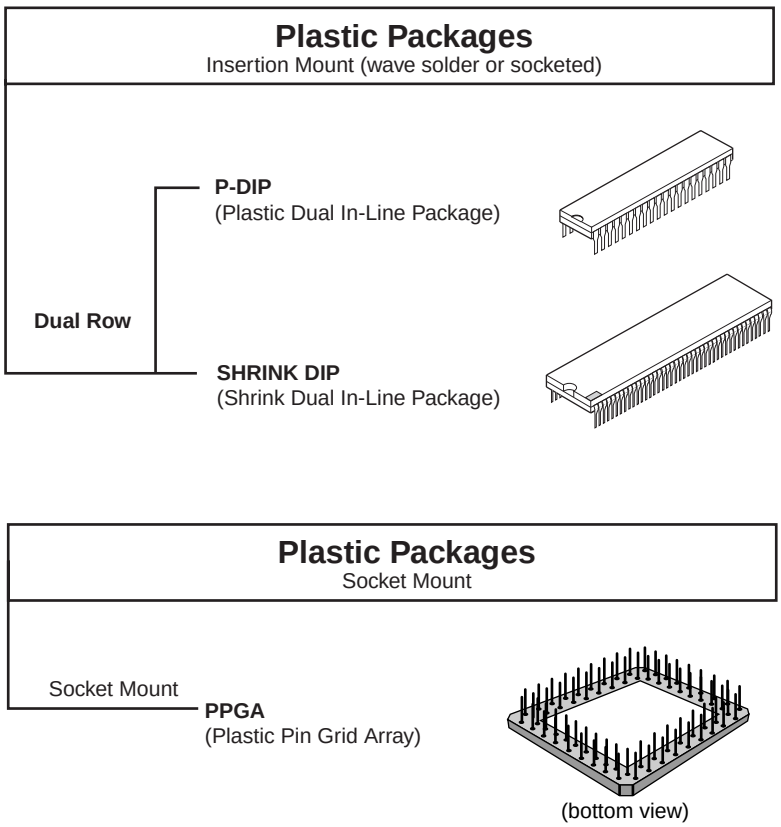
1.3.4 Modules



1.3.5 Plastic Packages - Surface Mount

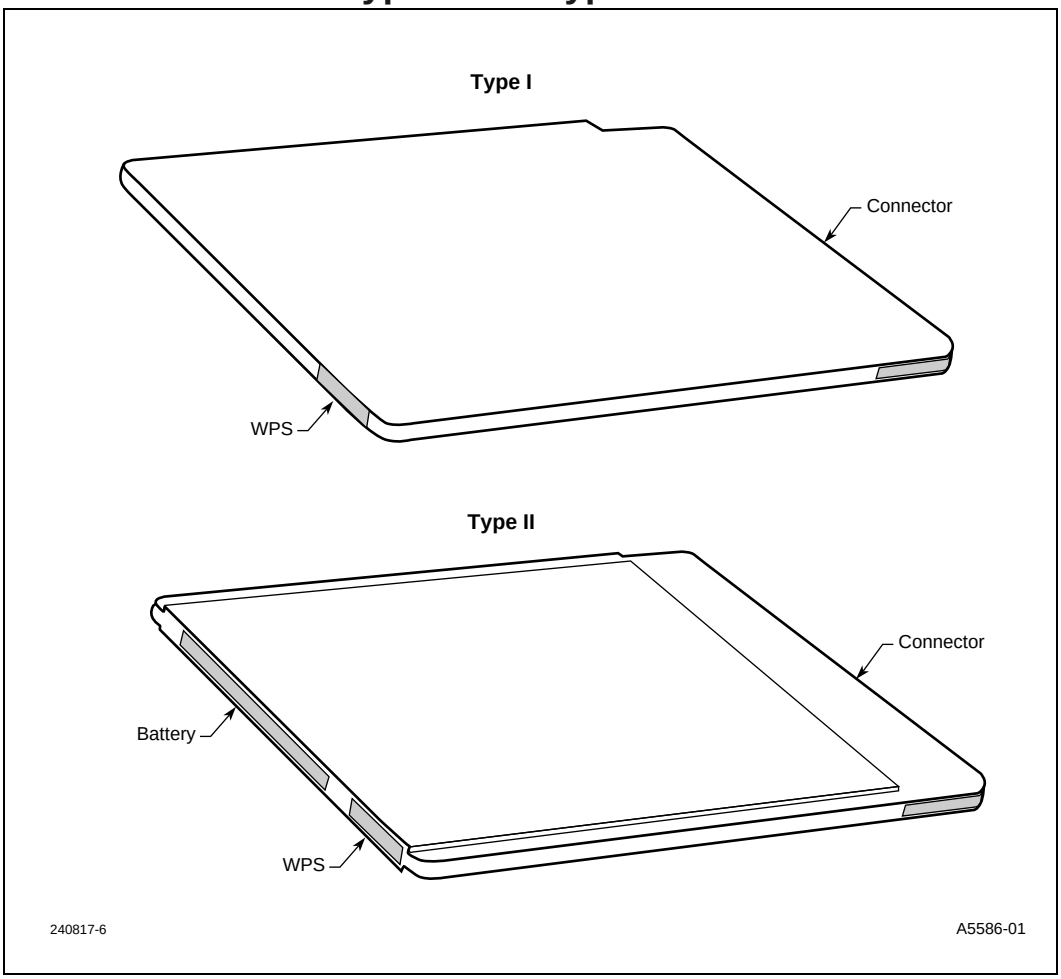


1.3.6 Plastic Packages - Insertion Mount/Socket Mount

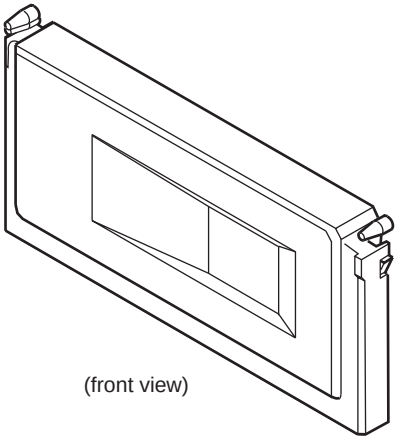


µPGA and FC-PGA can be found in Chapter 13 "pinned packages"

1.3.7 PCMCIA PC Card - Type 1 and Type 11



1.3.8 S.E.C. Cartridge (242 Contact)



(front view)

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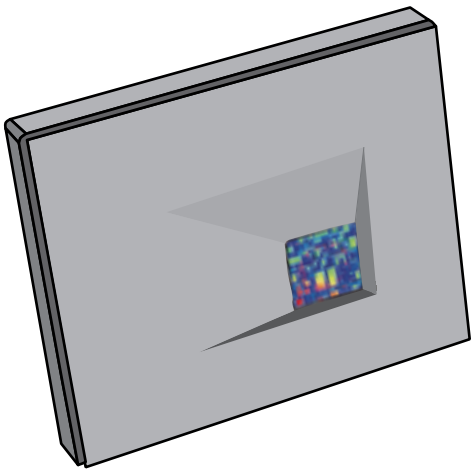
1.3.9 S.E.C. Cartridge (330 Contact)



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1.4 Package Attributes

Note: For Package Attribute information on Pinned Packages (Chapter 13), BGA (Chapter 14), and Chip Scale Packages (Chapter 15) please consult their individual chapters.

1.4.1 Ceramic Package Attributes

Table 1-1. Ceramic Dual In-Line Package (C-DIP)(Side Brazed)

Lead Count	40
Sq./Rect.	R
Pitch (Inches)	0.100
Package Thickness (Inches)	0.154* 0.123
Weight (gm)	
Max. Footprint (Inches)	2.020
UV Erasable	x
Shipping Media: Tubes	 x
Comments / Footnotes	* EPROM LID

Table 1-2. Leadless Chip Carrier (LCC)

Lead Count	68	68
Sq/Rect.	S	S
Pitch (Inches)	0.050	0.050
Package Thickness (inches)	0.096	0.130
Weight (gm)	4.67	4.67
Max. Footprint (Inches)	0.960	0.960
UV Erasable		x
Shipping Media: Tubes	x	x
Comments / Footnotes		

Table 1-3. Ceramic Pin Grid Array

Lead Count	68	68	68	88	88	132	168	208	240-280	272-320	387
Sq/Rect.	S	S	S*	S	S	S	S	S	S	S	R
Pitch (Inches)	0.100	0.100	0.100	0.100	0.100	0.100	0.100	0.100	0.100/ 0.50	0.100/ 0.50	0.100/ 0.50
Package Thickness (inches)	0.105	0.110	0.125	0.105	0.110	0.110	0.110	0.110	0.110	0.110	0.110*
Weight (gm)	8.69	8.69	8.69	10.43	10.43	16.07	23.3				84
Max. Footprint (Inches)	1.180	1.180	1.180	1.380	1.380	1.480	1.780	1.780	1.980	2.170	2.670
UV Erasable			x								
Shipping Media: Trays	x	x	x	x	x	x	x	x	x	x	x
Comments / Footnotes	* With EPROM										

Table 1-4. CERDIP

Lead Count	20	28	40
Sq/Rect.	R	R	R
Pitch (Inches)	0.100	0.100	0.100
Package Thickness (inches)	0.153	0.167	0.167
Weight (gm)	2.87	8.68	12.03
Max. Footprint (Inches)	0.995	1.485	2.085
UV Erasable	x	x	x
Shipping Media: Tubes	x	x	x
Comments / Footnotes	Inquire as to the availability with UV Window.		

1.4.2 Plastic Package Attributes

Table 1-5. Plastic Dual In-Line (PDIP)

Lead Count	24	28	32	40	64
Sq/Rect.	R	R	R	R	R
Pitch (Inches)	0.100	0.100	0.100	0.100	0.100
Package Thickness (inches)	0.152	0.152	0.150	0.160	0.167
Weight (gm)	1.67	1.94	4.815	6.128	12.05
Max. Footprint (Inches)	1.260	1.470	1.655	2.070	2.290
Shipping Media: Tubes	x	x	x	x	x
Comments / Footnotes	Some pin counts available in: Half lead, Wide body, Wide Body, and Standard Type P				

Table 1-6. Plastic (Flatpack)

Lead Count	68
Sq/Rect.	S
Pitch (Inches)	0.050
Package Thickness (inches)	0.168
Weight (gm)	5.6
Max. Footprint (Inches)	1.780
UV Erasable	
Shipping Media: Trays	x
Comments / Footnotes	Through Hole Use Only

Table 1-7. Plastic Quad Flatpack (PQFP)

Lead Count	84	100	132	164	*196
Sq/Rect.	S	S	S	S	S
Pitch (Inches)	0.025	0.025	0.025	0.025	0.025
Package Thickness (inches)	0.170	0.170	0.170	0.170	0.170
Weight (gm)	2.07	2.8	4.2	6.1	8.55
Max. Footprint (Inches)	0.790	0.890	1.090	1.290	1.490
UV Erasable					
Shipping Media: Tubes Tape & Reel Trays	 x x x	 x x x	 x x x	 x x x	 x x x
Desiccant Pack	x	x	x	x	x
Comments / Footnotes	All PQFPs are “Gull Wing” with bumpers *MM-PQFP				

Table 1-8. Quad Flatpack

Lead Count	44	48	64	80	80	100	100	128	144	160	176	208
Sq/Rect.	S	S	S	S	R	S	R	S	S	S	S	S
Pitch (mm)	0.80	0.80	0.65	0.50	0.80	0.50	0.80	0.80	0.50	0.65	0.50	0.50
Package Thickness (mm)	2.35	2.55	2.55	1.66	3.15	1.66	3.15	3.65	1.5	3.65	1.5	3.56
Weight (gm)	0.42		0.71	0.50	1.65	0.64	1.65					5.18 10.85*
Max. Footprint (Inches)	0.50	0.61	0.61	0.56	0.72	0.64	0.72	1.27	.881	1.22	1.03	1.220
Shipping Media: Trays	x	x	x	x	x	x	x	x	x	x	x	x
Desiccant Pack	x	x	x	x	x	x	x	x	x	x	x	x
Comments / Footnotes	Gull Wing lead Configuration, non-bumped * With heat slug											

Table 1-9. Plastic Leaded Chip Carrier (PLCC)

Lead Count	28	28	32	44	52	68	84
Sq/Rect.	S	R	R	S	S	S	S
Pitch (mm)	0.050	0.050	0.050	0.050	0.050	0.050	0.050
Package Thickness (mm)	0.152	0.108	0.108	0.148	0.150	0.150	0.150
Weight (gm)	1.15	0.85	1.1	2.31	3.17	4.8	6.2
Max. Footprint (Inches)	0.495	See Note	See Note	0.695	0.795	0.995	1.195
Shipping Media Tubes Tape & Reel Trays	x x x	x x x	x x x	x x x	x x	x x x	x x x
Desiccant Pack	x	x	x	x	x	x	x
Comments / Footnotes	All PLCCs are “J” Lead 28R--0.39 x 0.59 32R--0.48 x 0.59						

Table 1-10. Small Outline Package J-Lead (SOJ)

Lead Count	20	24
Sq/Rect.	R	R
Pitch (mm)	1.27	1.27
Package Thickness (mm)	0.105	0.113
Weight (gm)	0.50	0.62
Max. Footprint (Inches)	0.680	0.637
Shipping Media: Tape & Reel Tray	 x x	 x x

Table 1-10. Small Outline Package J-Lead (SOJ)

Desiccant Pack	x	x
Comments / Footnotes	"J" Configuration	

Table 1-11. Plastic Small Outline Package (PSOP)

Lead Count	44
Sq/Rect.	R
Pitch (mm)	1.27
Package Thickness (mm)	2.95
Weight (gm)	1.89
Max. Footprint (Inches)	0.640
Shipping Media Tubes Tape & Reel Trays	 x x x
Desiccant Pack	x
Comments / Footnotes	Gull Wing Lead Configuration

Table 1-12. Thin Small Outline Package (TSOP)

Lead Count	32	40	48	56
Sq/Rect.	R	R	R	R
Pitch (mm)	0.50	0.50	0.50	0.50
Package Thickness (mm)	0.0392	0.039	0.039	0.039
Weight (gm)	0.37	0.46	0.56	0.63
Max. Footprint (Inches)	0.795	0.795	0.795	0.795
Shipping Media: Tape & Reel Trays	 x x	 x x	 x x	 x x
Desiccant Pack	x	x	x	x
Comments / Footnotes	TSOP is "Gull Wing" Configuration			

Table 1-13. Shrink Small Outline Package (SSOP)

Lead Count	56
Sq/Rect.	R
Pitch (mm)	0.80
Package Thickness (mm)	0.050
Weight (gm)	1.15
Max. Footprint (Inches)	0.642
Shipping Media: Tape & Reel Trays	 x x
Desiccant Pack	x
Comments / Footnotes	Gull Wing Lead Configuration

Package attributes for Plastic Ball Grid Array can be found in Chapter 14. Package attributes for Micro Ball Grid Array can be found in Chapter 15.

1.4.3 Module Attributes

Table 1-14. Single In-Line Leaded Memory Module (SIP)

Lead Count	30
Sq/Rect.	R
Pitch (mm)	2.54
Package Thickness (mm)	2.00
Weight (gm)	
Max. Footprint (Inches)	3.105
Shipping Media: Tape & Reel	x
Comments / Footnotes	Insertable Module

Table 1-15. Single In-Line Leadless Memory Module (SIMM)

Lead Count	30	80
Sq/Rect.	R	R
Pitch (Inches)	0.100	0.050
Package Thickness (inches)	0.20	0.33
Weight (gm)		15.7
Max. Footprint (Inches)	3.505	4.655
Shipping Media Tubes Tape & Reel	x	x
Comments / Footnotes	JEDEC Standard Insertable Module	

1.5 Package/Module/PC Card Selection Guide

Table 1-16. Package / Module / PC Card Selection Guide (Sheet 1 of 2)

Package Type Description	Available Lead Counts	Marketing Designator	Special Notes
Ceramic Dual-In-Line (C-DIP). 0.100” Pitch, Socket or Insertion Mount 24, 28, 40, 48 C-DIPs Available with EPROM or Solid Lid 32 C-DIP Available with EPROM (lid) Only	16 18 22 24 28 32 40 48	C C C C C C C C	
Ceramic Leadless Chip Carrier (LCC), 0.050” Pitch, Socket or Surface Mount 32, 44, and 68 LCCs Available with EPROM or Solid Lid	18 20 28 32 44 68	R R R R R R	
Ceramic Pin Grid Array (CPGA), 0.100” Pitch for 68L - 208L, 0.100/0.50” for 264L- 387L Socket or Insertion Mount 68L and 88L “Cavity Up” Available with EPROM or Solid Lid	68 88 88 132 168 208 240-280 272-320 387	A A A A A A A A	 Cavity Down Cavity Down Cavity Down Cavity Down Cavity Down Cavity Down Cavity Down
Ceramic Quad Flatpack (CQFP), 68L Available in 0.050” Pitch. 164L and 196L Available in 0.025” Pitch, Socket or Surface Mount	68 164 196	Q K K	Flat Leads Flat Leads Flat Leads
Ceramic Dual-In-Line Package (CERDIP), 0.100” Pitch Socket or Insertion Mount	16 18 20 22 24 24 28 28 32 40 42	D D D D DP D DP D D D D	 .300” .300”
Plastic Dual-In-Line Package (PDIP); 0.100” Pitch 64L “Shrink DIP” has a 0.070” Pitch Socket and Insertion Mount	16 18 20 24 24 28 28 32 40 48 64	P P P P PD P PD P P P U	 .300” .300” Shrink

Table 1-16. Package / Module / PC Card Selection Guide (Sheet 2 of 2)

Plastic Flatpack (PFP), 0.050” Pitch Shipped in Carrier with flat Lead, Through-Hole Mount	68	FP	
Plastic Leaded Chip Carrier (PLCC), 0.050: Pitch Surface or Surface Mount 28L is Available in a Square and Rectangular Package Body 32L is Available in a Rectangular Package Body Only	20 28 32 44 52 68 84	N N N N N N N	Sq. Sq./Rect. Rect. Sq. Sq. Sq. Sq.
Plastic Quad Flatpack (PQFP), 0.025” Pitch, Surface Mount Some Packages Available in a Variety of Options: Die UP, Die Down, and Die Down with Heat spreader	84 100 132 164 196	KD KD, KU, NG KD, KU, NG KU KU	
Quad Flatpack (QFP), Variable Lead Pitch Surface Mount Quad Flatpack (QFP), Surface Mount, Copper Lead Frame	44 48 64 80 100 128 144 160 176 208 208	S S S SB, S SB,S S SB S SB SB SB	 Sq./Rect. Sq./Rect.
Plastic Ball Grid Array (PBGA)	208 272 324 352	FW FW FW GC	Sq.
Plastic Pin Grid Array (PPGA)	296	FV	Sq.
Micro Ball Grid Array* (uBGA)	40, 48	G G	Rect.
Small Outline J-Lead (SOJ), 1.27 mm Pitch Surface Mount	20 24	PE PE	
Plastic Small Outline Package (PSOP), 1.27 mm Pitch, Surface Mount	44	PA	
Shrink Small Outline Package (SSOP), 0.80 mm Pitch, Surface Mount	56	DA	
Thin Small Outline Package (TSOP) Pitch, Surface Mount Available in Die Up or Die Down (32, 40 only)	32, 40 48 56	E, R E E, DD	
Single In-Line Leaded Memory Module (SIP), 2.54 mm Pitch, Socket or Insertion Mount	30	GB	
Single In-Line Leadless Memory Module (SIMM) 0.100” Pitch, Connector Mount	30 80	SM SM	
Single Edge Contact Cartridge (S.E.C.C)	242 330		Cartridge mounts in a slot connector

1.6 Revision Summary

- Added S.E.C.C. (330 Contact) figure & information.
- Revised the introduction
- General review of the chapter