Simple, Fast High Reliability Rework of Leadless Devices

Bob Wettermann

Recently, the impact of leadless device reliability after rework was investigated as part of a NASA/DoD project for different leadless device rework processes. Leadless device packages, which are challenging to rework due to their large thermal ground planes, low standoff heights from the PCB and the lack of visually inspected criteria, were investigated in terms of their long term reliability after rework. Several leadless device rework methods, including the latest rework procedure (stay in place stencil)[1] were investigated in this study. The study, commissioned by Naval Surface Warfare Center (NSWC), Crane Division was attempting to answer the question : "*to what extent do rework procedures, including SnPb and lead-free mixed solder joints affect solder joint reliability of high-performance electronics .*"

Review of the Leadless Device Rework Procedures

There are numerous methods being used to rework leadless devices; either guided by the older IPC 7711 5.4.1 process guidelines or the newest stenciling techniques. The older of these methods includes solder paste printing the site location on the PCB followed by the placement and reflow of the device. The newer method includes the device pad "bumping" followed by placement of the device with a rework system using paste flux.

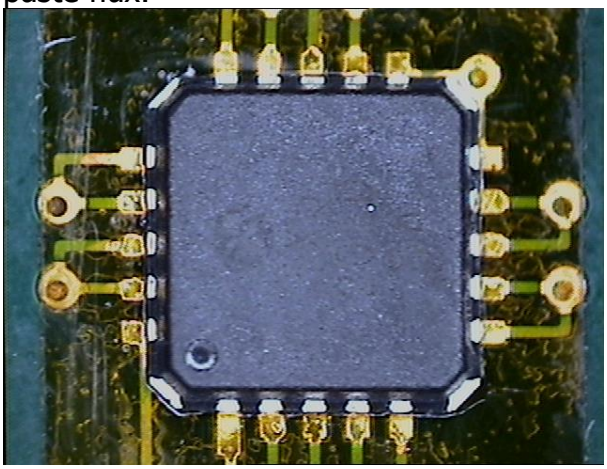

Figure 1- Reworked QFN using stay in place stencil

Several years ago a simpler, faster method for reworking leadless devices was developed using polyimide stencils. In this method a polyimide stencil is placed over the land patterns on the bottom of the device. Solder paste is then rolled in to the apertures. After reflow, the stencil is peeled off leaving "bumps" on the bottom of the device. (Figure 2) A stencil permanently affixed to the PCB filled with paste flux or solder paste then acts as the receptacle for these device "bumps" to fit in to. However, heretofore the longevity of such an interconnection was questioned. This study, a portion of which is described in this writing verifies the high reliability of these solder joints using this newer technique.

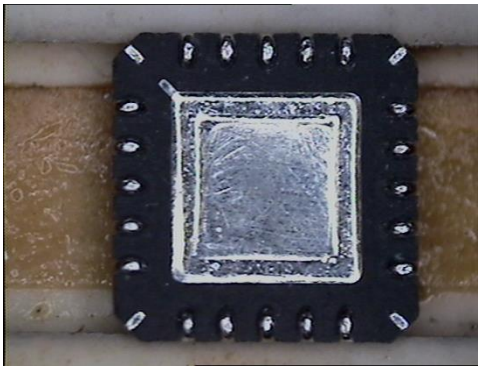
Figure 2-Bumped QFN Ready to be Placed onto PCB

Method

The goal of the NASA/DoD project was to generate data supporting the qualification of SnPb rework procedures for military hardware built with Pb-free processes through analysis of thermal cycling, vibration, and drop test data including micro section analysis.

Thirty (30) of the one hundred and ninety three (193) test vehicles were built for Naval Surface Warfare Center (NSWC), Crane Division, member, in support of the larger Naval Supply Command (NAVSUP) sponsored "Logistics Impact of Pb-free Circuits/Components" project. These PWBs were assembled using both SAC305 Pb-free solder alloys using boards with Pb-free component finishes. The boards had an FR4 laminate per IPC-4101/26 with a minimum glass transition (Tg) of 170ºC for the test vehicles. The raw boards complied with IPC-6012 (Qualification and Performance Specification for Rigid Printed Boards), Class 3, Type 3 specifications. The boards had an immersion silver finish. Circuit boards were processed per IPC-4553; Specification for Immersion Silver Plating for Printed Boards. The test vehicle was 14.5 X 9 X 0.09 inches with six 0.5-ounce copper layers Figure BB) .

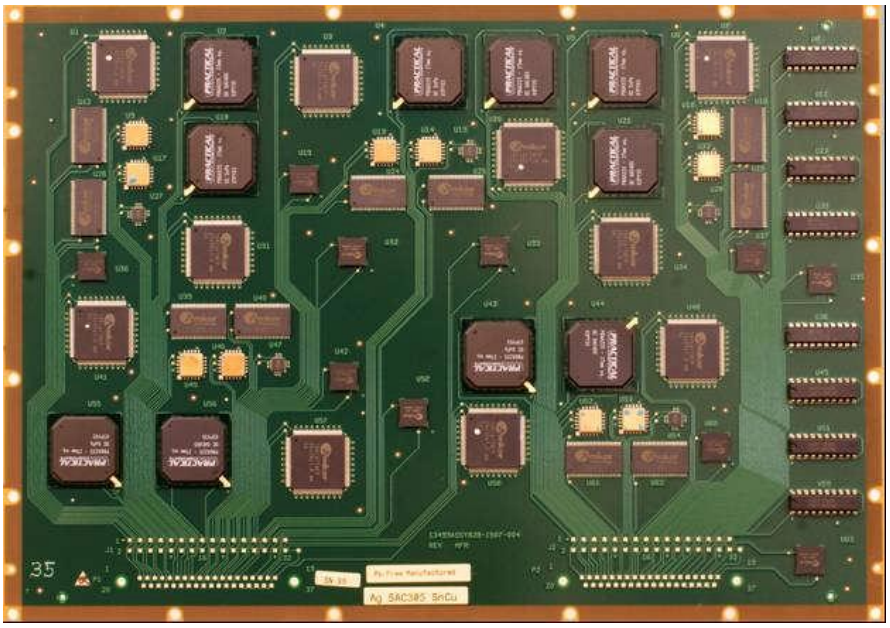
Figure 3 Test vehicle for QFN rework reliability study

Following assembly, rework was performed on random Pb-free DIP, TQFP-144, TSOP-50, MLF, LCC and the QFN components of interest using tin-lead solder. The components were reworked either once or twice. Specifically the QFN devices were reworked using two methods. In the first method the boards were paste printed PCB device locations paste printed on to the boards using rework systems. Devices were removed using IPC 7711 3.11. In the second method the IPC 7711 method 5.8.1.2. was used to "bump" the parts. Once bumped, the parts were inserted in to the stencil on the board (Figure 3). The matrix of the experiment is given in Table 1 below.

Table 1: Number of QFN's reworked once or twice for vibration, drop, and thermal cycle testing using a "traditional" hot gas rework method (IPC 7711 5.4.1) or the StencilMate™ (IPC 7711 5.8.1.2) method.

	Vibration			Drop			Thermal Cycle - SAC305			Thermal Cycle – SN100C		
	Traditional		StencilMate™	Traditional		StencilMate™	Traditional		StencilMate™	Traditional		StencilMate™
Site	1X	2X	1X	1X	2X	1X	1X	2X	1X	1X	2X	1X
U15	5	4	--	4	5	--	1	2	1	1	2	1
U27	4	5	--	5	4	--	1	1	2	1	1	2
U28	5	4	--	4	4	1	2	1	1	2	1	1
U47	5	--	4	5	--	4	1	2	1	1	2	1
U54	4	--	5	4	--	5	1	1	2	1	1	2

The particular focus of this paper are related to the QFN package (A-MLF20-5mm-.65mm-DC) as seen below:

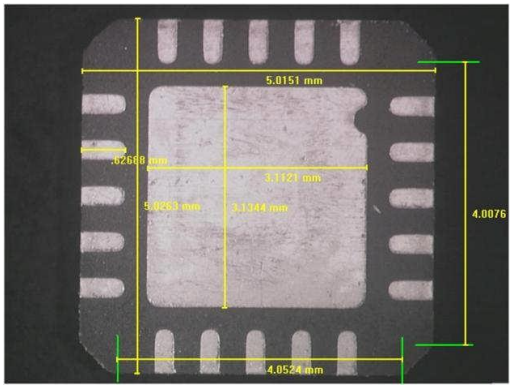

Figure 4 –QFN Packakge used in the reliability study

The test plan was chosen to represent the performance requirements in applicable military and industry standards. A key factor was selecting test parameters that would subject enough environmental stress to cause solder joints to fail, thus permitting differentiation between lead vs. lead-free performance. Military document MIL-STD-810F and industry documents IPC-SM-785 and IPC-TM-650 were primary references used for writing the test plan.

There were numerous tests as part of the overall test protocol. The **vibration** test was instituted per MIL-STD-810F, Method 514.5 (Vibration), in order to determine the reliability of the various solder alloys under severe vibration. The **thermal cycle testing** used was performed in accordance with IPC-SM-785 *(Guidelines for Accelerated Reliability Testing of Surface Mount Solder Attachments)* in order to determine the longevity of the solder joints under thermal stress conditions. It was conducted at two different conditions, -55 to +125°C and -20 to +80°C.The thermal cycle tests were run until greater than 63 percent of component failures are achieved in order to provide statistically meaningful data. The **mechanical shock test** was used to determine the resistance of the solder to the stresses associated with high-intensity shocks induced by rough handling, transportation, or field operation. The **Combined Environments Test** (CET) was used to predict the reliability of solders under combined thermal cycle and vibration. Finally drop testing was used to determine the resistance of board level interconnects to board strain induced by dynamic bending as a result of **drop testing**. These failure modes replicate the stresses seen during manufacturing, electrical testing (especially in-circuit test), card handling and field installation due to process issues and/or the quality of incoming components and/or boards.

Results

The polyimide stencil reworked solder joints were significantly thicker than the traditionally reworked solder joints (Figure 5 and 6).

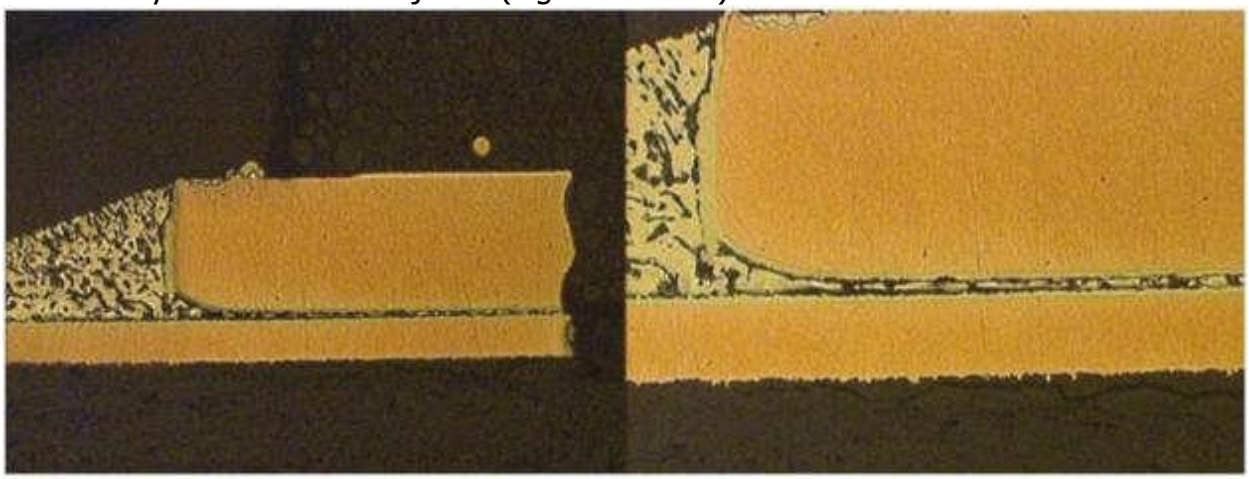

Figure 5 - QFN-20 Solder Joints, Board 107, Component U28, SN100C/Sn, Reworked with SnPb Paste, 1 Rework Failed @ 277 Cycles (approx. solder fillet thickness 1.5 mils)

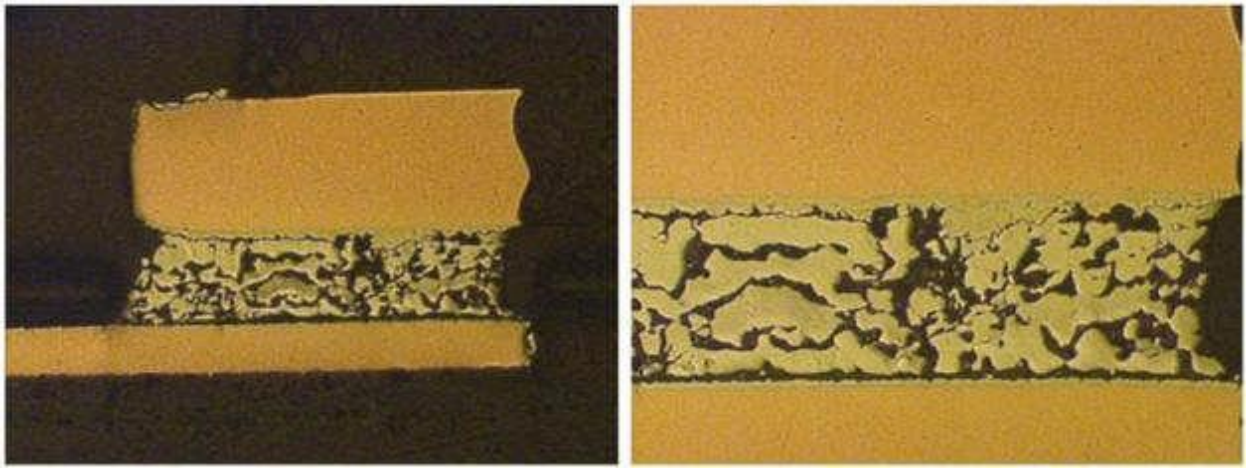

Figure 6 - QFN-20 Solder Joints, Board 109, Component U28, SN100C/Sn, Reworked with StencilMate™, 1 Rework, DNF (approx. solder fillet thickness 6.0 mils)

Thermal Cycle Testing

The thermal cycling testing was conducted between -55°C and 125°C with the specifics of the testing found at http://teerm.nasa/gov for the NASA-DOD Lead-Free Electronics. The temperature was cycled between -55°C and 125°C at a maximum rate of 10°C/min and a dwell time of 30 minutes at 125°C and 10 minutes at -55°C. A total of 4,068 cycles were completed. Electrical continuity was continuously tested and failure was recorded corresponding to the total number of cycles.

Table 2 below indicates the population of thermal cycle tested PCBs.

Table 2: Percent failure of QFN's during 4068 thermal cycles from -55°C to 125°C.

	SAC305			SN100C		
	Total Tested	Total Failures	% Failure	Total Tested	Total Failures	% Failure
As-Manufactured	25	2	8%	25	3	12%
1X Traditional	7	0	0%	6	2	33%
2X Traditional	6	0	0%	7	0	0%
1X StencilMate™	7	1	14%	7	1	14%

Vibration Testing

Vibration testing was conducted per the study's test protocol (available at the http://teerm.nasa.gov). Test vehicles were evaluated at 8 intensity levels from 8-28 G. Each intensity level was evaluated consecutively, starting with 8G and increasing in intensity every 60 minutes. The vibration profile for each level as programmed for the shaker table is outlined below (Table 3):

Table 3: Composite vibration intensity and profile as a function of test time. For all levels, the power spectral density (PSD) increased at the rate of 6db/octave between 20 and 50Hz and decreased at the rate of 6dB/octave between 1000 and 2000Hz.

Test Time [min]	Power Spectral Density, PSD, [G^2/Hz]			Composite [G_{rms}]
	20Hz	50-1000Hz	2000Hz	
0-60	0.00698	0.0438	0.0109	8
61-120	0.0107	0.067	0.0167	10
121-180	0.0157	0.0984	0.0245	12
181-240	0.0214	0.134	0.0334	14
241-300	0.0279	0.175	0.0436	16
301-360	0.03354	0.2215	0.0552	18
361-420	0.0437	0.2734	0.0682	20
421-480	0.0855	0.536	0.133	28

Results from the comparison of percent failure and time to failure for reworked QFNs are shown in Table 4 below. Percent failure was calculated by dividing the number of components in a group that failed during testing by the total number of components in that group. Average time to failure was calculated considering components that did and did not fail during testing.

Table 4: Percent failure and average time to failure for reworked QFN's during vibration testing. Differences in time to failure are considered significant if the percent failure differs by at least 40%

	Percent Failure, [%]			Average Time to Failure, [min]		
	Traditional		StencilMate™	Traditional		StencilMate™
Site	1X	2X	1X	1X	2X	1X
U15	100	100	--	117	90	--
U27	25	0	--	478	DNF	--
U28	**60**	**100**	--	446	421	--
U47	100	--	75	389	--	419
U54	**100**	--	**0**	366	--	DNF

Drop shock as well as other reliability testing results can be found on the http://teerm.nasa.gov web site.

Conclusion

Based on the extensive reliability testing undertaken in this study, it was determined that independent of the QFN rework method the polyimide stay-in-place stencil technique performed at the same level as the traditional board paste printing technique. In the case of the thermal shock, vibration (as well as shock, combined environmental and drop testing) there was no difference between rework methods. These results have shown that this simple to implement technique has been shown to not impact the reliability of a reworked device. In fact the microsections indicate that the stay in place polymide stencil technique, if time allowed, would outlast their traditional method hot air rework methods.

References

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2. "NASA-DOD PB-Free Electronics Rework Project: Effect of 1x and 2x Eutectectic Solder Rework on Vibration Reliability", J.P Tucker, C. A. Handwerker, A.E. Pedigo et el pp398+ SMTA International Proceedings 2011.
3. *"NASA-DoD Lead-Free Electronics Project",* March 2010 National Aeronautics and Space Administration
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