

Microspring Characterization and Flip-Chip Assembly Reliability

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Abstract—Electronics packaging based on stress-engineered spring interconnects has the potential to enable integrated IC testing, fine pitch, and compliance not readily available with other technologies. We describe new spring contacts which simultaneously achieve low resistance ($< 100\text{ m}\Omega$) and high compliance ($> 30\text{ }\mu\text{m}$) in dense 2-D arrays ($180 \sim 180\text{-}\mu\text{m}$ pitch). Mechanical characterization shows that individual springs operate at approximately $150\text{-}\mu\text{N}$ force. Electrical measurements and simulations imply that the interface contact resistance contribution to a single contact resistance is $< 40\text{ m}\Omega$. A daisy-chain test die consisting of 2844 contacts is assembled into flip-chip packages with 100% yield. Thermocycle and humidity testing suggest that packages with or without underfill can have stable resistance values and no glitches through over 1000 thermocycles or 6000 h of humidity. This paper suggests that integrated testing and packaging can be performed with the springs, enabling new capabilities for markets such as multichip modules.

Index Terms—Flip chip packaging, MEMS, package reliability, springs, testing.

I. INTRODUCTION

SOLDER bonding is the dominant method of interconnecting for electronics, but suffers from inherent problems such as brittleness and high-temperature assembly. Current commercial flip-chip interconnects, such as solder balls, gold bumps, and conductive adhesives, all have very limited compliance, making it difficult to compensate for the large thermal expansion mismatches typically existing in packages. Other challenges for flip-chip include scaling to fine pitch and small gaps—important for enabling ever smaller system-in-packages

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(SIPs). Currently, complex multichip packages are rare because of testing and the challenges of obtaining known good dies.

We are developing compliant thin film interconnects that have the potential to dramatically improve IC flip-chip packaging. They can absorb large thermal expansion mismatches between silicon chips and substrates, simplifying packaging design, as current solder-based approaches are not flexible. The high stresses of lead-free solder on organic boards can be avoided, facilitating integration of fragile low- k dielectrics. If the compliant interconnect enables bare die testing, then integrating at-speed testing of chips before bonding to a final substrate is possible, alleviating the need for an expensive known good die. Such capability can reduce the cost of multichip module (MCM) and SIP solutions by enabling both testing and packaging functions.

Other approaches for building a compliant interconnect include compliant layers under the solder [1], metalization over organic elastomers [2], [3], plated wirebonds [4], bent printed circuit board (PCB) metal [5], and machined bulk metal for land grid array (LGA). The use of compliant layers under the solder is established for memory packaging, but does not improve integrated testing for MCM (no rework) and is not low-profile. The wire-bond approach, because of its serial manufacturing process, is inherently more expensive than a batch process. The metalized elastomer requires more complicated fabrication than the stress-engineered approach presented here. The bent PCB metal has been recently commercialized and the LGA well established for sockets, but both are of millimeter scale and not readily scalable because of the use of thick films.

In contrast, the stress-engineered spring approach presented here has a wide mechanical and electrical design range and has been demonstrated down to high-density interconnect regimes. For flip-chip packaging, multiple packages have been demonstrated. Silicon dies with large springs ($> 500\text{ }\mu\text{m}$ pitch) have been assembled directly on organic substrates [6]. Because they are photolithographically defined, stress-engineered springs can offer tighter pitches than other compliant packaging approaches such as polymer bumps [2] or plated wirebonds [4]. Dense linear arrays of stress-engineered springs at both $20\text{-}\mu\text{m}$ [7] and $6\text{-}\mu\text{m}$ pitch [8] have been assembled into flip-chip packages. Previous stress-engineered springs have been designed for probe cards for probing aluminum pads [9] and can achieve many grams of force (tens of mN). The stress-engineered spring process inherently includes redistribution,

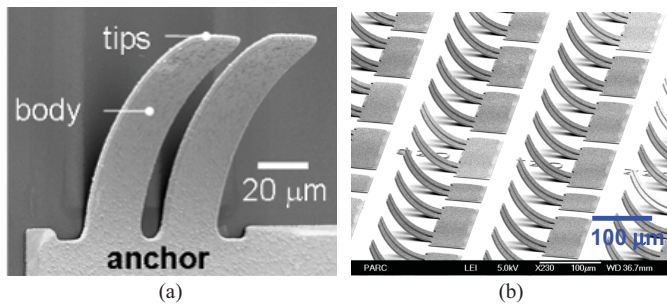


Fig. 1. SEM image of a (a) contact and (b) 2-D array contacts.

as the spring metal layers are also traces, which reduces the overall system cost. The fabrication process is a thin-film metallization process that is compatible with complimentary metal–oxide–semiconductor (CMOS) or backend wafer-scale packaging. The manufacturing cost of the process has been modeled and found to be similar to that of solder.

This paper describes a new stress-engineered contact design for dense 2-D array applications such as processors. An important future application of such contact design is in the construction of 2.5-D assemblies of chips where large vertical clearance and rematability are important for constructing tightly coupled multichip computing systems [10]. The springs achieve low resistance ($< 100 \text{ m}\Omega$), high compliance ($> 30 \text{ }\mu\text{m}$), and high yield for 2-D arrays (thousands of contacts, $180 \times 180 \text{ }\mu\text{m}$ pitch). In Section II, the spring fabrication and yield are described. Section III summarizes the mechanical and electrical characterization of a single spring. Simulations are used to estimate the interface contact resistance ($< 40 \text{ m}\Omega$). In Sections IV and V, various package assemblies and their reliability testing are described. Air-gap packages using spacer layers or self-aligning ball-and-pit [11], [12] mechanisms are described, as well as packages with springs embedded in adhesive.

II. SPRING FABRICATION

The microsprings are fabricated with stress-engineered thin-film processing. The key step is the deposition of a $1\text{-}\mu\text{m}$ thick alloy of molybdenum–chromium with a large stress gradient (GPa per μm). After being lithographically patterned into cantilever beams ($100\text{-}\mu\text{m}$ long, $30\text{-}\mu\text{m}$ wide) and subsequently released, the spring stress relaxes, lifting the tips out of the plane, forming a 3-D-compliant spring interconnect. Extra metal such as gold can be electrodeposited after the release to provide conductivity and strength. Fig. 1 shows a close-up of a contact, consisting of two springs in parallel and 2-D array contacts. The fabrication process uses 4-in wafer-scale processing and requires only two masks. Routing and redistribution can be performed without extra masks by using traces that are not released. The process is a low-temperature one and has been integrated at the wafer scale onto post-CMOS devices [13]. See [14] for other fabrication details.

The spring process is uniform and of high yield. A key parameter is the lift-height, defined as the vertical distance of the tip above the substrate. Each test chip is $14 \times 16 \text{ mm}$ and has 2844 contacts (Fig. 2). A commercially available

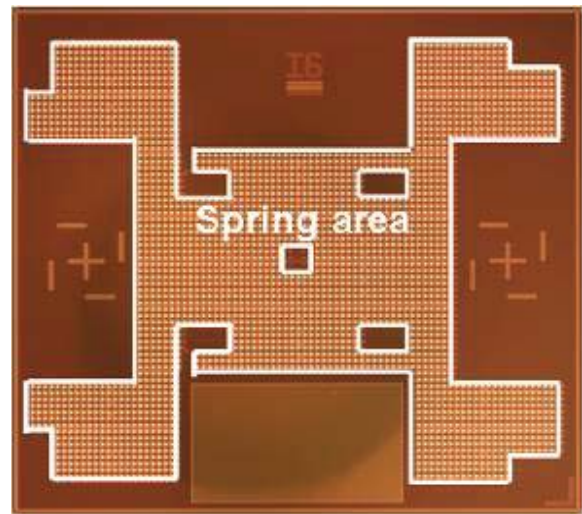


Fig. 2. Spring chip die with 2844 contacts and an area of $14 \times 16 \text{ mm}$.

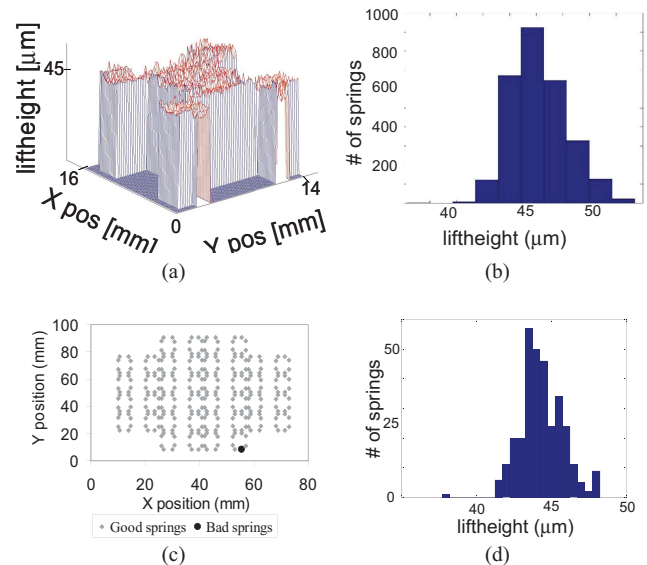


Fig. 3. Spring lift-height uniformity measurements. (a) and (b) Across a chip of 2844 contacts. (c) and (d) Across a wafer.

tool (Nikon VMR-3020) is used to automatically measure the lift-heights using pattern recognition. The repeatability of the measurement technique is $\pm 3 \text{ }\mu\text{m}$. Measurements of each spring in the chip give an average height of $\sim 45 \text{ }\mu\text{m}$, with a variation equal to or less than the measurement error [Fig. 3(a) and (b)]. Measurements across a 4-in wafer give similar results [Fig. 3(c) and (d)]. Out of 319 measured springs spaced evenly across the wafer, only one spring on the wafer edge (black dot) is outside of $42\text{--}48 \text{ }\mu\text{m}$ range (the measurement error is $\pm 3 \text{ }\mu\text{m}$). Release yields above 99.9% have been demonstrated (based on $\sim 10^5$ springs per wafer), and 100% yield has been achieved for more than half of the 20 dies per wafer in our research prototype facility.

III. SINGLE SPRING CHARACTERISTICS

Chips consisting of single spring test structures are used to measure the mechanical and electrical properties of a single

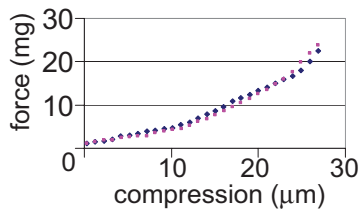


Fig. 4. Measured force of a single spring. Two measurements are shown.

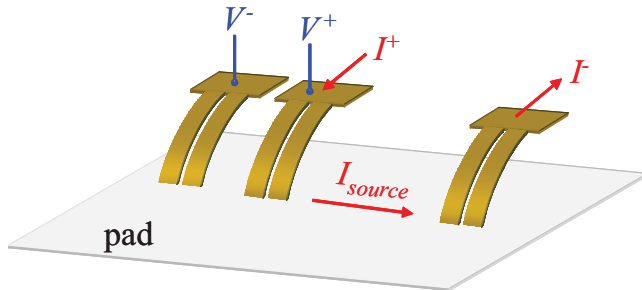


Fig. 5. Four-wire resistance measurement of a contact (middle contact). I_{source} is forced from I^+ to I^- , electrical potential drop $V_{sense}(V^+ - V^-)$ is monitored during compression. Electrical resistance of the middle contact is V_{sense}/I_{source} .

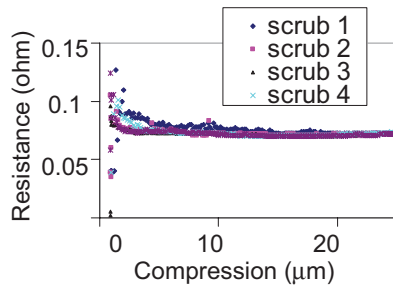


Fig. 6. Four-wire resistance monitored while the spring is compressed. The plateau value is ~ 72 m Ω .

spring. The measured force versus compression of a spring is directly measured by a force scale (see [15] for setup description). Fig. 4 shows that the force curve is repeatable as the spring is repeatedly compressed to just under $30 \mu\text{m}$. After full compression, a negligible change in the lift-height is observed. This suggests that the spring is operating below the yield point threshold for plastic deformation. A typical compression in a package is $25 \mu\text{m}$, corresponding to a compressive force of 0.015 g ($150 \mu\text{N}$). While this force is significantly less than in macroscopic pressure contacts, the pressure is similar (~ 15 MPa, see [16] and therefore, we believe, is adequate for gold-to-gold pressure contacts. Note that microscale gold pressure contacts have already been commercialized as RF microelectromechanical systems switches, showing that there are no fundamental barriers to high reliability [17].

A resistance test structure is measured and modeled to study the resistance constituents. A single contact (two-spring) device in a four-wire configuration is measured as a function of compression (Fig. 5). Fig. 6 shows a typical measurement versus spring compression against a large gold pad. The resistance reaches a plateau of ~ 70 m Ω when compressed

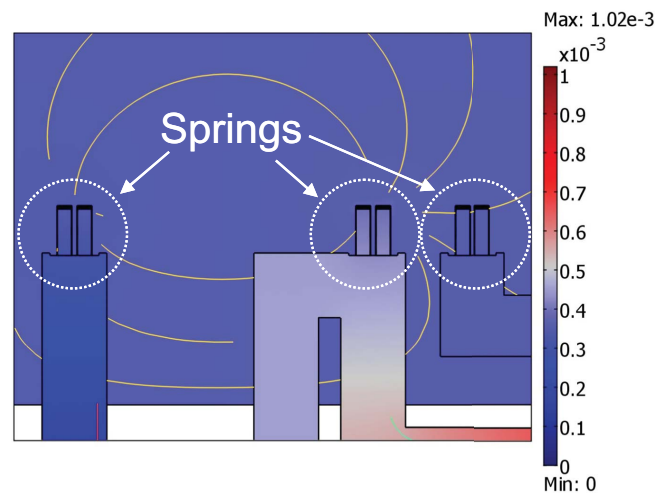
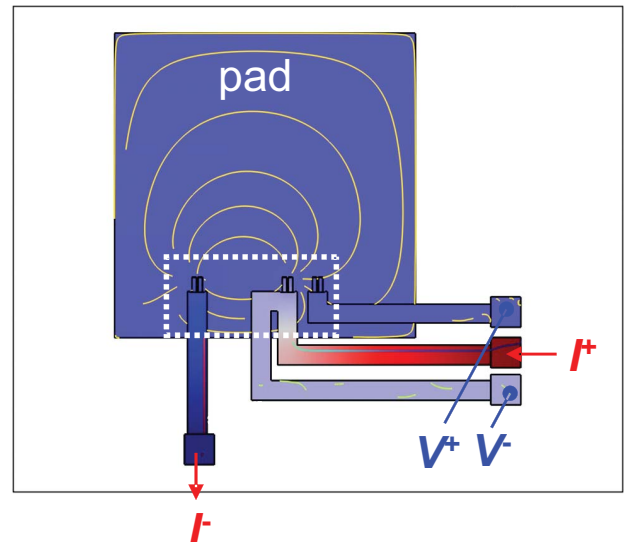


Fig. 7. Electrical potential with current density arrows of single-contact four-wire resistance test structure. Constant current I_{source} is forced from I^+ to I^- and potential drop $V_{sense}(V^+ - V^-)$ is calculated.

by $10\text{--}20 \mu\text{m}$. Finite element modeling (FEM) was used to study the resistance components of the test structure. Using the commercial software COMSOL, a geometric model was constructed. The electrical potential distribution of the entire structure was calculated by setting I_{source} (1 mA) and calculating V_{sense} (Fig. 7). The simulated total resistance value equals V_{source}/I_{source} . Several potential drops contribute to V_{sense} , including the lead traces, spring body, tip-pad interface, and pad spreading (Fig. 8). All of them are defined as effective resistance components that contribute to total measured resistance (V_{source}/I_{source}). FEM was used to determine all of these components based on measured sheet resistance and geometric values, except for the tip-pad resistance. The tip-pad interface resistance physically consists of asperities and constriction resistance. While models for this resistance exist [18], they require assumptions concerning multiple variables, such as the effective contact area, asperity dimensions, and local conductivity. We, instead, modeled the tip-pad interface resistance as a simple resistor and swept the value of this resistor to fit the total measured resistance.

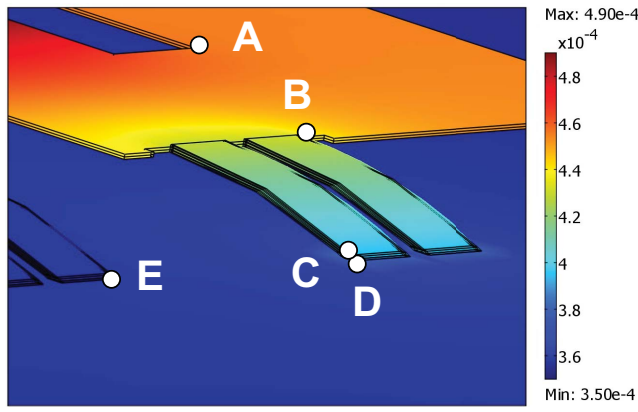


Fig. 8. Electrical potential distribution of the middle contact. Measured V_{sense} equals V_{A-E} , and is composed of effective lead trace V_{A-B} , spring body V_{B-C} , tip-pad interface V_{C-D} , and pad spreading V_{D-E} .

TABLE I
RESISTANCE COMPONENTS OF ONE CONTACT

Resistance component	Value (m Ω)
Lead trace R_{A-B}	23
Spring body R_{B-C}	36
Tip-pad R_{C-D}	11–41
Pad spreading resistance R_{D-E}	~ 0
Total	70–100

Total measured resistances of 70–100 m Ω were observed, which were used for estimating the range of the resistance components based on the above FEM analysis. Table I shows that 16%–41% of the resistance is due to the tip-pad interface. This is an estimate of the low resistance limit for a gold-gold pressure contact with this contact area and force (11–41 m Ω). This is similar to other reported values [18]. The spring body contributes another third of the resistance. This value can be lowered by changing the spring dimensions. For example, if a smaller lift-height or compliance is required, then the spring can be shorter. The trace resistance contributes 23%–33%. This routing exists to enable the measurement, and would be much less for the typical case of a spring on via (with no routing). The spreading resistance was found to be almost negligible.

IV. PACKAGE ASSEMBLY

To study the reliability and packaging options, flip-chip packages were assembled by placing a chip with springs (see Fig. 9) onto the corresponding metal pads on another chip (pad chip) using a variety of approaches. Generally, two types of packages were built: springs in air, and springs embedded in adhesive (Fig. 10). Other important parameters include how the gap between the chips is controlled and the bonding method. The gap should ensure that the springs are compressed by more than 15 μm to operate in the resistance plateau region (Fig. 6). For springs with initial lift-heights of 45 μm , our target gap was 20 μm , corresponding to a 25- μm compression. The gap was defined by using a polyimide spacer wall on the pad chip, a precise ball-and-pit scheme [19], or precision assembly. The bonding methods

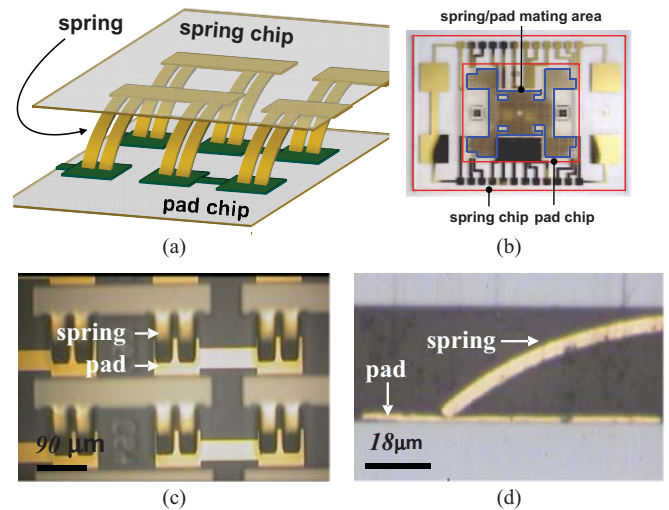


Fig. 9. (a) Schematic of a flip-chip package with aligned springs and pads. (b) Top view and (c) close-up of a glass-on-glass package with 2844 springs landing on 2844 pads in spring/pad mating area. (d) Cross section of a silicon-on-silicon flip-chip package. Note that the slight delamination of the pad in this picture is caused by the cross-sectioning procedure; such defects have never been observed in actual packages (as inspected visually for glass packages, and with infrared imaging for silicon packages).

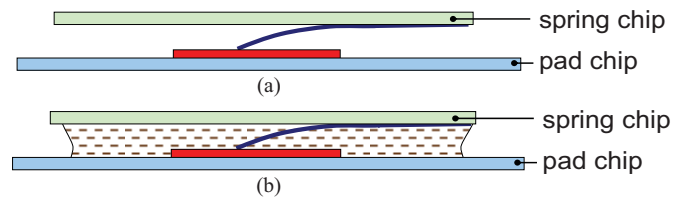


Fig. 10. Schematic of two package types. (a) Spring and contact are in air. (b) Springs embedded in adhesive.

used are adhesive on the edges/corners, at the corners only, all along the edges, or everywhere (Loctite 352 adhesive). Note that, for the last case, the adhesive can be applied onto the spring chip before assembly, or after assembly by wicking from the edges. An activator can be mixed with the adhesive for curing, or UV cure can be used for the adhesive on the edges. Note that the spring and pad substrates are either silicon or glass. Glass substrates aid inspection during development and have the same thermal expansion coefficient as silicon.

The relative merits of each assembly approach depend on the application requirements. Chips in air are easier to rework. In previous work, we have shown springs in air with no adhesive, as they are bonded through a clamping mechanism [19]. Such an approach can be appropriate for large high-end MCMs, where easy rework is particularly important. Springs in adhesive can have lower profiles (no clamp on top) and have extra protection from the environment. These cannot be readily reworked, but at-speed testing can be performed before bonding. Gap control based on a spacer layer is substrate-independent, while the ball-and-pit approach requires silicon substrates.

V. PACKAGE TESTING

Thermocycle testing consisted of cycling between 0 $^{\circ}\text{C}$ and 100 $^{\circ}\text{C}$ with 10 min dwells and 10 min rise and fall

TABLE II
SUMMARY OF PACKAGE RELIABILITY TESTS

Package	Springs	Adhesive	Gap Stop	Humidity (hours)	Thermocycle (cycles)	Resistance	Pre-scrubs
A	In Air	Edges and corners	Spacer layer		1017	+/-15%	NO
C	In Air	Edges and corners	NONE	6474		Mostly increasing, submerged	NO
D	In Air	Perimeter	Balls/pits	2347		Decreasing	YES
E	Embedded	Pre-mixed activator	Spacer layer		1082	Mostly decreasing	NO
G	Embedded	Underfill pre-mixed activator	Spacer layer		1112	Stable or decreasing	NO
H	Embedded	Pre-mixed activator	Spacer layer	7746		Stable or decreasing	NO

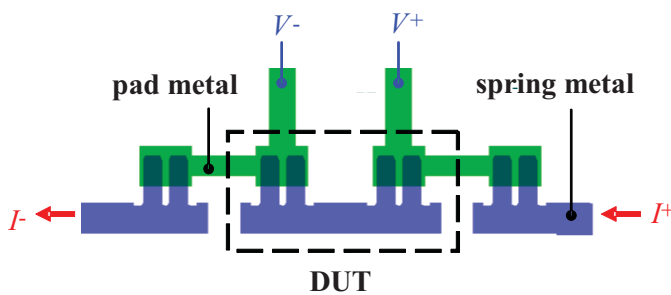


Fig. 11. I_{source} forced from I^+ to I^- and electrical potential drop $V_{\text{sense}}(V^+ - V^-)$ measured. Device under test (DUT) resistance equals $V_{\text{sense}}/I_{\text{source}}$.

times in an oven (Sigma Systems, model M18). The packages inside the thermocycle oven were wired to an event detector so that any momentary resistance increase in any one of the 2844 contacts of longer than 200 ns was detected as a glitch. For humidity testing, the packages were stored in an oven (Espec, SH-241) at 85 °C, 85% RH. Periodically, the packages were removed from the thermocycle and humidity chambers and four-wire resistance measurements of the daisy chains were taken (Fig. 11). The measured resistance is composed of the spring resistance (body, tip-pad interface, spreading) and significant amounts of spring trace and pad trace. These measurements used an automated pogopin setup which had a system repeatability of approximately $\pm 5\%$, corresponding to ± 10 – 20 m Ω for the two spring contact chains. Table II summarizes the reliability testing. None of the packages showed glitches during thermocycling. The majority of resistances were stable or decreased from initial values through over >1000 thermocycles and 2000–6500 h in humidity. No increases over 15% the nominal stable value for a chain were observed, unless noted by an obvious defect.

Within the air-gap packages, the resistance tends to decrease during testing if pre-scrubs are performed (see Package C). For pre-scrubbing, the die was compressed until the gap was less than 20 μm , fully retracted, and then repeated five times before bonding. We believe this helps to clean the tips and pads as well as increase the effective contact area. Note that pre-scrubbing is commonly used for probe cards. Separate mate

TABLE III
PACKAGE A THERMOCYCLING MEASUREMENTS

Number of Contacts in a Daisy Chain	Four-Wire Resistance, ohms			% Change
	Initial	680 Cycles	1017 Cycles	
2	0.155	0.148	0.166	6.7
2	0.169	0.157	0.190	12.2
2	0.214	0.176	0.182	-15.0
2	0.180	0.153	0.165	-8.0
2	0.168	0.162	0.186	10.6
2	0.165	0.153	0.174	5.5
2	0.143	0.124	0.121	-14.8
2	0.128	0.112	0.126	-1.9
2	0.106	0.103	0.120	13.5
2	0.117	0.118	0.115	-1.2
134	0.259	0.247	0.271	4.5
134	0.257	0.246	0.281	9.2
246	0.286	0.272	0.300	4.9
246	0.278	0.267	0.293	5.4
384	0.305	0.253	0.271	-11.1
384	0.253	0.239	0.256	1.1
530	0.270	0.249	0.257	-4.6
530	0.253	0.245	0.260	2.7

Total 2608

and remate tests show that scrubbing can reduce the resistances by 5%–20%. Air gap packages with the pre-scrubs more consistently show resistance decreases with time, possibly caused by an annealing of the interface contact or increase in the effective contact area during cycling. Slight reductions in resistance with time are typical for gold-to-gold contacts [20]. Thermocycle data for a package similar to Package C is reported in [19], and shows similar results.

For the springs embedded in adhesive, very stable or decreasing resistance values are observed for both thermocycle and humidity testing. The package that is underfilled after assembly (E) shows stable or decreasing resistance values. These packages do not have pre-scrubs. Performing pre-scrubs might reduce the initial resistance values and improve reliability.

TABLE IV
PACKAGE B HUMIDITY MEASUREMENTS

Contacts Per Chain	Four-Wire Resistance, ohms			% Change
	Initial	1015 Hours	6474 Hours	
2	0.405	0.420	0.448	10.8
2	0.418	0.419	0.459	9.9
2*	0.097	0.100	0.129	33.4
2	0.386	0.391	0.418	8.3
2	0.416	0.410	0.407	-2.2
2	0.407	0.407	0.406	-0.2
2**	0.310	0.345	0.401	29.4
2	0.357	0.366	0.407	14.2
2	0.307	0.312	0.317	3.3
2	0.360	0.379	0.392	9.0
132	40.448	41.252	43.118	6.6
132	38.554	39.707	38.602	0.1
246	82.412	84.219	88.270	7.1
246	77.789	79.157	78.930	1.5
384	108.800	113.265	119.071	9.4
384	109.931	109.782	113.748	3.5
530	152.799	157.965	161.965	6.0
530	159.962	161.684	159.326	-0.4
Total 2608				

*Chain resistance is low initially, due to suspected electrical short.

**Chain increase cause unknown, though possibly water related as packages was accidentally submerged in water and then subsequently dried.

TABLE V
PACKAGE C HUMIDITY MEASUREMENTS

Contacts Per Chain	Four-Wire Resistance, ohms			% Change
	Initial	909 Hours	2347 Hours	
2	0.352	0.349	0.352	0.1
2	0.367	0.358	0.360	-1.9
2	0.351	0.347	0.347	-1.1
2	0.371	0.356	0.355	-4.7
2	0.388	0.368	0.365	-6.4
2	0.390	0.366	0.363	-7.3
2*	0.234	0.242	0.263	10.8
2	0.243	0.245	0.245	0.7
2	0.262	0.251	0.247	-6.0
2*	0.258	0.271	0.283	8.8
134	46.012	44.551	44.359	-3.7
134	46.597	44.587	44.301	-5.2
246	90.377	89.284	89.090	-1.4
246	93.151	90.352	89.807	-3.7
384	128.603	127.055	127.238	-1.1
384	132.793	127.651	127.068	-4.5
530	177.211	177.477	178.036	0.5
530	185.669	180.171	179.276	-3.6
Total 2608				

*Chains increasing; suspected gap issue because both on corner of package.

TABLE VI
PACKAGE D THERMOCYCLE MEASUREMENTS

Contacts Per Chain	Four-Wire Resistance, ohms			% Change
	Initial	435 Cycles	1082 Cycles	
2	0.232	0.222	0.217	-6.5
2	0.232	0.233	0.226	-2.7
2	0.240	0.255	0.247	2.8
2	0.230	0.247	0.246	6.9
2	0.230	0.219	0.216	-6.1
2	0.236	0.222	0.214	-9.2
2	0.191	0.189	0.201	5.3
2	0.206	0.190	0.190	-7.9
2	0.189	0.178	0.177	-6.3
2	0.194	0.198	0.193	-0.8
134	29.303	28.243	28.135	-4.0
134	29.579	28.474	28.240	-4.5
246	60.408	58.821	58.705	-2.8
246	60.539	58.866	58.658	-3.1
384	87.527	85.201	84.465	-3.5
384	87.801	86.363	86.353	-1.6
530	116.468	113.676	113.717	-2.4
530	119.233	115.577	114.736	-3.8
Total 2608				

TABLE VII

PACKAGE E THERMOCYCLE MEASUREMENTS

Contact Per Chain	Four-Wire Resistance, ohms			% Change
	Initial	322 Cycles	1112 Cycles	
2	0.238	0.230	0.228	-4.1
2	0.233	0.229	0.228	-2.2
2	0.220	0.218	0.215	-2.4
2	0.229	0.227	0.225	-2.1
2	0.238	0.228	0.228	-4.3
2	0.242	0.227	0.225	-6.7
2*	0.181	0.173	0.201	11.0
2	0.173	0.164	0.162	-6.5
2	0.165	0.159	0.157	-5.2
2	0.171	0.182	0.172	0.8
134	28.836	28.066	27.848	-3.4
134	29.022	28.269	28.051	-3.3
246	59.129	57.584	57.054	-3.5
246	59.777	57.961	57.408	-4.0
384	82.418	82.069	81.327	-1.3
384	78.453	78.585	77.799	-0.8
530	117.680	113.601	113.111	-3.9
530	117.205	114.195	115.975	-1.0
Total 2608				

*Chain had a bubble contacting springs, caused by insufficient underfill supply.

Detailed reliability results for packages with springs in air and springs embedded in adhesive are given in Tables III–VIII. All four-wire measurements of contacts are reported for each

package (2608 total). In general, the initial uniformity of the measurements within each contact chain type (highlighted) is less than 5% within a package. Variations between packages

TABLE VIII
PACKAGE F THERMOCYCLE MEASUREMENTS. PACKAGE F HAS UNSTABLE INITIAL RESISTANCE VALUES. THEREFORE % CHANGE IS CALCULATED BETWEEN 160 h AND 7746 h

Contacts Per Chain	Four-Wire Resistance, ohms			%
	Initial	160 Cycles	7746 Cycles	
2	0.364	0.357	0.348	-2.7
2	0.356	0.361	0.359	-0.4
2	0.365	0.371	0.36	-2.9
2	0.375	0.37	0.359	-2.9
2	0.146	0.374	0.36	-3.7
2	0.344	0.275	0.285	3.7
2	0.353	0.344	0.277	-19.4
2	0.258	0.262	0.248	-5.5
2	0.18	0.293	0.282	-3.7
134	44.753	44.406	43.434	-2.2
134	44.495	44.229	43.211	-2.3
246	90.561	93.858	89.506	-4.6
246	90.511	98.071	90.528	-7.7
384	127.219	128.525	125.921	-2
384	128.287	129.145	126.373	-2.1
530	177.553	175.475	172.228	-1.9
530	7799.544	180.266	176.815	-1.9

Total 2608

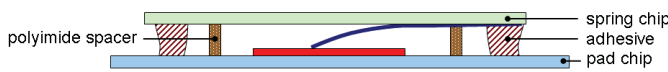


Fig. 12. Schematic of assembled Package A.

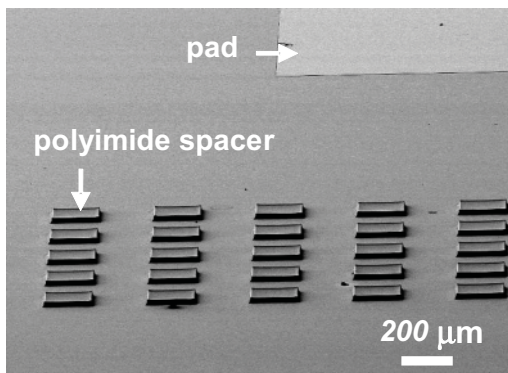


Fig. 13. SEM image of the polyimide spacer.

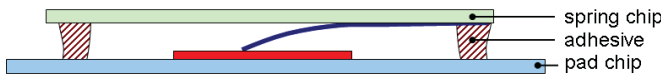


Fig. 14. Schematic of assembled Package B.

are attributed to variations between the spring trace and pad trace metal thickness, as pad chips and spring chips are from different fabrication process runs.

Certain chains with relatively high resistance are denoted with asterisks. Inspections show that most are caused by clear assembly or spring fabrication defects, such as particles near

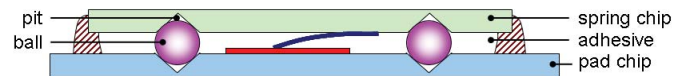


Fig. 15. Schematic of assembled Package C.

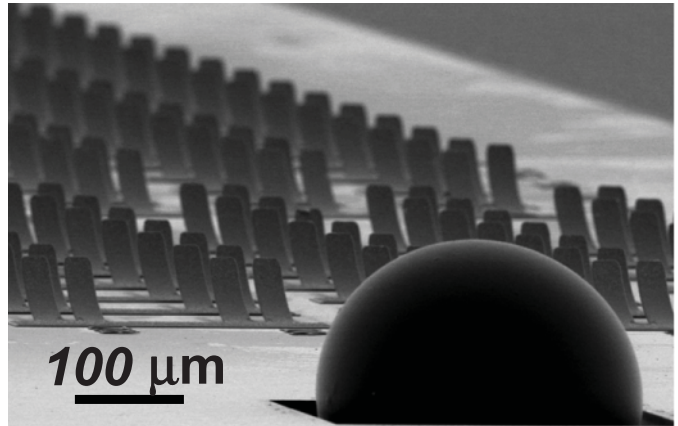


Fig. 16. SEM image of balls/pits with springs [19].

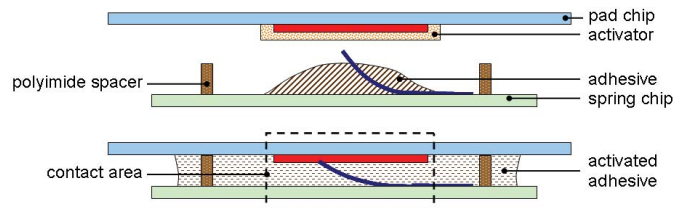


Fig. 17. Adhesive near the contacts of Package D cured by activator and edges cured by UV light.

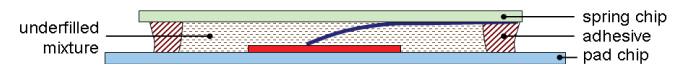


Fig. 18. Schematic of Package E.

the spring tips, lithography defects, or air bubbles in the case of adhesive. It is important to avoid these defects, as during assembly process development it is observed that these defects can also cause clear failures such as large resistance increases or opens.

1) Air-Gap Package (Thermocycle):

Package A: Package gap is defined by a lithographically defined polyimide spacer. The Loctite 352 adhesive holds the spring and pad chips together after UV curing. The adhesive is applied at four corners of the chip, see Figs. 12 and 13.

2) Air-Gap Package (Humidity):

Package B: Package gap control is performed by a precision flip-chip assembler. The Loctite 352 adhesive holds the spring and pad chips together after UV curing, see Fig. 14.

Package C: Package gap is defined by self-aligned balls and pits. Loctite 352 on edges holds the spring and pad chips together after UV curing (Figs. 15 and 16).

3) Embedded Package (Thermocycles):

Package D: Package gap is defined by polyimide spacer. Contact area is cured by Loctite 352 which is activated/cured

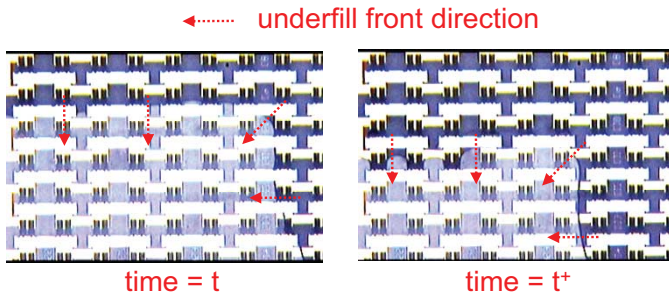


Fig. 19. Image of Package E during underfill. Capillary force pull the adhesive toward the bottom left of the image.

by the activator. Noncontact area is cured by the adhesive that is cured by UV light, see Fig. 17.

Package E: After assembly, Loctite 352 on the corners only holds the package. The package is underfilled by the self-curing and UV curable mixture. Non-contact area on the edge is cured by UV light, see Figs. 18 and 19.

4) Embedded Package (Humidity):

Package F: The assembly method is the same as package D.

VI. CONCLUSION

A microspring capable of low resistance ($<100\text{ m}\Omega$), high compliance ($>30\text{ }\mu\text{m}$), and dense 2-D array pitches ($180 \times 180\text{ }\mu\text{m}$) has been demonstrated. The components of the resistance have been analyzed in detail, suggesting that the tip-pad interface is $<40\text{ m}\Omega$ for the contact area ($100\text{ }\mu\text{m}^2$) and force (0.01 grams) used in these contacts. High yield and uniform fabrication enables flip-chip packages with 100% assembly yield with thousands of contacts. A variety of packaging methods have been demonstrated, including springs in air, springs embedded, and use of different spacers (no spacer, polymer, ball-pit). *In situ* glitch testing shows no intermittent resistance increases during thermocycling. Stable or decreasing resistances were observed during thermocycle and humidity testing. Pre-scrubbing the tips was found to be a beneficial assembly step.

This paper suggests that a micropressure contact can be used for next-generation flip-chip packaging. Such an architecture can enable new ways to address the known-good-die problem, which prevents more complex MCMs from being fabricated, because the chips can be tested at speed and reworked if needed before final assembly. The fabrication process is scalable to even smaller pitch 2-D arrays because it is based on lithographically patterning of thin films. Similarly, if less than $30\text{ }\mu\text{m}$ vertical compliance is required, shorter springs can be used, enabling lower resistance and increased parallelism. Note that while solder and gold bumps have already demonstrated $<100\text{ m}\Omega$ contacts, these have negligible compliance compared to the springs. The gaps (bond-line) between the chip surface and pad surface is approximately $18\text{ }\mu\text{m}$ in this paper, but can be made much smaller as the springs are designed to be fully compressible. This enables packages with smaller vertical heights. The spring compliance can accommodate more thermal expansion mismatch than conventional approaches.

The springs have the potential to be a basic enabler for future microsystems.

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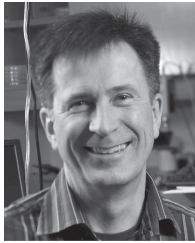


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