High Performance Multilayer PCBs Design and Manufacturability

Judy Warner, Transline Technology
Chris Savalia, Transline Technology
Michael Ingham, Spectrum Integrity

IT STARTS WITH THE DESIGN:

Multilayer printed circuit boards (PCBs) that utilize high performance materials are inherently far more challenging for a fabricator to build, due to significant material property differences over standard epoxy glass FR4. These unique material characteristics often require higher processing temperatures, special surface treatments (to aid in hole and surface plating), they possess different expansion properties, making layer-to-layer registration more difficult to control, and require many other unique considerations.

A designer can avoid making these, already difficult, fabrication challenges even more difficult by being aware of the "PCB Fundamentals." In doing so, a designer can reduce the number of unnecessary critical features; create a more robust design, while optimizing performance and cost.

THE CHALLENGE:

Over the past decade there has been a vast increase in higher integration of functions built into semiconductor component devices, and these devices are running with much greater signal speeds. For critical applications, and when using high-pin count highly integrated devices, there is now a need to run very high speed signals on multiple layers using high-performance dielectrics. Compound this with applications including both RF and high-speed digital in the same circuit; a circuit now has requirements that compete with each other on the same PCB.

THE PROBLEM:

Essentially, there appears to be a widespread knowledge gap in knowing how to implement theory within the limits and guidelines of PCB manufacturing. Moreover, CAD design programs can let one inadvertently design a circuit that is impractical or impossible to build. The electrical aspects of these applications are quite complex and it is common to see the "PCB fundamentals" get neglected. There are very smart and talented engineers who are very knowledgeable of the electrical theory, but lack knowledge of the fundamental PCB manufacturing capabilities typically available. At the other end, there are highly skilled PCB Designers who lack the engineering expertise. A general observation is that more and more engineers and scientists are starting to try to do their own PCB designs due to the electrical complexity. Before one embarks down this path, it is imperative to get a firm understanding of "PCB Fundamentals" in regards to sound design and fabrication. Additionally, dedicated PCB Designers will need to learn additional skills and have access to a technical authority for guidance as needed.

COMMON DESIGN PROBLEMS (that make a hard problem, harder)

Specifying an overrated material

It is a very common oversight of a designer to select materials based solely on them possessing the lowest dissipation factor, or Loss Tangent, specification. This approach appears sound, but as a general rule, materials with the lowest loss tangent are going to be the most difficult to build, have the highest cost and may not necessarily give the best performance. Overrated material selection can make building a multilayer construction even more challenging than it needs to be which can create poor yields, drive up cost, minimize your capable supplier base, and in a worst case scenario, may be impossible to manufacture.

In addition to Loss Tangent, the following properties warrant careful attention:

Dielectric Constant is impacted by moisture. There are some materials that tend to absorb moisture and this can cause the effective Dielectric Constant to vary dramatically. Moreover, materials that absorb moisture are subject to absorbing certain chemicals during fabrication processing. It is important to be aware of this. For critical applications, choosing a material with very low moisture absorption is recommended. As a rule of thumb, Teflon/PTFE is less vulnerable to moisture, while ceramic loaded substrates and polyimide are more vulnerable to moisture.

Dielectric Constant can be affected by temperature. Be aware of the effects of Dk variance over temperature fluctuation and verify if a chosen material will be appropriate for the application. Some materials exhibit dramatic changes with temperature and this can cause performance problems that are extremely difficult to isolate.

Coefficient of Thermal Expansion. It is important to be aware of the expansion properties when designing a stack up. Avoid mixing materials with greatly different expansion rates. This can prevent potential fabrication problems and make your design more reliable.

Thermal Conductivity. Many devices dissipate a great deal of power. If a material has poor thermal conductivity, there can be localized heating and possible performance degradation for the high-powered device. It is good practice to pay attention to this specification if a design has high-powered devices.

Dimensional Stability. This is important for multilayer designs and will assist the fabricator. Using materials with poor dimensional stability can impact final yield and drive costs higher. This cannot always be avoided, but when you can, it will be helpful for both fabricator and assembler.

Copper Finish. This is often overlooked. At high frequencies, conductive losses due to *skin effect* are a significant component of overall loss. For very high-speed/high-frequency designs, choosing a smooth copper finish can give an added performance boost and will, many times, allow a lower grade material be used for some applications.

Signal Path Loss – not considering "the big picture"

It is very important to look at the big picture when selecting materials for use with critical signals. There are four main components of loss: conductive, dielectric, radiation, and "design induced". Taken collectively together, these determine the total loss for a given signal path.

Figure 1 below shows a general loss calculation accounting for both the dielectric and conductor loss. Note that the conductor loss is a significant contributor to overall loss.

Figure 1. Loss Calculation for a sample Transmission Line

Dielectric Loss – this is the component of loss contributed by the dielectric material. Choosing materials with low Dissipation Factors (or Loss Tangents) help to reduce this component. However, this is just one component of overall loss. By also attending to the other loss factors, it may be highly likely a material with a higher loss tangent may be acceptable. In this way, one can expect increased yields, lower costs and broader available supplier base.

Conductor Loss – this is due to the resistance of the metal of signal traces. It is important to note that for RF and higher signal speeds, the surface finish is a significant factor due to *skin effect* properties. The graph below in Figure 2 shows a simulation of Insertion Loss for two types of metal finish for the same dielectric material. The smooth finish performs substantially better.

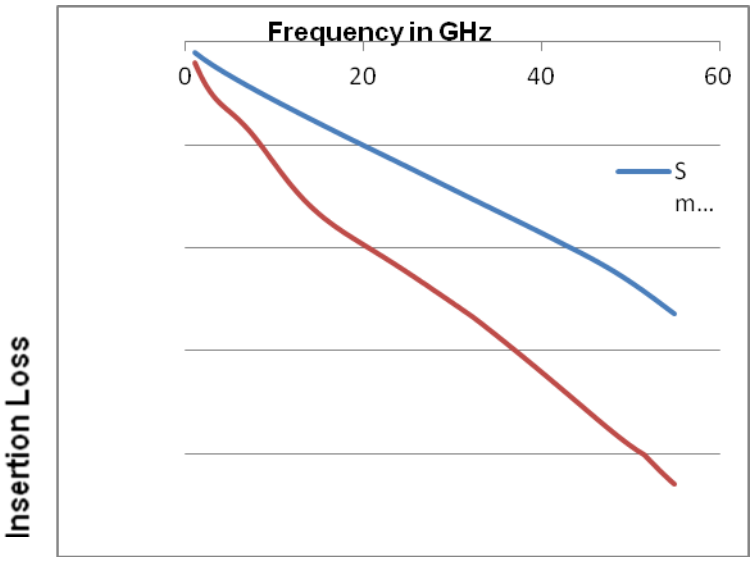

Figure 2. Insertion Loss Simulation for rough and smooth copper finish

Radiation Loss – this is due to the type of transmission line used. As a general rule, microstrip types of traces on outer layers will have more radiation loss compared to coplanar types of lines. Lines routed on internal layers, such as stripline types, have substantially less radiation loss.

Design induced Loss – these are generally due to discontinuities in signal paths. Care must be taken during the design phase to keep this at a bare minimum. Common ongoing problems seen include not properly transitioning between different types of transmission line structures, having gaps in ground planes underneath signals, not optimizing connector footprints to PCB (field match and impedance match), and many more.

Unbalanced Stack up

It is important to maintain a balanced stack up for multilayer PCBs that are using high performance materials. This means to maintain symmetry about the PCB center plane with both material type and thicknesses. Very often, much attention is spent in designing the layers which support the critical signals. Consequently, the layers that are not high-speed, or carry RF signals, get less needed attention. Too often, the stack up of these remaining layers is done as an afterthought. An unbalanced stack up can cause warpage, impact fabrication yields, and possibly add stress on plated through holes resulting in barrel cracks. Latent problems can occur long after fabrication, when the boards are being assembled. They may bow or twist as they become unstable after being subjected to an additional thermal cycle.

It is generally preferred to use a foil construction for a multilayer design as it reduces fabrication costs and is sometimes easier to build. However, there are a few things to keep in mind when it comes to a high-performance design:

- Controlled Impedance lines perform better if etched on a core rather than foil. For transmission lines that need to be on outer layers and have high performance, using core construction (where cores are on outer layers) will yield better impedance control and better performance due to the wide array of core materials available and better fabrication control.
- Some high-performance prepregs have lower copper peel strength and this can be a concern if a PCB needs to be reworked.

Stack ups that are not Practical or Possible

Unfortunately, it is quite common for a fabricator to receive data that specifies a stack up that just isn't practical or possible to build. For example: a symmetric stripline type of transmission line that is defined using two cores as the dielectric medium. Fusion bonding would be required to make this work, and this adds cost and is very difficult to build for a multilayer PCBs fabricator. In fact, only a handful of PCB manufacturers in the country can successfully perform fusion bonding. A better approach would be to use a core with the signal etched on its surface and closely matched prepreg material to make up the other section of dielectric to define the stripline structure. It appears that designers may sometimes not fully understand the differences between cores, prepregs, and bond ply materials. If unsure, it is highly recommended to consult with your fabricator, prior to design, when determining your stack up.

Incorrect use of Blind and Buried Vias

Today's CAD programs are all extremely powerful and it is very easy to design with unlimited flexibility if not being careful to set up the design environment to restrict how blind and buried vias are used. A basic knowledge of PCB sequential lamination is needed. Consult with your fabricator if unsure. It is quite common to see design data calling out a myriad of blind and via combinations which are just aren't possible or practical to be manufactured. Knowing the limitations ahead of time can save wasted time in having to redesign and reduce frustrations and manage fabrication costs more effectively.

Unrealistic Tolerances Specified

Many times PCB fabricators see tolerances specified that are beyond actual or typical manufacturing capabilities. This, of course, is not practical and causes delays and frustration for all involved. It is highly recommended to get familiar with the chosen fabricators capabilities, often listed on their websites, and not specify tolerances that are impossible or impractical. In addition, it is recommended to avoid specifying overly strict tolerances that aren't really necessary. These will add to the cost to fabricate and oftentimes won't give the desired performance benefit that was sought.

A common example is when a designer specifies very tight etch-to-artwork tolerances for controlled impedance traces that are beyond capabilities. True, the final trace width is a determining factor of the impedance, but specifying fractional mil tolerances doesn't have a significant impact on the final impedance. Very successful high-performance designs are continuously being produced with standard PCB manufacturing tolerances. Selecting materials with a well characterized dielectric constant and good thickness control are the main factors a designer can influence for targeting good impedance control.

High Drill Aspect Ratios

Multilayer PCBs using high-performance materials can become very thick as layers are added. It is important to not lose sight of hole aspect ratios (length to width) and keep fabrication capabilities in mind throughout the design process. A 6 mil finished hole size may be fully capable on a standard 0.062" thick PCB, but on a 0.093 (or thicker) these minimum hole sizes start adding to the cost and encroach on manufacturing capabilities.

Very Thin Transmission Lines

It is easy to draw nice looking traces on a CAD screen, with the image is magnified greatly, and to lose sight of how they will appear on the final product. It is common to see very thin transmission lines routed, such as differential pairs, over lengths of several inches. Thin lines are much harder to control impedance on, because the fabrication tolerances have a much greater impact. For example, a trace pair having line widths of 4 mils can suffer anywhere from a 12% to 25% difference between final etch and designed widths. Standard impedance tolerance is 10%, and if the fabrication tolerance impact is higher than this, impedance control becomes extremely difficult to maintain. To illustrate, a sheet of paper is approximately 3- 4 mils thick. A transmission line drawn at 4 mils may look reasonable on the CAD screen, but realize that this line will be near as thin as a sheet of paper. These tiny lines can easily suffer microscopic nicks during normal process handling—which can create problems that are difficult to detect in the future. In addition, conductive losses of such thin lines are much greater. Only use such thin lines when absolutely necessary. Avoid setting up global routing design rules for an entire board with very fine lines, when they are only needed in a few distinct areas.

Hole to Metal Clearances

High performance materials have very different scaling factors when fabricating, compared to FR4, and having tight hole-to-copper features can impact yield significantly. It is recommended to maintain a minimum of 0.012" clearance between copper features and drilled holes. If not possible due to tight breakout patterns, then using oblong shaped pads may be a compromise in squeezing as much clearance as possible.

Poor Documentation

Surprisingly, this is a common problem. Fabrication drawings are often omitted as well as fabrication notes. Other common problems arise when leftover "boiler plate" notes are cut and pasted to a drawing that do not apply to the existing design. At best, these will cause delays at fabrication due to time needed to straighten out and get clarification. At worst, the PCB can be built incorrectly and be of no use and get scrapped. The IPC maintains excellent standards for documentation and these are very helpful to consult. In addition, getting input from your fabricator on acceptable documentation is very helpful in avoiding this unnecessary problem.

Data Problems

Fabricators can cite endless examples of data problems they encounter when receiving fabrication data for a new build. Many of these can be avoided by setting up DRC rules in the design and also run DRC on *the data* and resolve errors prior to submitting. The easiest problem to avoid is to ensure all the data files are included along with a good Fabrication Drawing. Gerber files remain the preferred data format for most PCB fabricators. Most have conversion tools to accommodate many common data files, yet if you can supply Gerber data any conversion issues can be averted.

OVERLOOKED ITEMS THAT CAUSE PERFORMANCE EXPECTATIONS TO NOT BE MET

Performance not matching simulations

Advanced designs with RF and ultra high-speed signals frequently undergo extensive simulation and analysis during the design phase. It is not uncommon for simulation data to not match measured data from a finished PCB. One item of "disconnect" often seen is that engineers set up their simulation models using a copper thickness based on which copper thickness is called out, such as ½ oz, 1 oz, etc. The factor that often gets overlooked is when plated-through-holes get plated, this plating also gets added to the PCB outer layers. Since plating is a "wet process" where the manufacturing panel is immersed in a chemical bath for plating, plated holes typically get 0.001" of copper, and the outer layers also get this copper added. So if simulations are based on a ½ oz copper thickness (which is approximately 0.067"), the actual finished thickness can be 2X, or more, due to the hole plating process and this isn't being accounted for in the simulation model. This can throw off simulation data and impact designed etched features such as transmission lines, filters, coupled lines, etc.

A simplified graphical illustration of plating effects can be seen in Figures 3 and 4 below. Figure 3 shows a section of a 4 layer PCB with a drilled hole prior to hole plating. Figure 4 then shows the resulting plated hole and this extra plating being added to the outer layers. (the plating metal is shown as gold just for illustrative purposes)

With sequential lamination cycles, the effects can be more dramatic such as blind vias being exposed to multiple plating cycles. Figures 5 through 8 provide an example of plating effects due to multiple plating steps. The different colors of the metal shown below, gives a visual representation of the cumulative plating effects.

Illustrative example of effects of plating holes adding copper to outer layers:

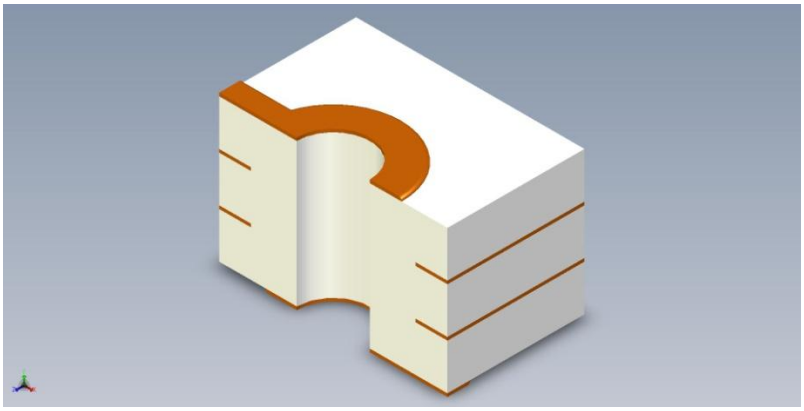

Figure 3. Drilled holes prior to plating

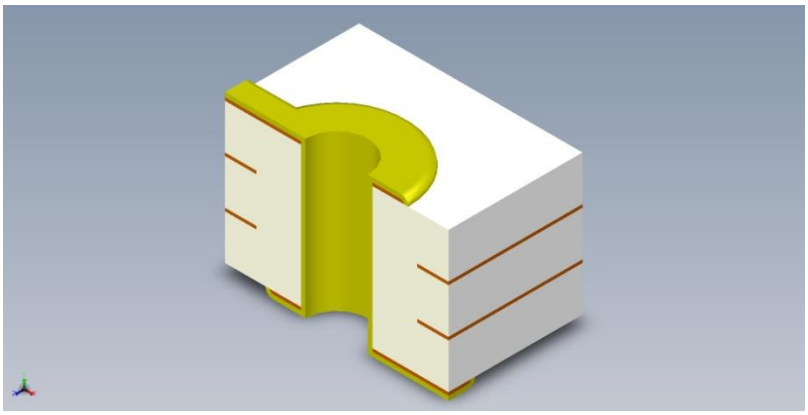

Figure 4. Drilled hole after plating

Illustrative example of effects of multiple plating steps adding copper to outer layers:

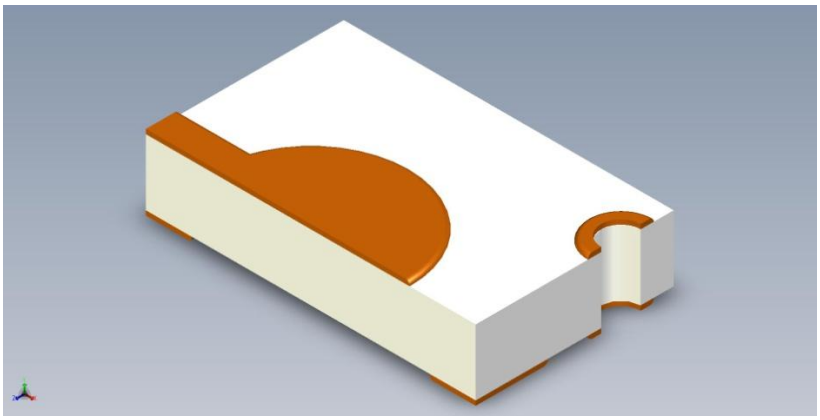

Figure 5. First core drilled prior to via plate

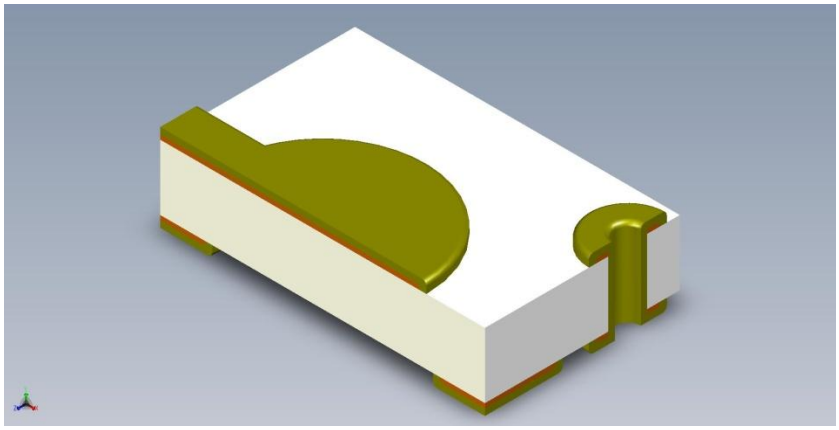

Figure 6. Core plated and copper gets added to all exposed surfaces

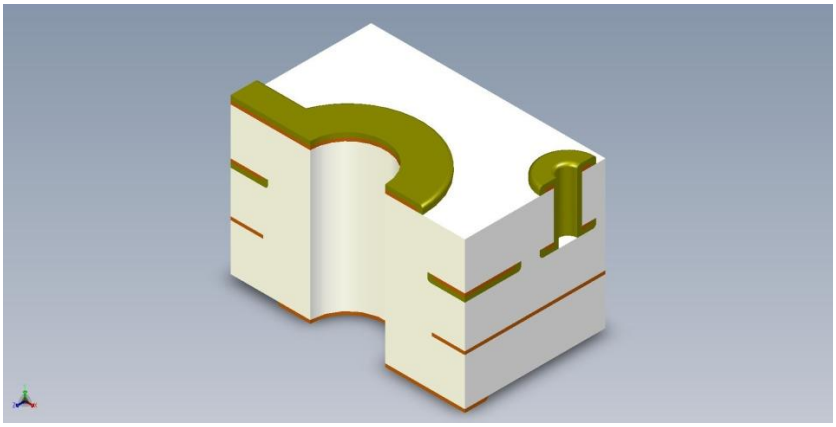

Figure 7. Core from Figure 6 gets laminated to form a four layer assembly and through holes are drilled

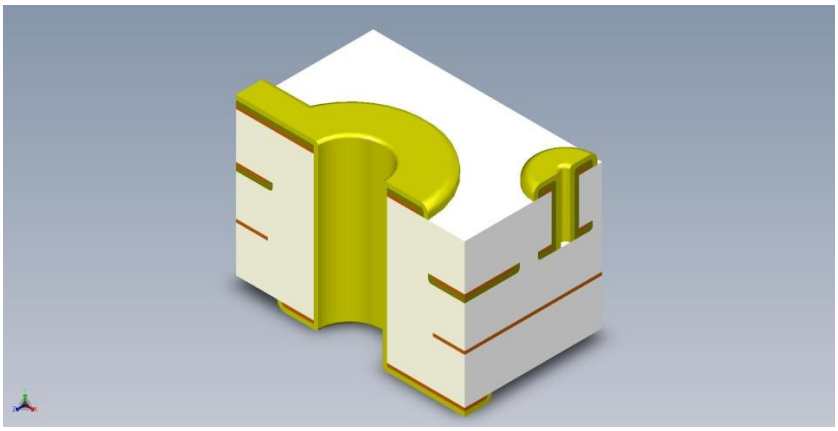

Figure 8. Four layer assembly through-hole plated and all exposed areas get copper added

CONCLUSION

High-Performance multilayer PCBs, that use high-performance materials, bring added challenges to both the fabricator and designer. It is important to be aware of current PCB fabrication fundamentals and to be aware of additional material properties besides the Dielectric Constant and Loss Tangent. This knowledge will prevent a designer from inadvertently making a design more difficult to build, and more costly than it should be. In addition, it will assist the fabricator with obtaining higher yields, better cost management, and producing robust, reliable PCBs. Collaboration and strong working partnerships between Material suppliers, Engineers, Designers and Fabricators will fill the existing knowledge gaps, and are the key to success when producing these unique products.

For Questions or additional information the authors may be contacted at the emails listed below:

Michael Ingham	Spectrum Integrity	michael@spectrumintegrity.com
Judy Warner	Transline Technology	judy@translinetech.com
Chris Savalia	Transline Technology	chris@translinetech.com