NSOP Reduction for QFN RFIC Packages

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Abstract
Wire bonded packages using conventional copper leadframe have been used in industry for quite some time. The growth of portable and wireless products is driving the miniaturization of packages resulting in the development of many types of thin form factor packages and cost effective assembly processes. Proper optimization of wire bond parameters and machine settings are essential for good yields.

Wire bond process can generate a variety of defects such as lifted bond, cracked metallization, poor intermetallic etc. NSOP – non-stick on pad is a defect in wire bonding which can affect front end assembly yields. In this condition, the imprint of the bond is left on the bond pad without the wire being attached. NSOP failures are costly as the entire device is rejected if there is one such failure on any bond pad. The paper presents some of the failure modes observed and the efforts to address NSOP reduction [1]

Introduction
Wire bonding process is one of the most critical processes in the integrated circuit(IC) package .Typical bond pad metallization consists of Aluminum with1% Silicon and 0.5% copper. The quality of the bond pad surface used for gold wire bonding is very critical for the overall package performance. For example the bond pad surface affects the wire bonding processibility during the package assembly process. A poor quality bond pad surface can result in NSOP and therefore a low yield during the wire bonding process. The paper addresses the quality issues affecting NSOP failure mode. It summarizes the different failure modes observed from wafer fabrication as well as wafer backend operations of laser scribe, singulation and wire bond assembly operations[2]

Overview of Assembly Process Flow
The package assembly is preceded by wafer back end processes which may include wafer probe, backgrinding, wafer saw, singulational of which can affect bond pad quality if not properly controlled and optimized. . Figure 1 shows the wafer backend process flow.

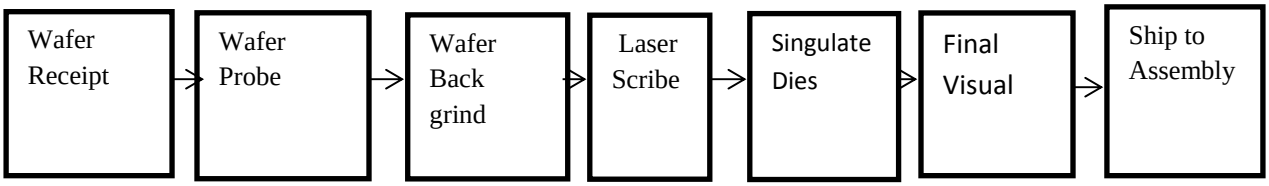

Figure -1- Wafer Backend Process Flow

Wire bonded assembly has a unique process flow and material set to provide optimum yield. Wire bond assembly operations are separated as front end of line(FOL) and back end of line (BOL). FOL includes die attach, wire bond and 3rd Optical inspection. EOL includes mold, cure, mark, plate and singulation processes as shown in Figure 2

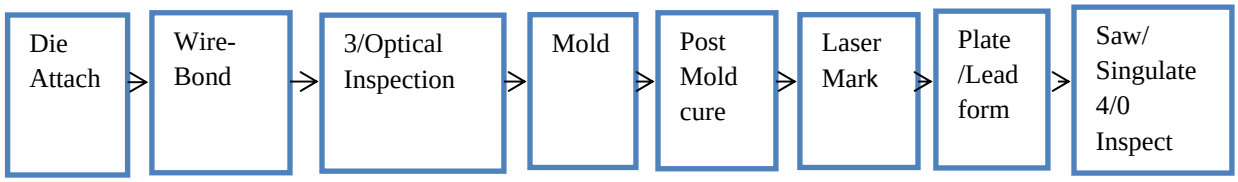

Figure 2 Wire Bond Assembly (Metal leadframe, gold wire)

After completing assembly, packages go through Test, Tape and Reel and are then packaged for shipment.

Incoming Defects and failure mode evaluation

Prior to initiating die attach and wire bond operations, the wafer are subjected to incoming quality inspection and sort to minimize escape of defects to the assembly operations. There is a variety of wafer back end defects that can escape to assembly if not properly screened. Figure 3 shows the IQC process flow.

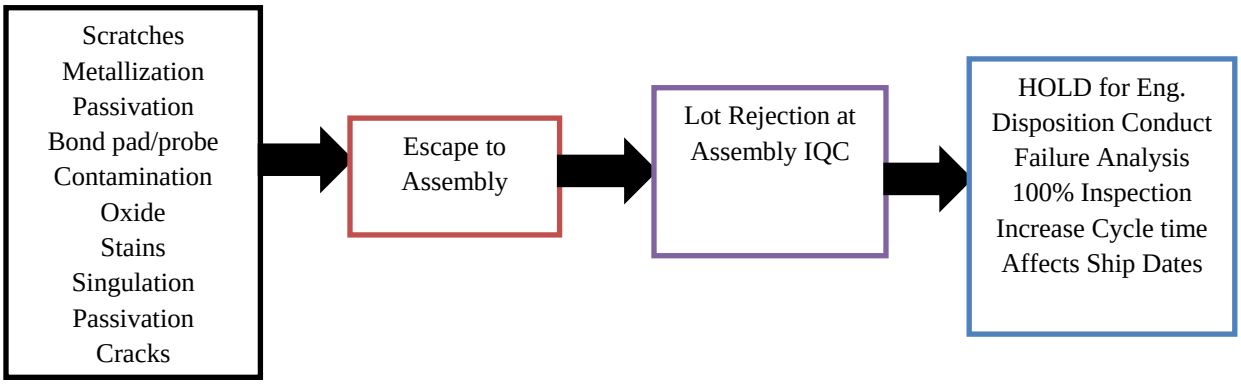

Figure 3 – Incoming Quality Process Flow

The wafer IQC is done at LTPD 95/5 with a sample size of 45 per wafer. 10 dies are inspected per quadrant of wafer and 5 dies are inspected in the center of the wafer. The lots were experiencing a high rejection rate due to defects such as contamination, broken die, metal scratch, foreign material etc. Figure 4 shows typical defects seen at IQC.

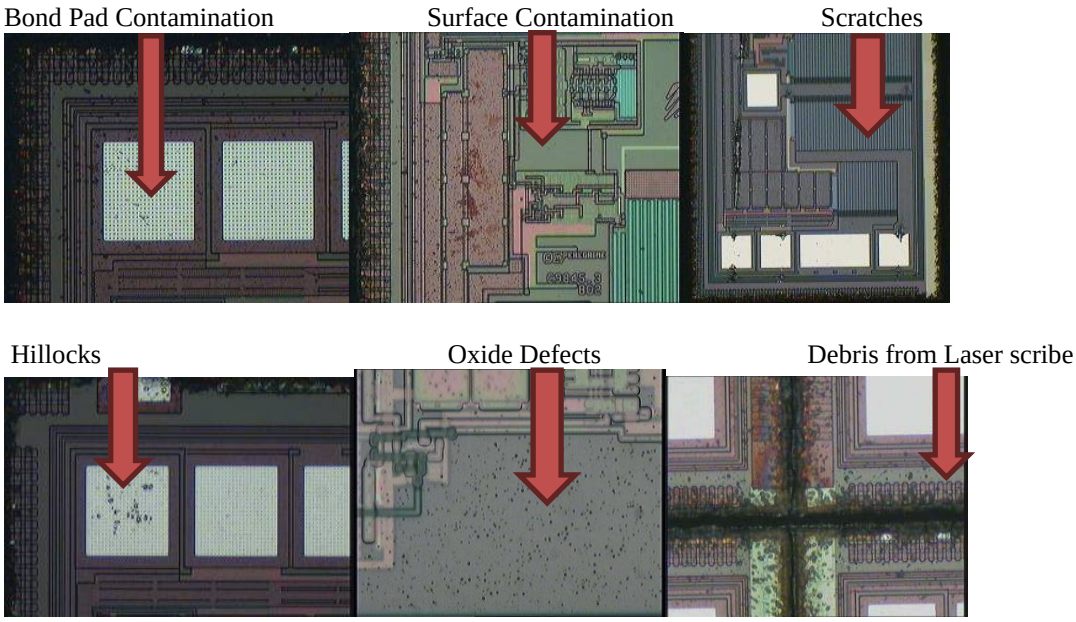

Figure 4- Typical Defects at IQC

Failure Analysis:

Contamination, scratches, foreign material etc. seen on the bond pads are of prime concern to wire bonding yields.
However, some of the defects seen on the passivation layer and other areas of the die were also characterized to see if they were embedded or removable by wash operations. One such defect was showing up as contamination on the die surface. SEM/EDX analysis was conducted to get a better understanding of this defect. Figure 5 shows the SEM image of the surface contamination. This image is showing the dirt and particles on the die surface. These are presumed to be from the laser scribe operation.

Figure 6 is an EDX dot map for aluminum. Concentrations of aluminum are indicated by the yellow contrast.

Surface Particles Aluminum particles

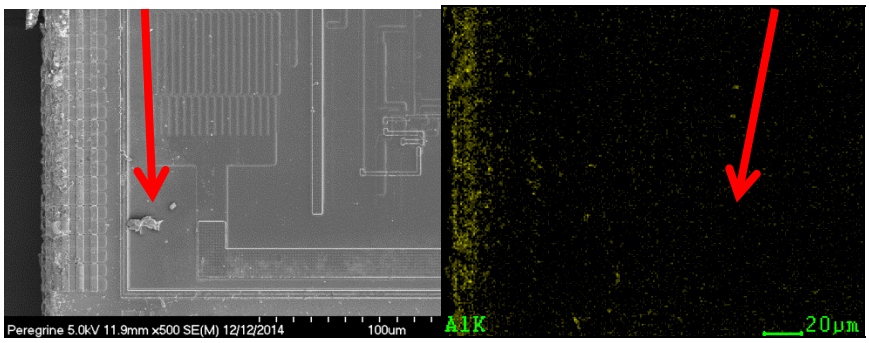

Figure 5 -surface contamination **Figure 6 – Aluminum particles**

Defect characterization was needed to understand the failure mode and clarify the acceptance criteria at IQC.

Another defect that was characterized was "Hillocks" seen on the bond pads. It was seen both on the passivation layer and the bond pad and the concern was damaging the wire bonds. Hillocks in both areas were analyzed to understand the composition and height of the hillocks. Figure 7 shows the SEM image of the hillock on passivation layer and Figure 8 shows the hillock on the bond pad.

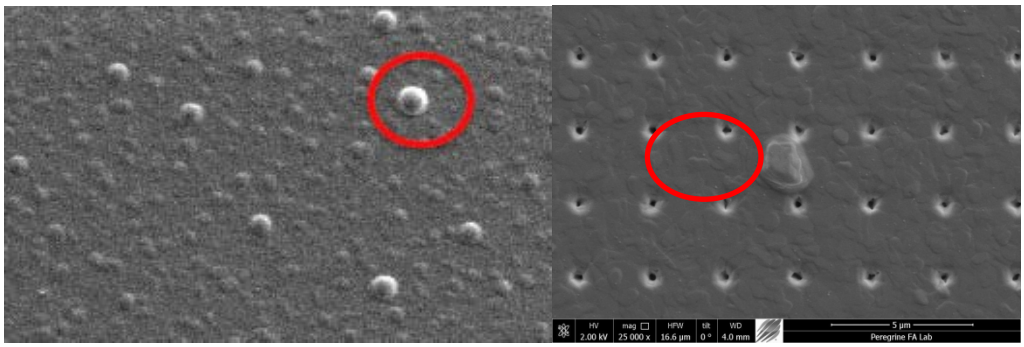

Figure 7- Hillocks on passivaton **Figure 8- Hillocks on bond pad**

After failure analysis it was determined that Hillocks were not a major issue for NSOP, so the IQC acceptance criteria for hillocks was revised.

Wafer Backend Process Improvements

In order to address defect escape, failure analysis was conducted as shown above and defects were categorized as wafer incoming, and defects induced in the backend process. The goal was to characterize the top 3 defects and reduce lot rejection rate at IQC. In order to accomplish this, Automated Optical inspection (AOI) was added to screen defect before shipping to assembly. AOI acceptance criteria was defined for each defect and programmed in the machine. This replaced the optical inspection and improved the cycle time. AOI also helped tracking repetitive defects and isolating defect categories by product type. At the same time an effort was made to root causes the defects at the backend process. By using a multiple screening approaches and focusing on the backend processes, the defect escape was reduced as shown in Figure 9and Figure10.

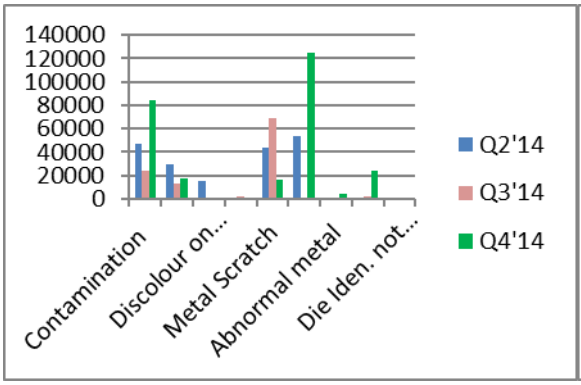

Figure 9- 2014 IQC Defect PPM

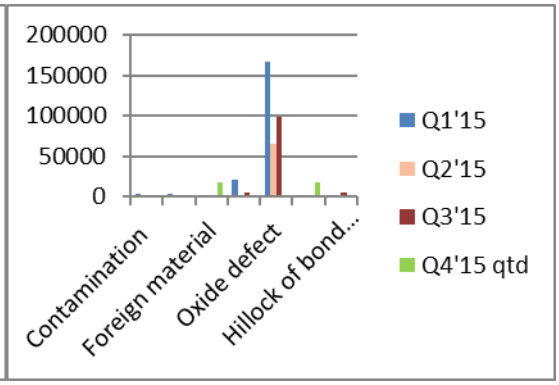

Figure 10 2015 IQC Defect PPM

Assembly Process Optimization

Wire bond process optimization begins with a clear understanding of the bonding equipment, machine set up, the response variables involved and their relationship to one another. [3]. Surface cleanliness and bond pad metallurgy are critical for successful wire bonds. Evaluating these parameters is time well spent and an important step towards developing a robust wire bond process. Well optimized processes lead to improved Cpk (process capability index) and good yields. For volume manufacturing, consideration should also be given to cost, portability of the process and reliability.

When the wire bond assembly was initiated for production, designed experiments were conducted to dial in the wire bond process using bond power, bond force, and bond time and bond temperature as the variables. The key bond parameters were compared for several packages to understand package commonality. Capillary design and dimensions are also an important variable for optimization. Typical response variables of a wire bond process is wire pull data (5gms min) and ball shear data. (15gms min).

During the wire bond process, the dies that exhibited "Non Stick on Pad" (NSOP) condition were isolated and mapped to the position on the wafer map. This was done to enable the location on the wafer where contamination was occurring and use this data to provide feedback to the wafer fabs. SEM/EDX analysis was performed on the NSOP dies to understand the type of contamination. The mapping is shown in Figure 11.

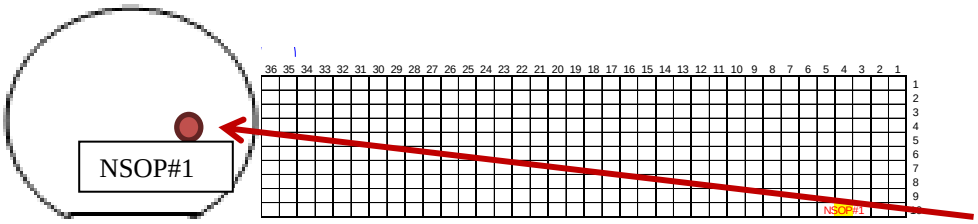

Figure 11- Process mapping of NSOP location on lead frame to die position on wafer.

The results of SEM/EDX analysis showed that high% atomic oxygen and carbon elements on the pads with contamination. The results also showed some Na, Cl, N, Fe Zn, Mg and K on the NSOP dies. Some fluorine element was also seen on good units. It is possible that Na, K and Mg might come from handling and finger touching, but the other contamination was not induced in the assembly process. Table 1 shows EDX analysis of good units and Table 2 shows the EDX analysis of NSOP units.

Unit	O	Al	C	F
1	1.5	98.5	0	0
2	1.62	98.38	0	0
3	1.48	98.52	0	0
4	1.56	98.44	0	0
5	1.61	98.39	0	0
6	1.65	98.35	0	0
7	1.36	98.64	0	0
8	1.60	98.4	0	1.12

Table 1 – EDX Analysis – Good Units

Table 2- EDX Analysis – NSOP Units (%atomic)

Unit#	Point	O	Al	C	F
1	1	9.27	81.55	9.18	0
	2	14.79	0	18.91	0
2	1	4.28	37.30	5.96	0
	2	3.00	93.32	2.21	1.47
3	1	1.79	94.72	2.39	1.10
	2	0	0	100	0
4	1	18.34	36.76	31.76	0
	2	13.00	14.51	43.74	0
5	1	7.59	36.60	7.71	0
	2	16.22	1.54	54.06	0

The process mapping experiments assisted in verifying the root cause of NSOP was bond pad contamination.
As a follow up parallel efforts were put in addressing the defect escape from back end processes. It was observed that the high carbon on bond pads was contributed by the tape residue from the back end operations. Rinse operations were optimized by adjusting the spray pressure and angle of the spray to facilitate proper removal of the residue and minimize escape to assembly operations. Recipes for laser scribe operations were verified to minimize debris from backend laser scribe operations. By putting controls in the backend operations and screening defects using AOI, outgoing DPPM was reduced and this facilitated in improving lot rejection rate at assembly IQC and reduced the NSOP defect at wire bond assembly. This was achieved with team efforts of in-house manufacturing and quality organizations and subcontract process engineering teams. Figure 12 shows the 2014 NSOP PPM and Figure 13 shows the reduction in 2015 NSOP DPPM

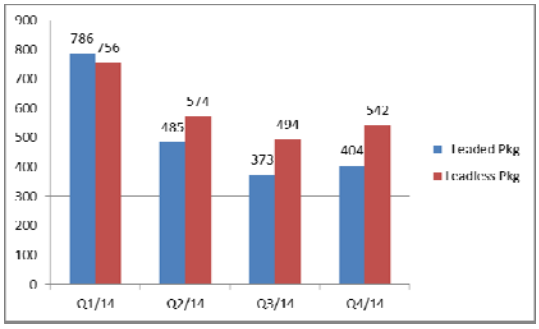

Figure 12- 2014 NSOP PPM

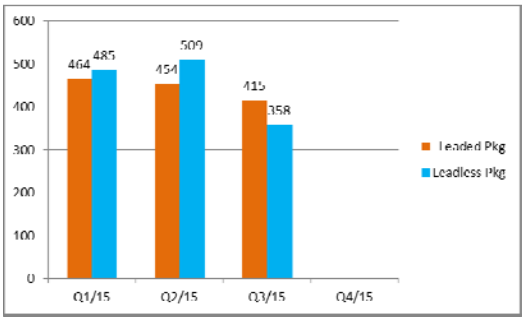

Figure 13- 2015 NSOP PPM

Conclusion

Die bond pad quality can be affected in numerous ways during processing and handling. Both wafer fabrication and assembly facilities as well as intermediate process owners such as probe/back grind/laser scribe/singulation operations need to address outgoing quality issues with proper detection and preventive methods. Automated Optical inspection (AOI) is a valuable tool in screening defects and categorizing them. Successful and reliable wire bonding can be achieved by contamination free surface, machine maintenance, optimized process settings and providing an optimal bonding environment.

Acknowledgements

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References

1. Wire Bonding in Microelectronics – Material s, Processes, Reliability and Yields George Harman
2 Reducing non-stick on pad for wire bon d: A review RS Sethu AJME Vol.9, No.2 pp 147-157
3 Bonding Process P.S. Chauhan et al. DOI 10.1007/978/-14614-5761-9_2

NSOP Reduction of QFN RF-IC Packages

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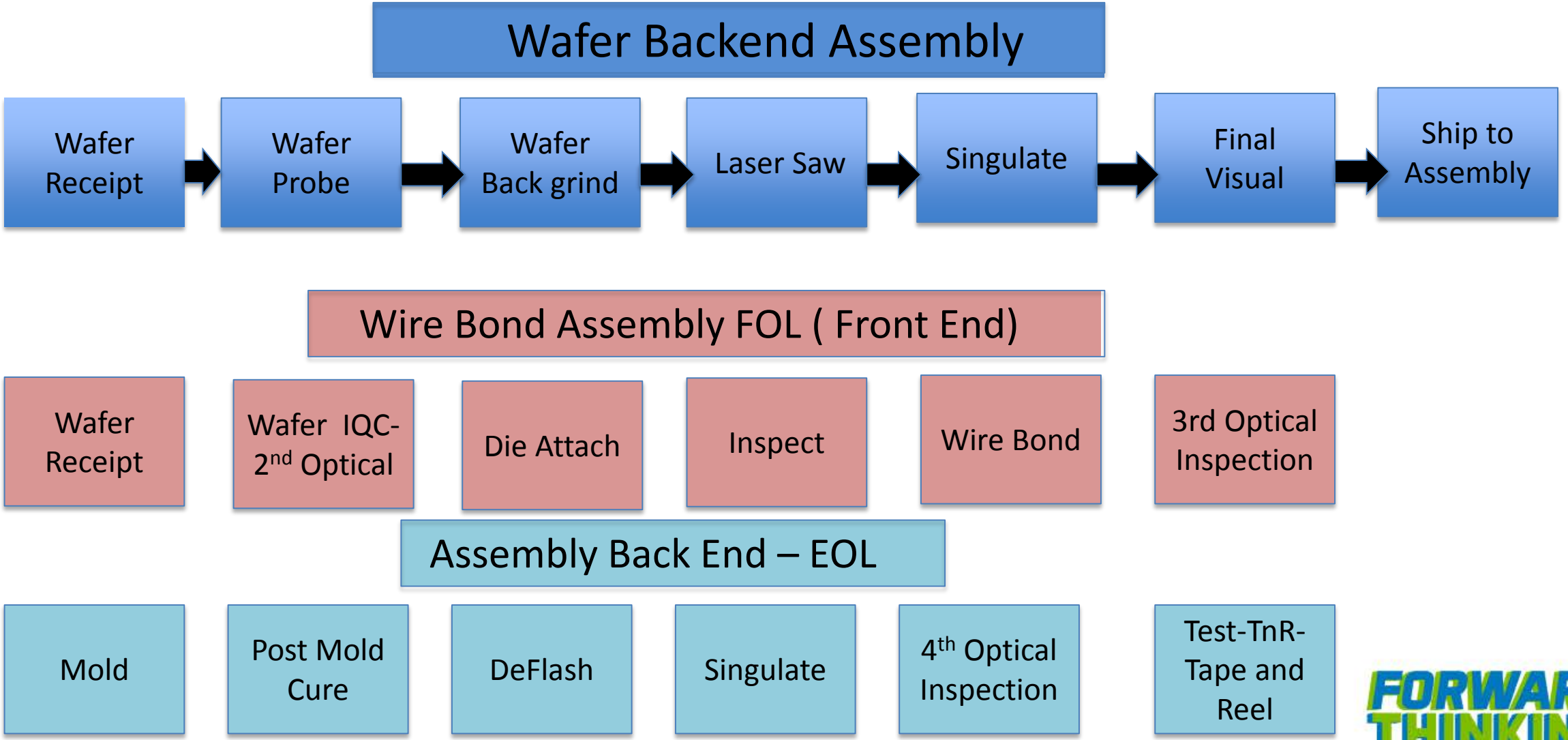
Overview

- Objective
- Backend Process Flow
- Assembly Process Flow
- Failure Isolation
- Process Mapping
- Failure Analysis
- Process Optimization
- Future Outlook

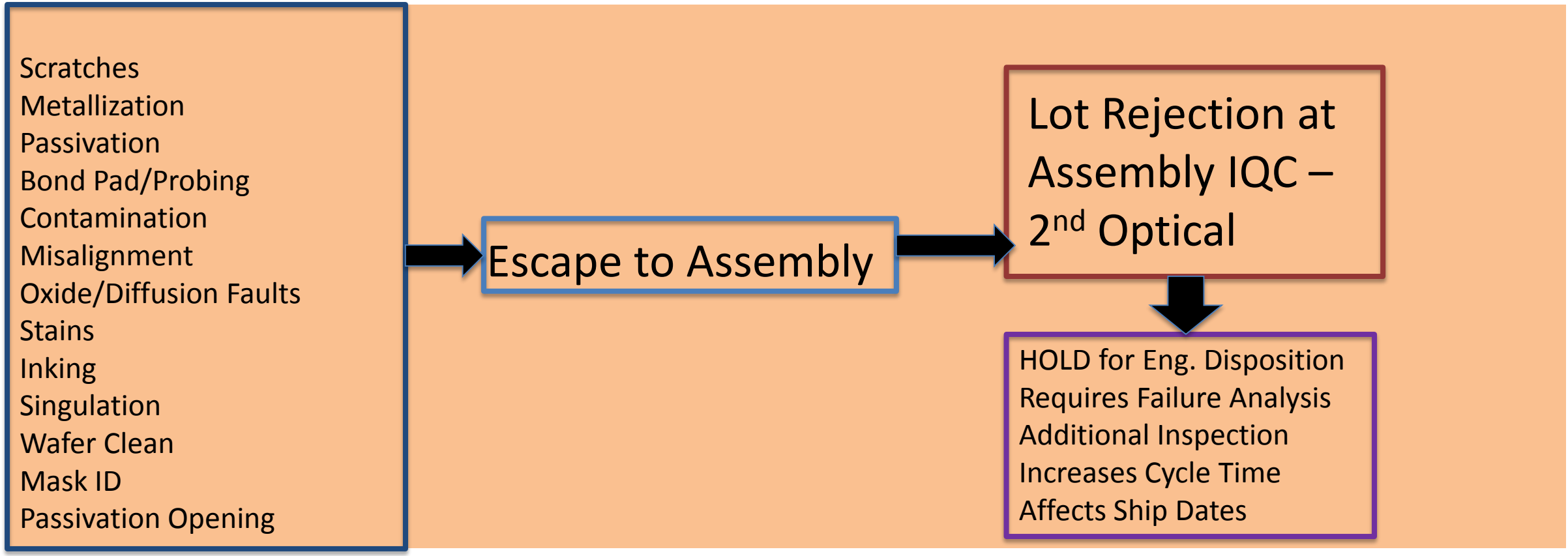
Objective

- To reduce Lot rejection rate at wafer IQC (Target-5%)
- To reduce DPPM at Wire bond Operation (Target -100PPM)

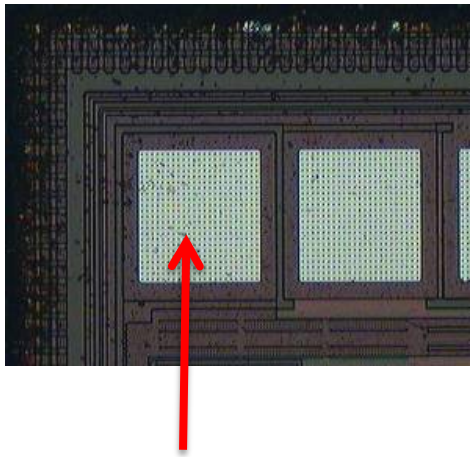
Assembly Process Flow



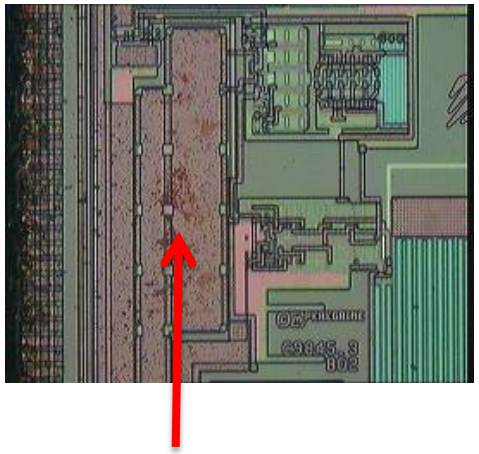
Typical Defects at Wafer Backend



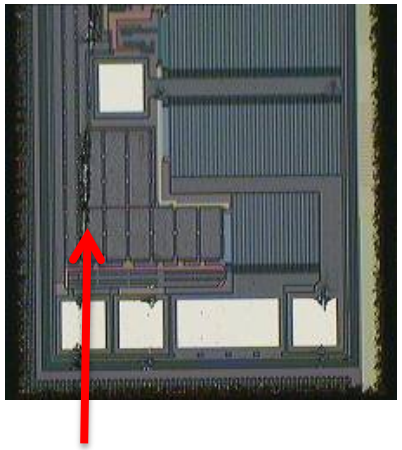
Defects Identified at IQC



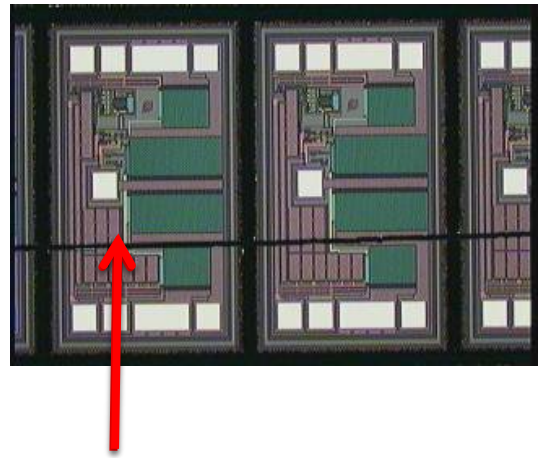
Bond pad contamination



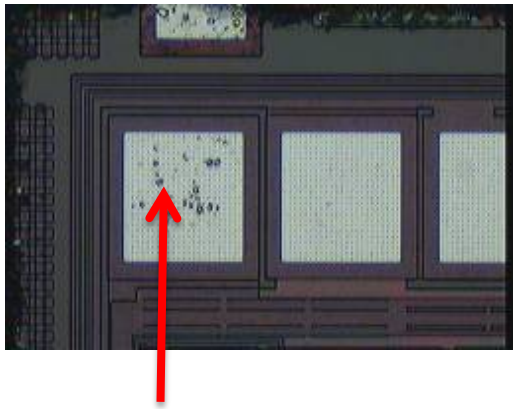
Die Surface Contamination



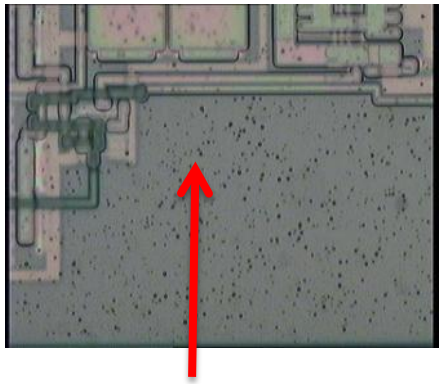
Scratches



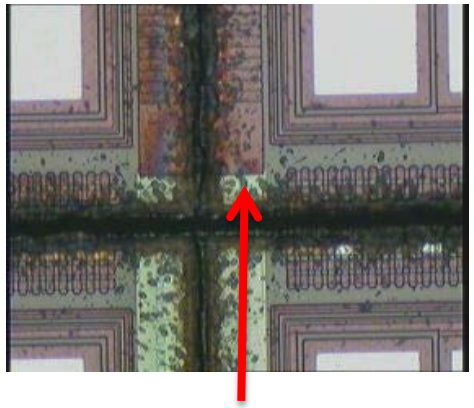
Cracks



Hillocks on Bond Pad

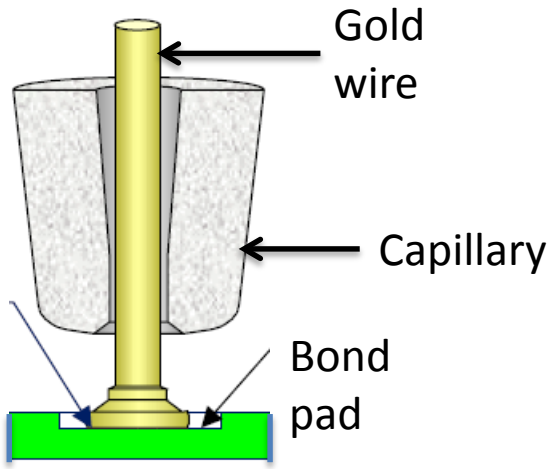


Oxide Defects

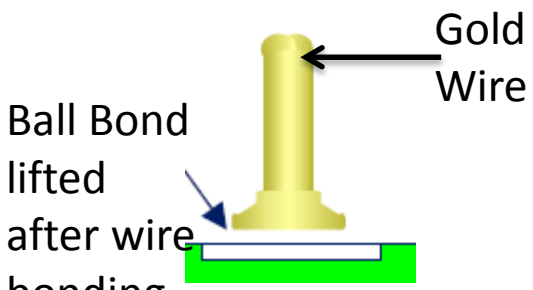


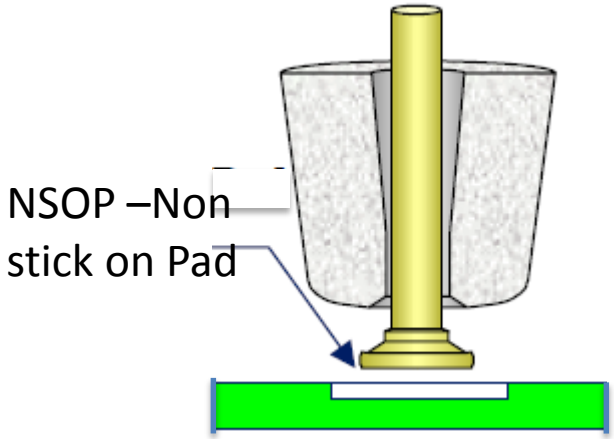
Debris from sawing

Wire Bond Defects



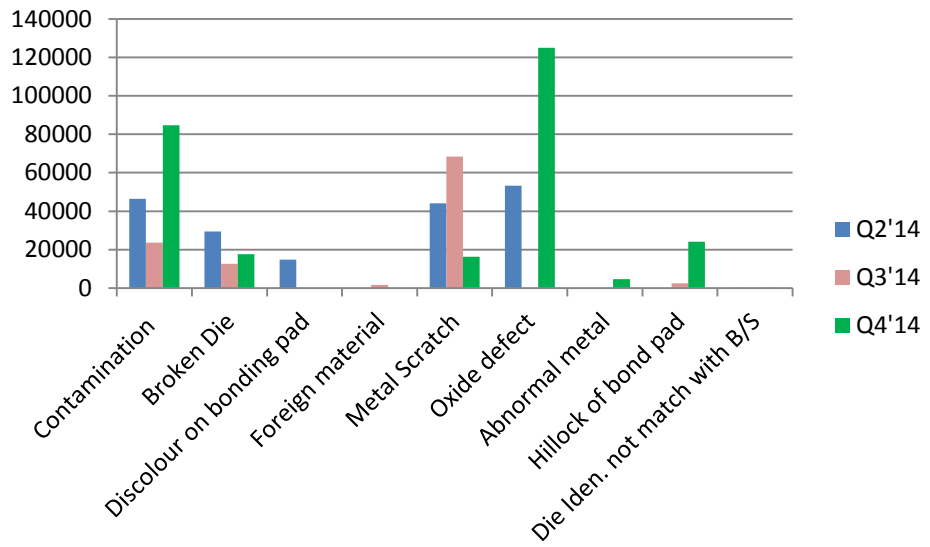
Acceptable
Wire bond





Assembly IQC

- Wafer IQC- LTPD 5%-sample size 45 10/per quadrant and 5 center –X100
- Q2014 -LRR- High Lot Rejection Rate – 50- 60%
- Typical Defects –Contamination, Broken Die, metal scratch, foreign material
- 2014 IQC Defects-PPM

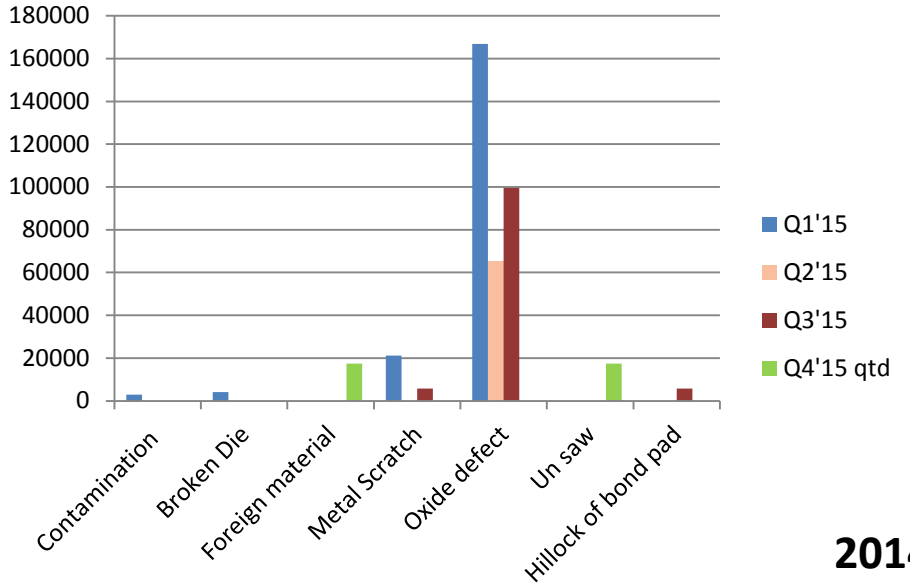


Goal – Focus on top 3 defects and reduce Lot rejection rate at IQC and wire bond assembly

Implement AOI (Automated Optical Inspection) at Wafer Back end, Isolate and Root Cause Defects

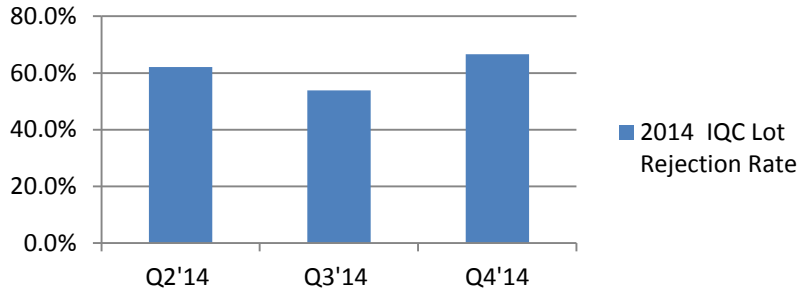
AOI Implementation

2015- IQC Defect PPM

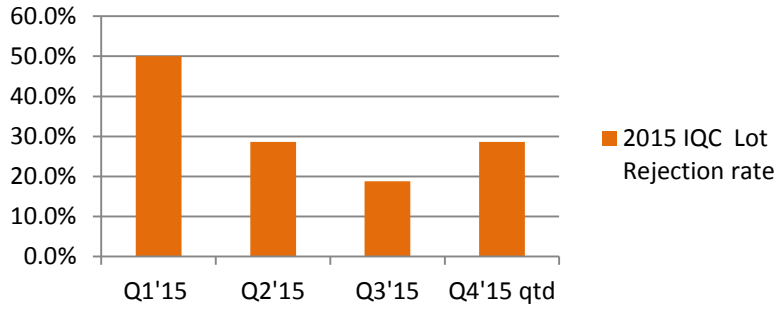


Defects from wafer Fab
Defect induced during backend process
Defects induced in transit

2014 IQC Lot Rejection Rate

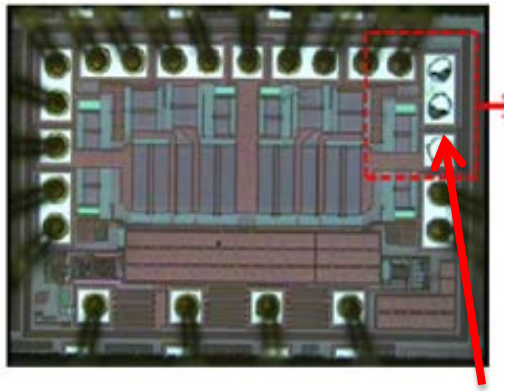


2015 IQC Lot Rejection Rate

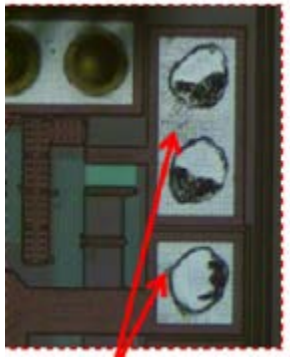


Wire Bond Assembly

- Ball Bond on Die
- Stitch Bond on Post
- 1mil gold wire on Aluminum Bond pad
- Process Variables
  - Bond Temp.
  - Bond Time
  - Bond Force
  - Bond Power
  - Capillary Design



Non Stick Bond

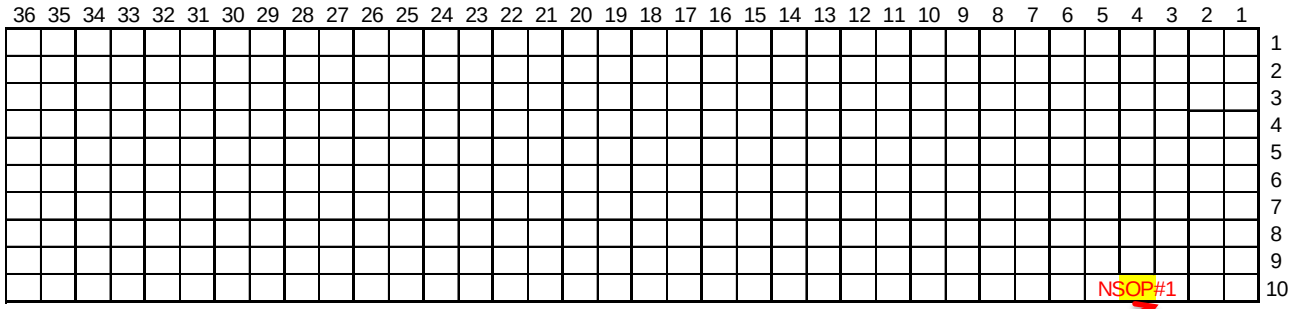


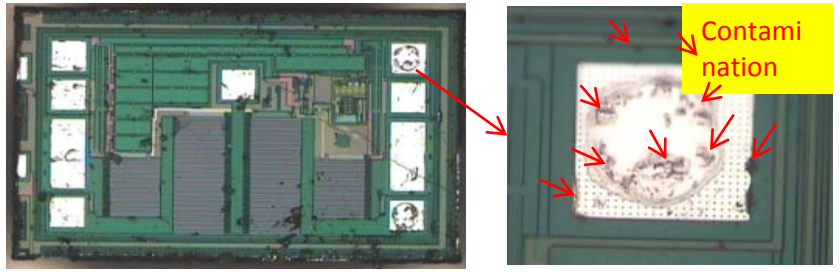
Pad Contamination

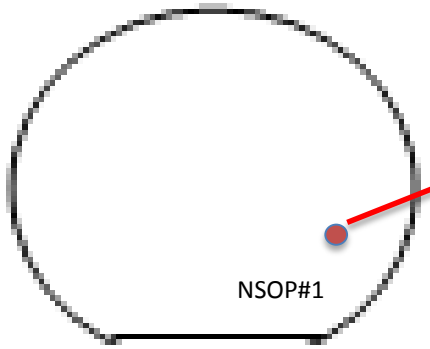
Process Optimization

- Categorize Defects
  - Wafer Fabs
  - Wafer Backend Process
  - Wire bond Assembly process
- Conduct process mapping
  - AOI @ Backend
  - Map Wafer to Lead frame
  - Optimize Process Windows-Min/Max Parameters
  - Package Commonality studies
  - Revised Acceptance Criteria
- Assign Corrective Action teams

Wire Bonding Assembly DoE







EDX Analysis: % Atomic

	Good Unit			
Unit#	O	Al	C	F
1	1.50	98.50	0	0
2	1.62	98.38	0	0
3	1.48	98.52	0	0
4	1.56	98.44	0	0
5	1.61	98.39	0	0
6	1.65	98.35	0	0
7	1.36	98.64	0	0
8	1.82	98.18	0	0

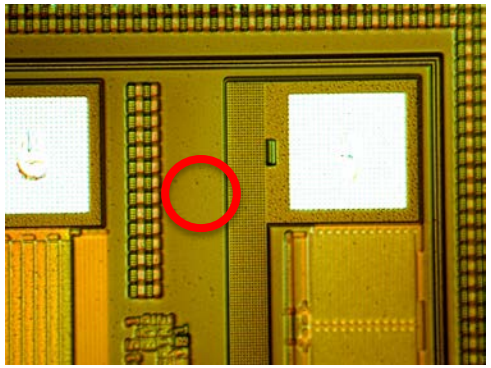
EDX Analysis – NSOP Unit

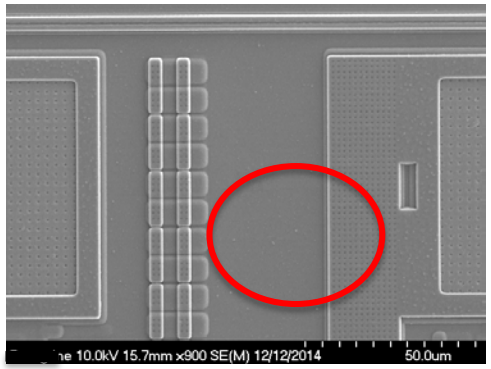
Unit#	Point	O	Al	C	F
1	1	9.27	81.55	9.18	0
	2	14.79	0	18.91	0
2	1	4.28	37.30	5.96	0
	2	3.00	93.32	2.21	1.47
3	1	1.79	94.72	2.39	1.10
	2	0	0	100	0
4	1	18.34	36.76	31.76	0
	2	13.00	14.51	43.74	0
5	1	7.59	36.60	7.71	0
	2	16.22	1.54	54.06	0

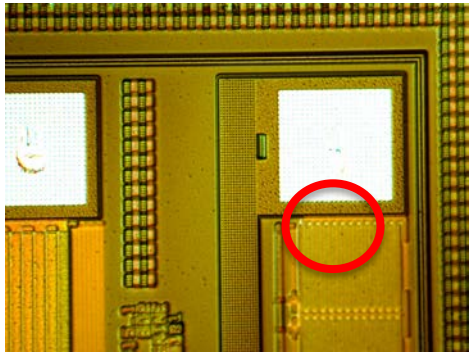
Actions:
Assigned to Wafer Fabs
Wafer Backend Controls
AOI Implementation

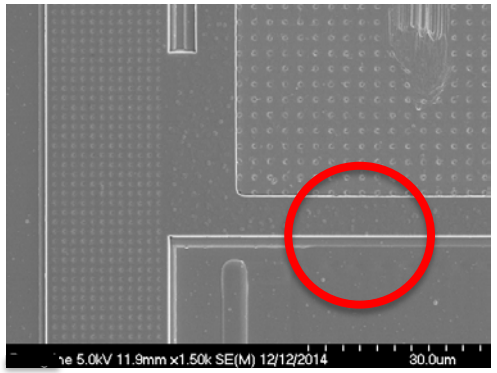
High % O and C element was found on contaminated pads and small amounts of F ,Na, Mg

Black Dots Analysis







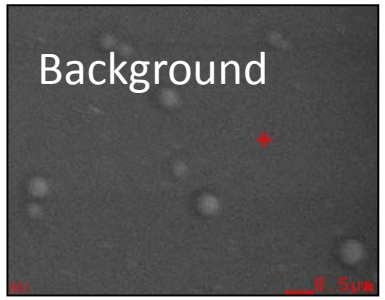


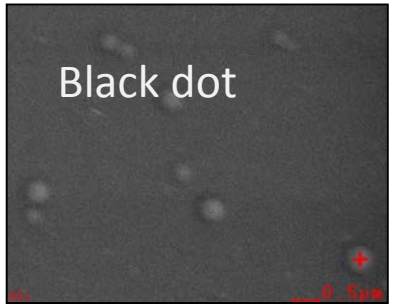
Element	Wt%	At%
CK	02.26	04.30
NK	19.07	31.17
OK	00.65	00.92
SiK	78.03	63.61
Matrix	Correction	ZAF

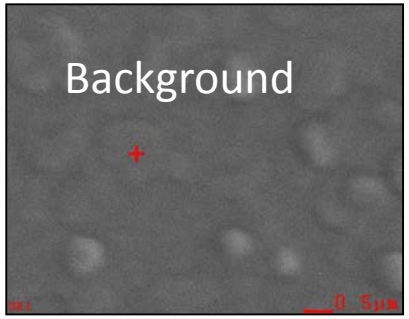
Element	Wt%	At%
CK	02.38	04.36
NK	23.59	37.15
OK	00.58	00.79
SiK	73.46	57.70
Matrix	Correction	ZAF

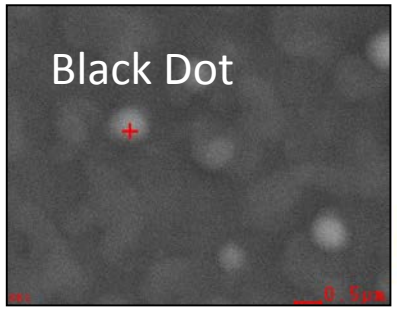
Element	Wt%	At%
CK	02.02	03.92
NK	18.73	31.20
OK	00.19	00.28
AlK	03.56	03.08
SiK	72.02	59.83
TiK	03.47	01.69
Matrix	Correction	ZAF

Element	Wt%	At%
CK	02.19	04.22
NK	19.17	31.65
OK	00.29	00.42
AlK	02.73	02.34
SiK	72.99	60.10
TiK	02.63	01.27
Matrix	Correction	ZAF

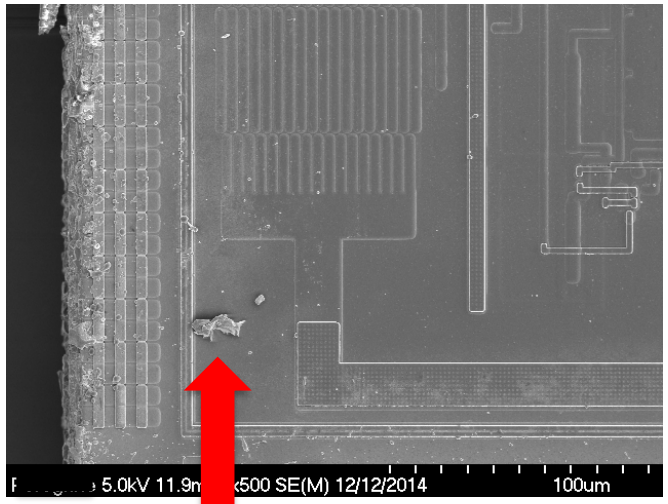




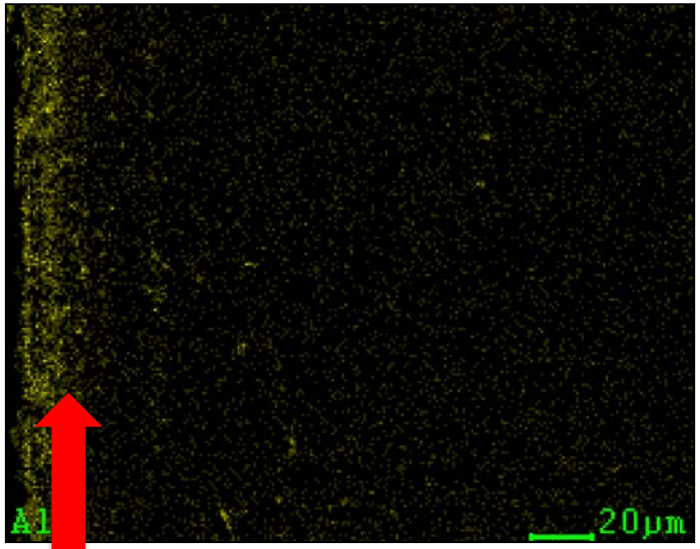




Surface Contamination

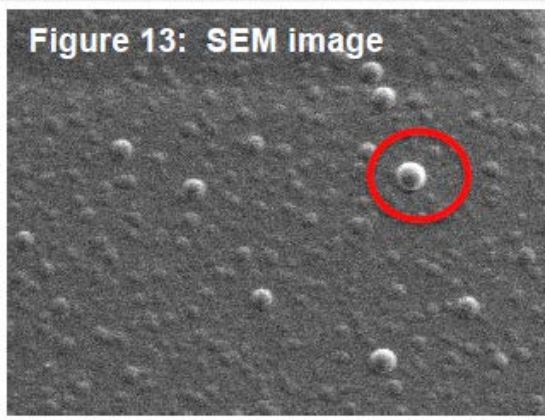


The SEM image 4 shows dirt and particles on the die surface. These are presumed to be from the laser scribe operation

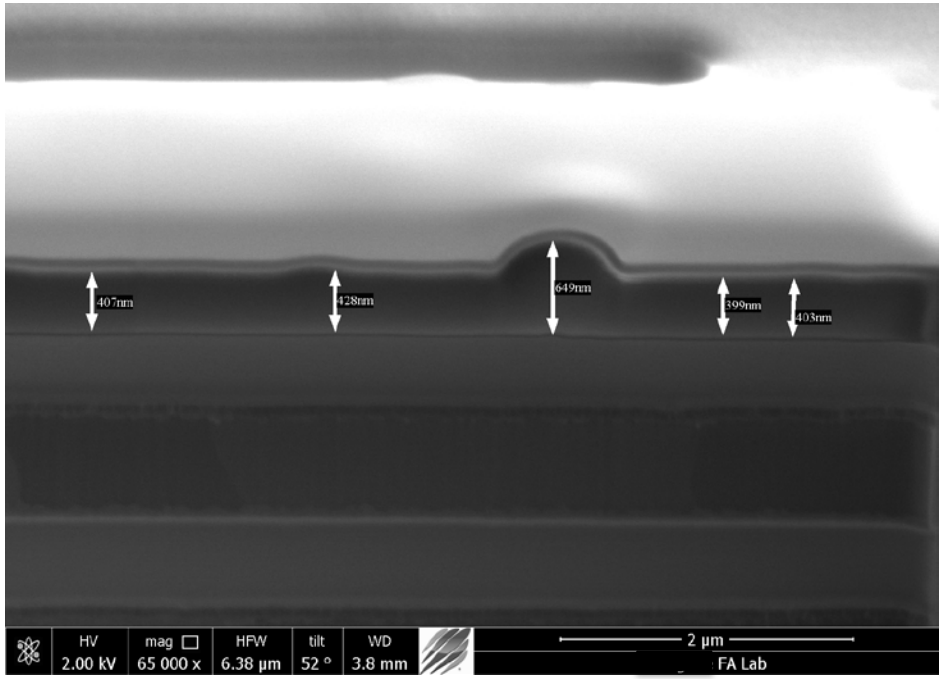


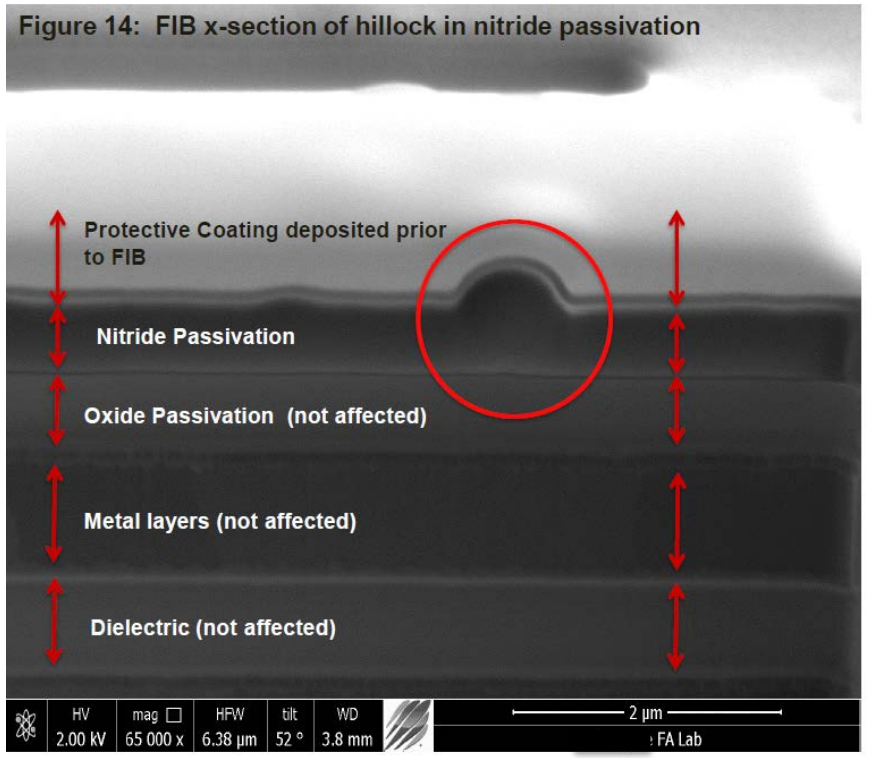
EDX dot map for aluminum. Concentrations of aluminum are indicated by the yellow contrast.

Hillocks on Passivation Layer

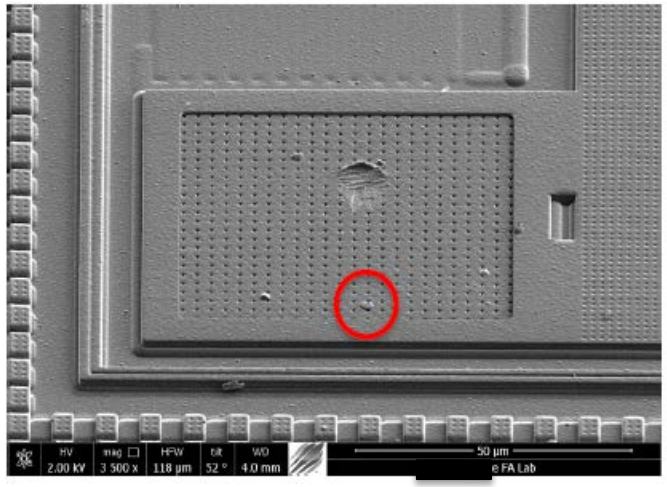


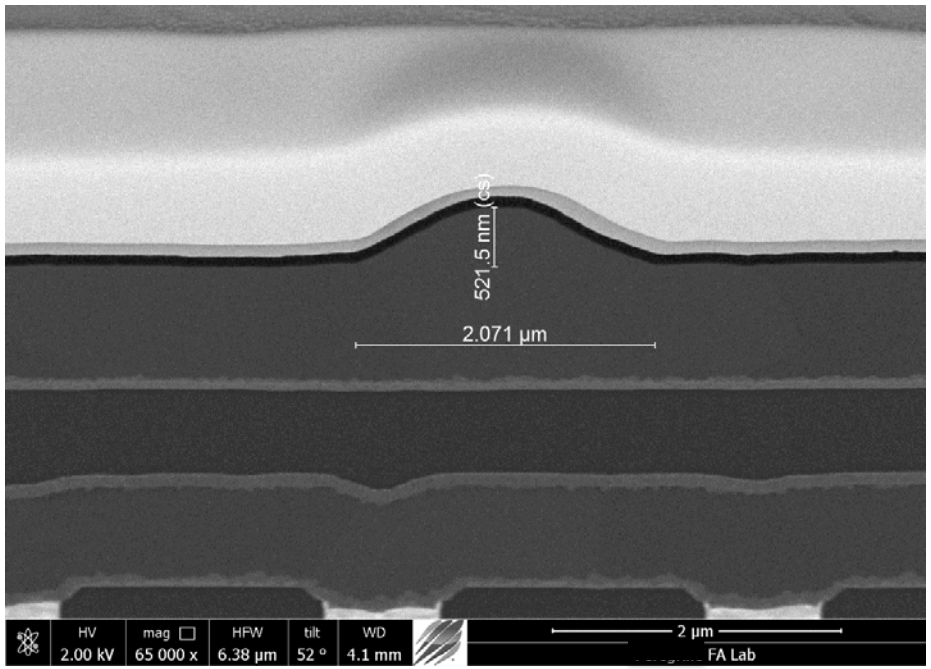
Hillocks Characterized
Aluminum Composition
Non- issue with wire bond
IQC Reject Criteria Revised

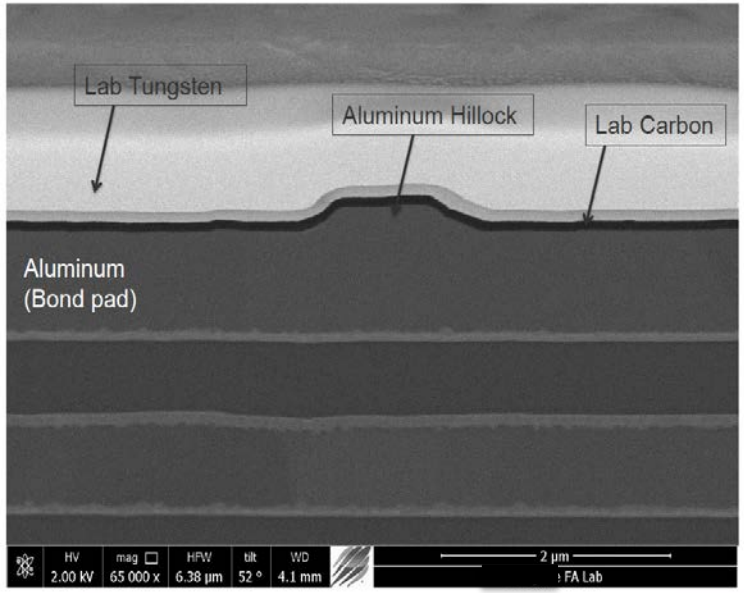


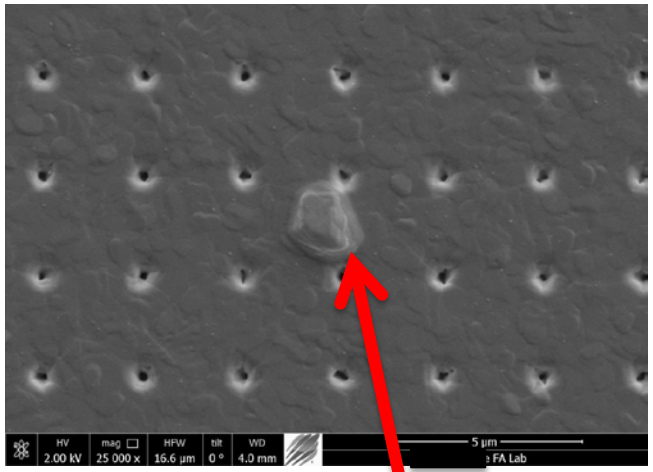


Bond Pad Hillocks









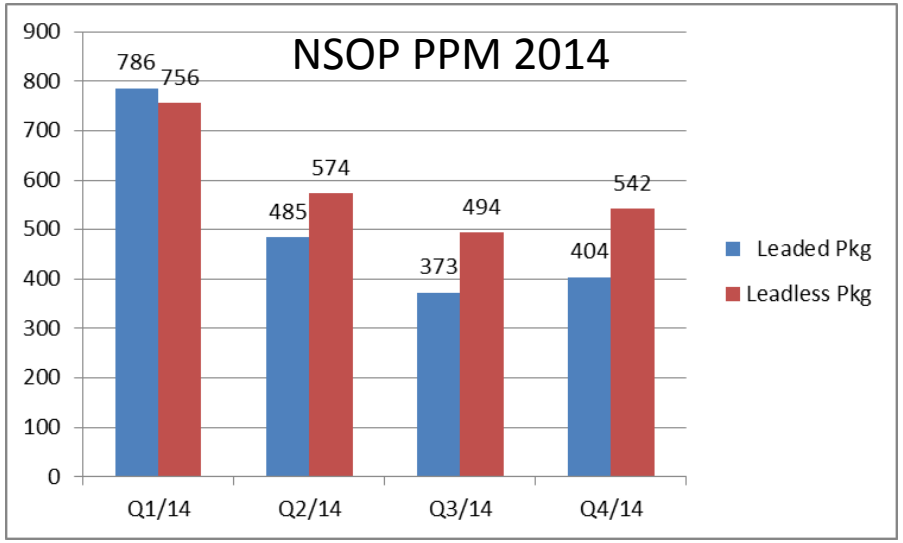
Hillock

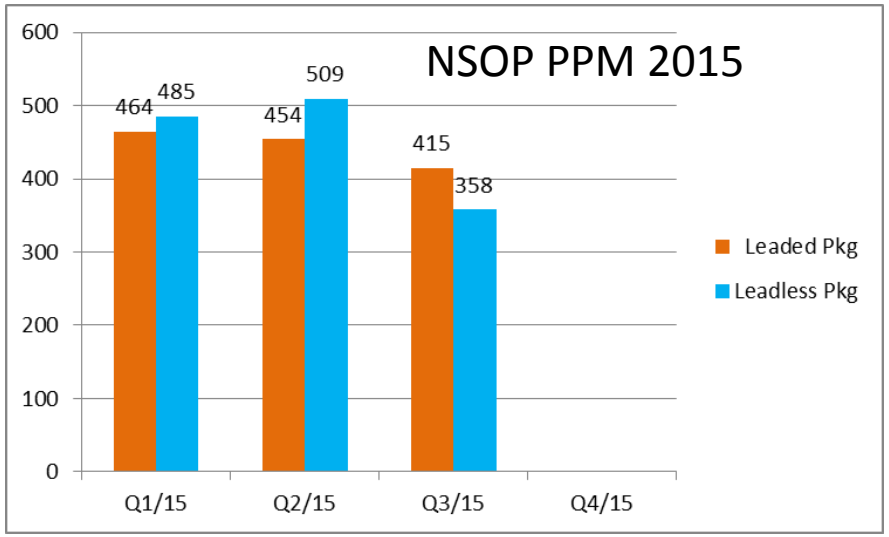
Bondability was not affected by hillocks on Bond pads.

Pre /Post AOI NSOP PPM

NSOP PPM 2014				
Product	**Q1/14**	**Q2/14**	**Q3/14**	**Q4/14**
Leaded Pkg	786	485	373	404
Leadless Pkg	756	574	494	542

NSOP PPM 2015				
Product	**Q1/15**	**Q2/15**	**Q3/15**	**Q4/15**
Leaded Pkg	464	454	415	
Leadless Pkg	485	509	358	





Conclusions

- Assembly yields can be improved by process optimization
- Process mapping and root cause analysis are essential steps.
- AOI is a valuable tool for Defect screening and mapping.
- Communication and teamwork leads to success

Acknowledgements

- The author wishes to acknowledge the support of the engineering teams in wafer fabs, backend processing, subcontract assembly, internal and external failure analysis labs and quality teams.