Optimizing BNC PCB Footprint Designs for Digital Video Equipment

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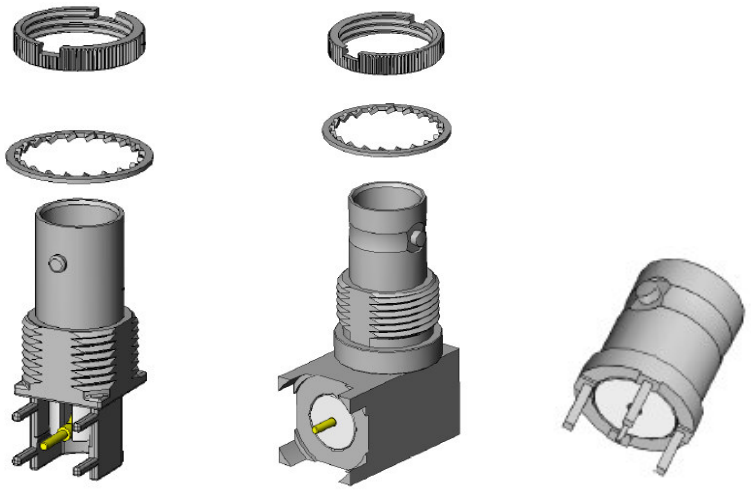
Introduction

An increasing number of video equipment is running at Gigabit rates today. They are interconnected through relatively large size coaxial BNC connectors. While these connectors are in general of good quality, their performance in the equipment depends on how they are mounted onto the printed circuit board. Use of non-optimized connector footprints introduce impedance mismatches, reflections, signal loss, and impair the signal fidelity of the equipment. The task of printed circuit board layout designs for BNC footprints falls into the hands of layout designers and hardware engineers who often do not have the time or tools to get it right. This article outlines a few common problems in BNC footprint designs, and illustrates examples of carefully designed footprints for edge-mount and through-hole connectors for use with National's LMH0384 3G/HD/SD adaptive cable equalizer, LMH0303 cable driver, and LMH0387 Configurable I/O devices.

BNC Types

Video equipment have historically used BNCs with 75Ω coaxial cables. Video pictures are used to transport at the standard definition rate (270Mb/s), upgraded to the high definition rate (1.485Gb/s), and are now migrating to 3Gbit/s. The BNC connectors must be capable of supporting 3Gbit/s signal transmission with minimum signal loss, while maintaining 75Ω characteristic impedances in order to minimize reflections.

Many connector vendors offer different types of BNCs, depending on how they are mounted onto the printed circuit board. With regard to mechanical considerations, they can be vertical mounted, right-angle mounted, or board-edge mounted. For electrical, the signal pins are either surface mounted to landing pads on the top side of the board, or soldered into plated-through holes with signal routings on the opposite side of the board. Figure 1 shows some examples of the through-hole BNCs. Figure 2 shows examples of edge-mounted BNCs with surface-mount signal pins and Figure 3 shows an example of a right-angle BNC with a surface-mount signal pin.



Source: Samtec True75™ right angle BNC BNC7T-RT-BN2 | Samtec True75™ right angle BNC BNC7T-RT-BN1 | Samtec Tru75™ straight BNC BNC7T-ST-TH1

Figure 1. Examples of Through-hole BNCs

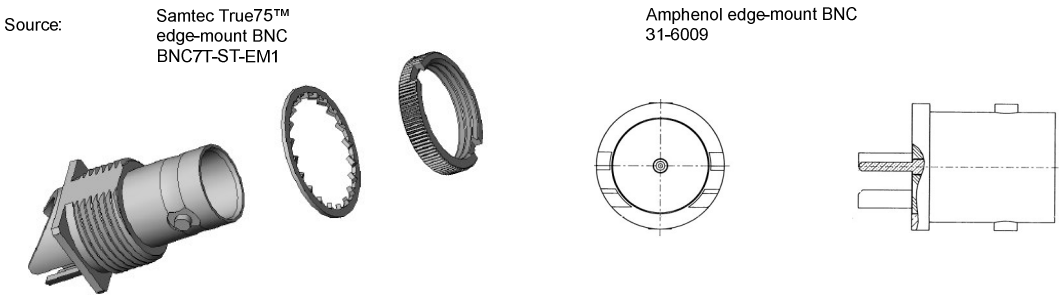


Figure 2. Examples of Edge-mount BNCs

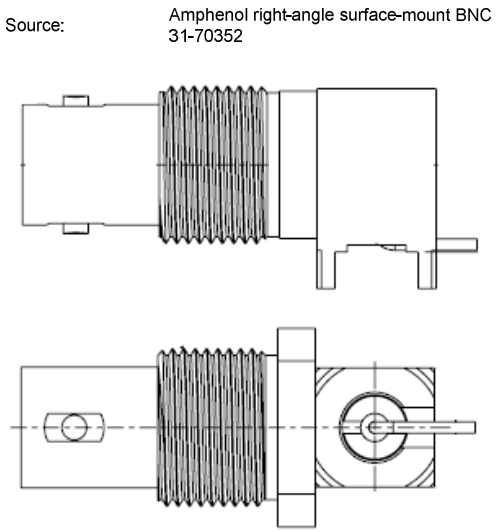


Figure 3. Example of a Surface-mount BNC

BNC Testing

BNC is a coaxial connector designed to support up to 3Gb/s video transmission. Its performance is primarily determined by the coaxial structure inside the BNC. The transition from the BNC connector to the printed circuit board will heavily influence the performance of the BNC. A well-designed BNC footprint is necessary to preserve the BNC's bandwidth and its characteristic impedance.

Time domain reflectometer (TDR) is a very good tool to quickly check out the intrinsic performance of the BNC's coaxial structure without its signal pin or its footprint. A simple way to do this measurement is to launch a TDR step into the BNC, with its signal pin shorted to its shield pins using a flat metal blade. By measuring the reflected signal from the launched TDR step, the instrument is able to derive the impedance over the time that the step travels.

Figure 4 illustrates the impedance profile of a good BNC. This right-angle BNC has a uniform coaxial structure with its 75Ω characteristic impedance practically constant inside the BNC. Its footprint should be designed to achieve the same characteristic impedance as the BNC.

Figure 5 shows the impedance profile of a fair BNC. This right-angle BNC shows sign of non-uniformity in its coaxial structure. At the right-angle bend, the characteristic impedance starts to decrease from the nominal 75Ω. In this case, its footprint can be designed to have slightly higher characteristic impedance in order to offset the imperfections from the BNC.

Figure 6 shows the impedance profile of a poor BNC. This right-angle BNC shows multiple signs of non-uniformity in its coaxial structure. At the right-angle bend, it has difficulty to maintain its characteristic impedance. In this case, it will be challenging to design a footprint with good return loss performance for this BNC.

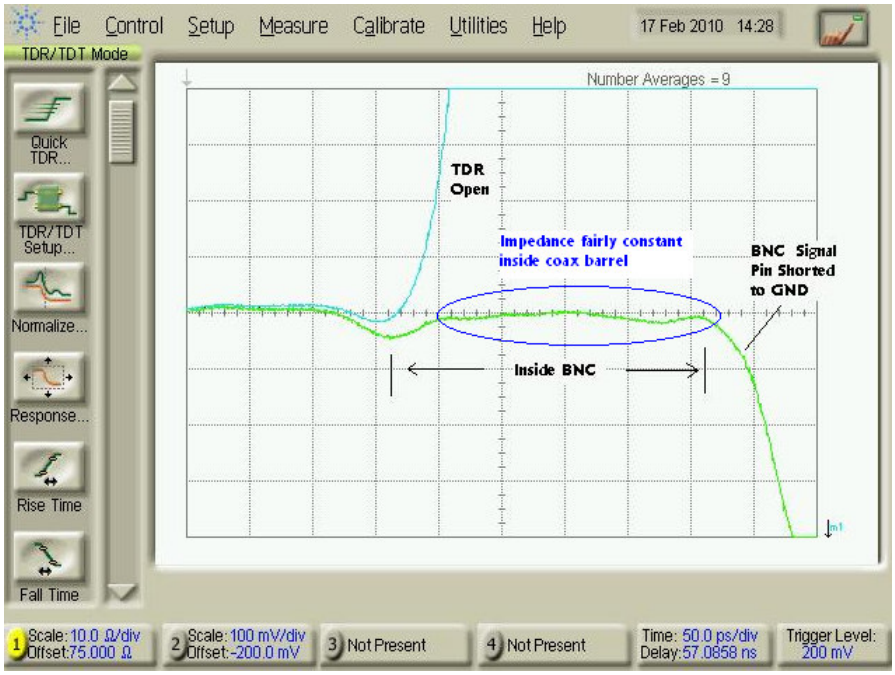


Figure 4. Impedance profile of a good BNC

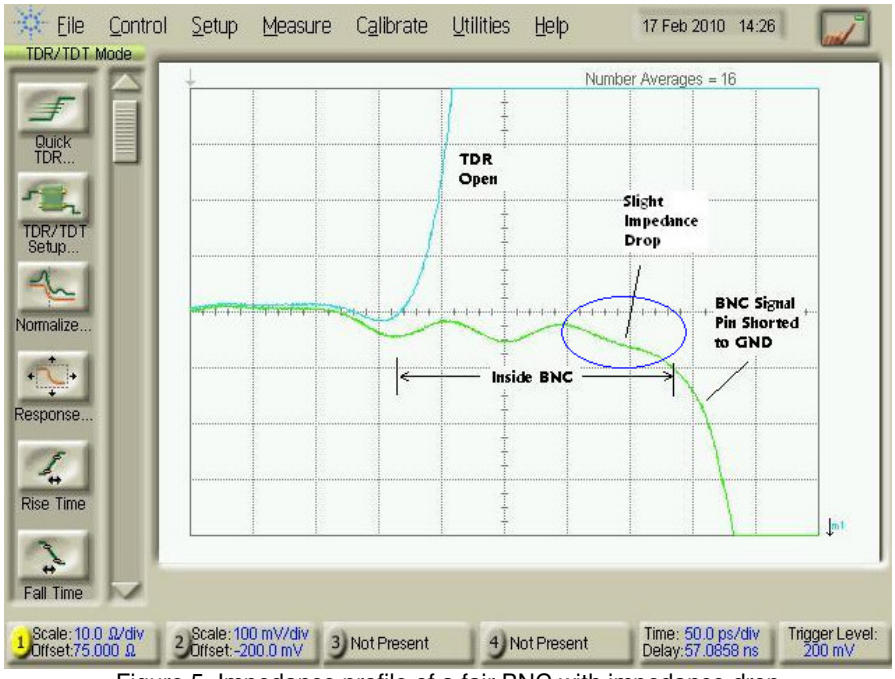


Figure 5. Impedance profile of a fair BNC with impedance drop

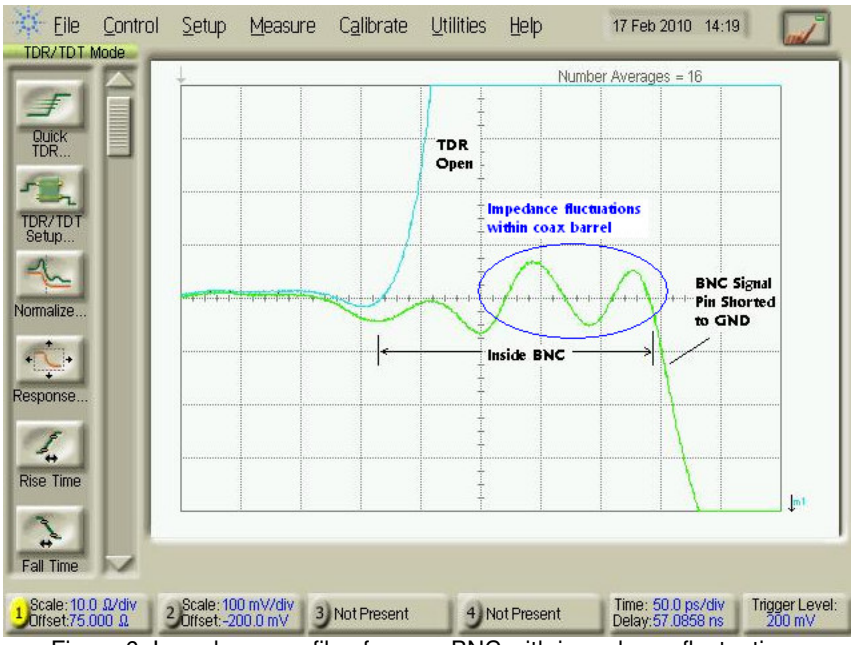


Figure 6. Impedance profile of a poor BNC with impedance fluctuations

Common Problems in BNC-to-Board Transition

Most surface-mount BNC connectors have large signal pins of about 30-40 mils diameter. Landing pads of about 50-mil width are necessary for soldering the signal pins properly onto the printed circuit board. For ease of routing, thinner surface traces of 8-15 mil widths are commonly used to route signals from the BNC connectors to high pin-count integrated circuits.

Figure 7 shows the top and cross-sectional views of a non-optimized edge-mount BNC footprint. A 12-mil width microstrip, placed at 15-mil above its GND plane, is designed to achieve the 75Ω characteristic impedance. The BNC's landing pad is effectively a 50-mil wide microstrip. With a GND plane 15mil below the pad, the characteristic impedance of the pad is significantly lower than that of the trace. The pad introduces a large impedance drop that will impact the signal quality and add parasitic capacitance that reduces the BNC's bandwidth.

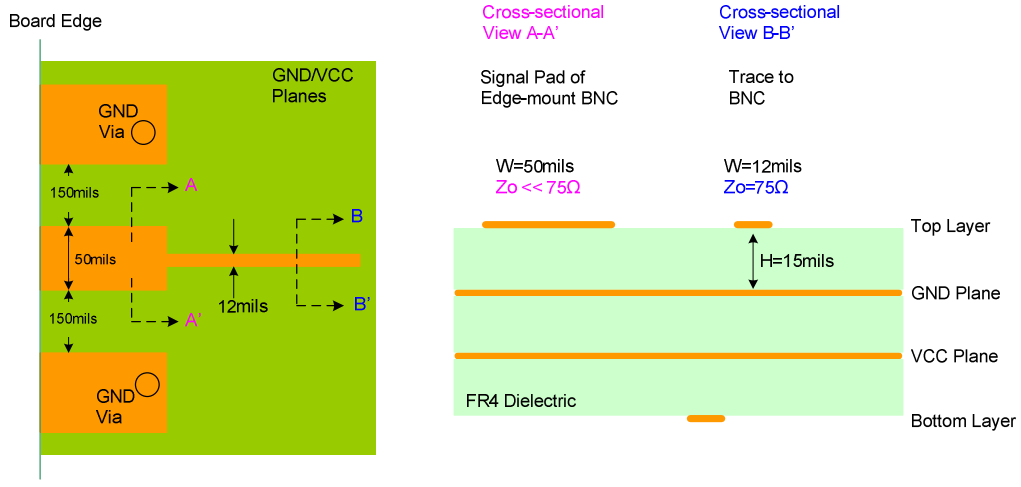


Figure 7. Top and cross-sectional diagrams of a non-optimized edge-mount BNC footprint

Many types of video equipment typically use through-hole BNCs because of the better mounting robustness. The BNCs are usually mounted on the top side of the board, with their signal pins soldered into fairly large plated-through holes, and signal routing is done on the bottom side of the

board. Figure 8 shows the top and cross-sectional views of a non-optimized through-hole BNC footprint. The inner ground and power layers are isolated from the plated-through hole to avoid shorting the signal pin. The cylindrical barrel of the plated-through-hole introduces a small amount of inductance. Each inner power plane introduces parasitic capacitance to the plated-through hole, the amount of which depends on the clearance distance from the barrel. A large plated-through hole with a small clearance exhibits excessive capacitance that results in a large impedance drop. If the signal is routed on the same side of the BNC, the plated-through-hole becomes a stub hanging on the signal trace and presents a large parasitic capacitance and even larger impedance drop.

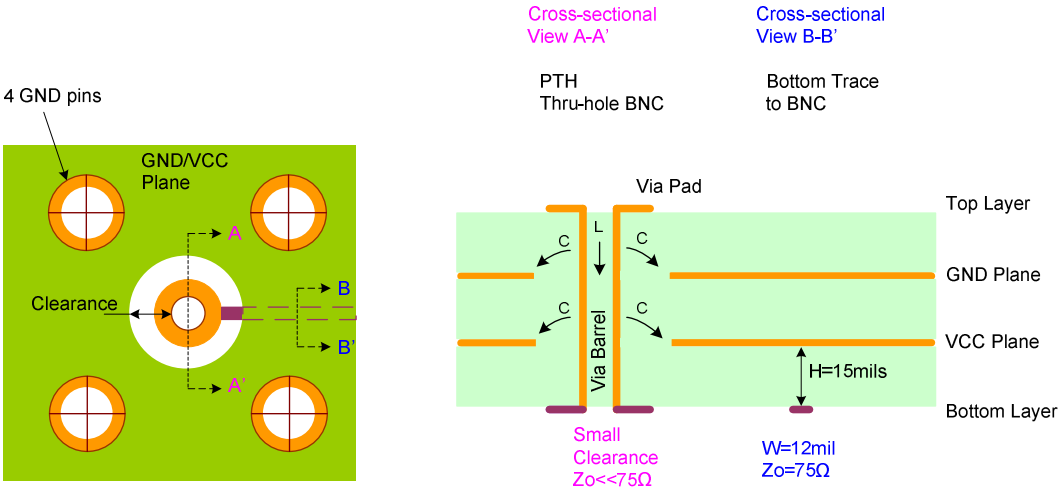


Figure 8. Top and cross-sectional diagrams of a through-hole BNC footprint

Effect of Non-Optimized Signal Launch

The Society of Motion Pictures and Television Engineers (SMPTE) publishes standards[1] that govern the transport of digital video over coaxial cables. The SMPTE standards include input and output return loss requirements, which basically specify how well the input or output port resembles a 75Ω network. Figure 9 shows the SMPTE requirements on return loss specifications. A poor BNC or a non-optimized BNC footprint introduces impedance mismatches and makes it challenging to pass the SMPTE return loss limits.

Severe impedance mismatches cause reflections that will adversely affect the signal quality and reduce the voltage or timing margin of the data eye. Excessive parasitic capacitance at the signal launch reduces the bandwidth of the signal path, and introduces inter-symbol interference jitter. Figure 10 illustrates an example of a signal waveform degraded by a non-optimized signal launch.

Figure 9. SMPTE return loss requirements for video ports

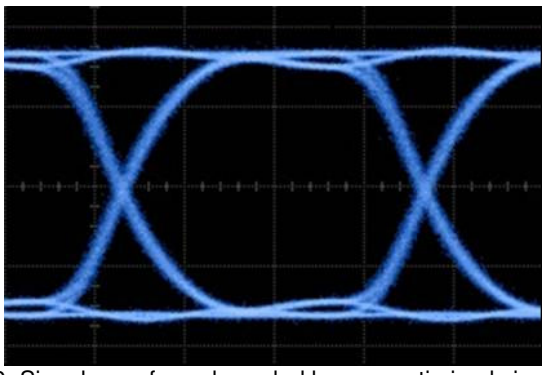


Figure 10. Signal waveform degraded by non-optimized signal launch

BNC Selections

The choice of BNCs is primarily determined by their mechanical construction and compatibility to the equipment's enclosure. On the electrical front, the BNCs are expected to support up to 3Gbit/s transmission with little insertion loss. They are also expected to maintain uniformity and a fairly constant characteristic impedance in their coaxial structure. They preferably have small signal pins, such that the smallest possible through-hole or landing pads can be used in the footprint designs with the goal of minimizing impedance discontinuity.

Transparent BNC Footprints – Surface-mount BNCs

A transparent footprint is one that has identical characteristic impedance as the BNC connector, and does not significantly add circuit parasitic that impacts the BNC's bandwidth. Several techniques are explored here. One effective method is to walk through the signal path, look for board geometry that deviates from the target impedance, and devise means to restore the impedance back to the target value.

In the case of the surface mount BNC shown in Figure 7, the large landing pad creates a huge impedance drop. Raising its impedance requires the use of larger dielectric separation (H>>15mils), which is not an option. One way to raise the pad's impedance is to shave off the excessive parasitic

capacitance by using relief in one or more power plane layers under the pad. The size of the relief opening is designed to provide just enough fringing capacitance to restore the landing pad's impedance to its target. Figure 11 illustrates this technique of using plane relief under the pad. The footprint is dependent on the location of the first GND plane, and the location as well as the number of power planes used in the board.

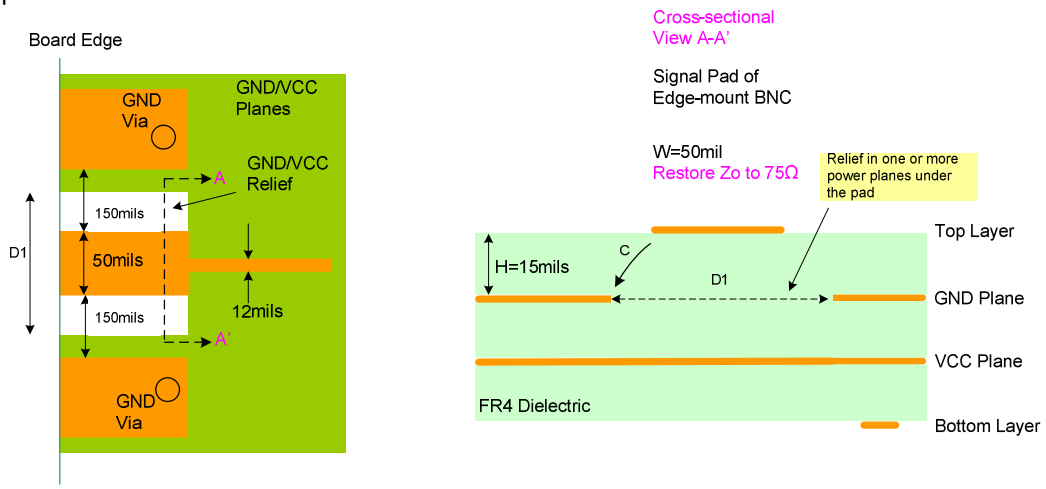


Figure 11. Use of Plane Relief for Surface-mount BNC footprint

Figure 12 shows an example of an improved footprint. In this example, a larger GND/VCC relief is used on all the power planes under the pad. This step raises the characteristic impedance of the pad well above 75Ω (the target impedance for this example). To bring the impedance back to the target 75Ω, strips of ground metal are added on both sides of the pad. The ground strips are placed at a pre-determined distance from the pad, such that they introduce just enough ground coupling to achieve the desired impedance[2]. This structure has the advantage of being fairly independent from different board stack-ups, and can be re-used in multiple board designs.

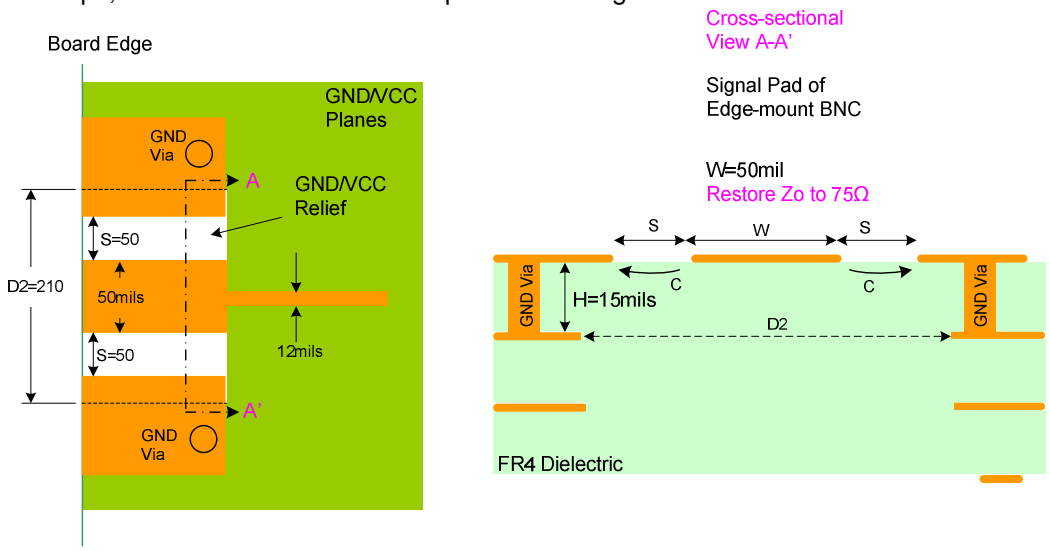


Figure 12. Use of GND relief and GND guards for a surface mount BNC footprint

Transparent BNC Footprints – Through-hole BNCs

For a through-hole BNC, its footprint is made up of two structures – the plated-through-hole, and its exit trace. The plated-through hole is typically 30-50 mils in diameter. Large clearance (anti-pad) in the power planes is necessary to maintain the impedance of the plated-through hole to 75Ω. The size of the anti-pad is determined by the diameter of the plated-through hole as well as the number of the power planes in the board. With a large anti-pad, the exit trace within the anti-pad region loses its GND reference and its impedance increases. To overcome this problem, a short strip of metal is

extended into the anti-pad for preserving the exit trace's impedance. The metal strip extension is needed for the first power plane above the bottom exit trace, and its width is typically 3-5 times the trace's width. Figure 13 illustrates the BNC footprint with this technique. Another commonly used technique is to widen the exit trace within the anti-pad region to lower the exit trace's impedance. Figure 14 illustrates the BNC footprint implemented with this technique.

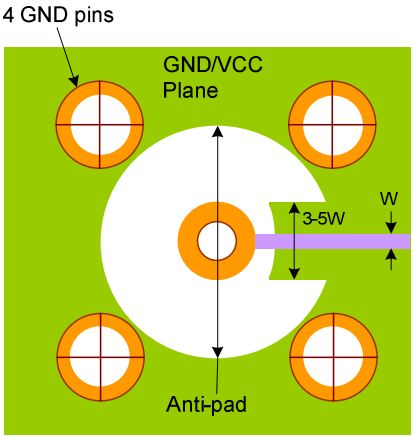


Figure 13. Use of GND strip above exit trace for through-hole BNC footprint

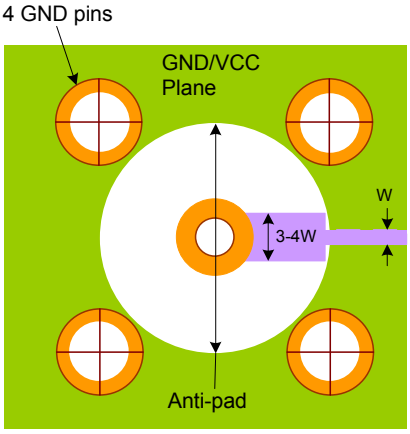


Figure 14. Use of wider exit trace for through-hole BNC footprint

Figure 15 illustrates an improved footprint. In this example, two GND strips are placed at either side of the widened exit trace on the bottom metal layer. The ground strips are placed at a pre-determined distance from the exit trace, such that they introduce just enough ground coupling to achieve the desired impedance for the short exit trace. This structure has the advantage of allowing independent adjustments of the anti-pad in the power planes for controlling the impedance of the plated-through-hole, and the gap of the ground guards to control the impedance of the exit trace.

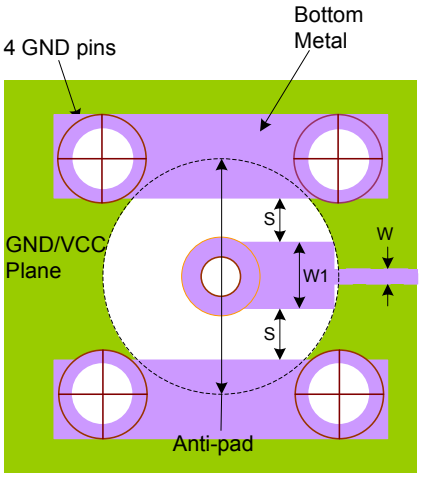


Figure 15. Use of GND guards to exit trace for through-hole BNC footprint

BNC Footprint Optimization

BNC footprint designs involve placement of anti-pads, or relief in the GND and VCC inner layers, or placement of surface GND strips to introduce just enough parasitic capacitance for maintaining the desirable characteristic impedance. The footprint is dependent on the signal pin diameter of the BNC, as well as the number of power plane layers in the board. In some cases, the footprint is designed to deviate from the nominal 75Ω in order to compensate for a small imperfection in the BNC itself. Hardware engineers have to optimize BNC footprints based on past experience and in many cases, multiple board re-spins are common.

BNC footprint design is best optimized with the use of 3-dimensional electromagnetic simulations. Starting with the BNC's 3-dimensional model (mechanical dimensions and material properties), the proposed footprint structure, and the board's properties (trace width, stack-up and material properties) are entered into the 3-D EM simulator[3]. Frequency domain simulations are performed to ensure compliance to design goals on return loss and insertion loss. Simulated TDR can also be done to examine the impedance profile of the BNC and the footprint.

BNC vendors, with the complete knowledge of the BNC's model, are best in running such simulations with the customers' input on board stack-up. The simulation example shown in this section is courtesy of Samtec, a connector supplier.

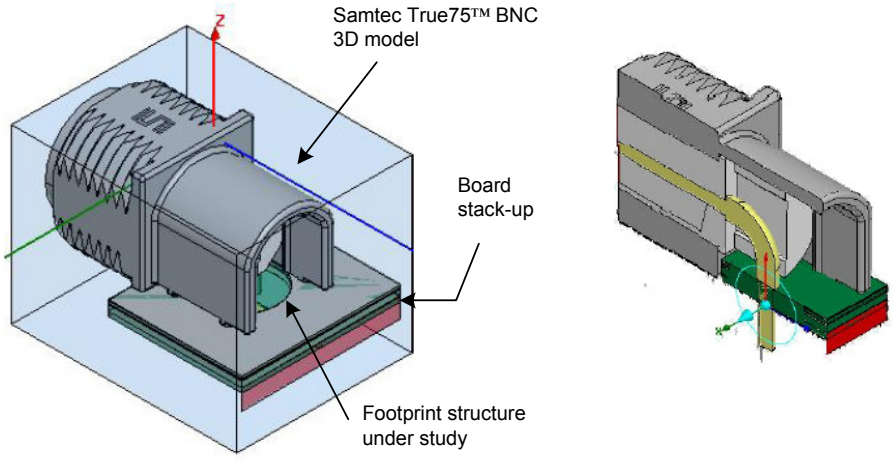


Figure 16. 3-D model of Samtec's right-angle BNC and its footprint on a PCB

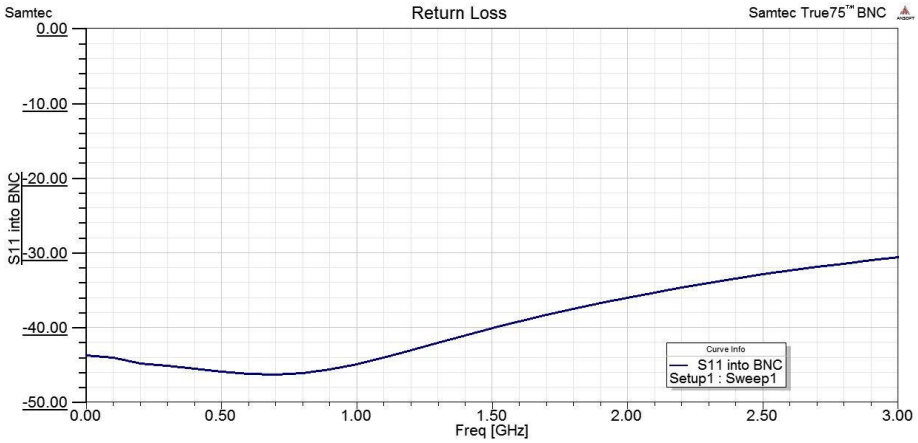


Figure 17. Simulated return loss of BNC and its footprint

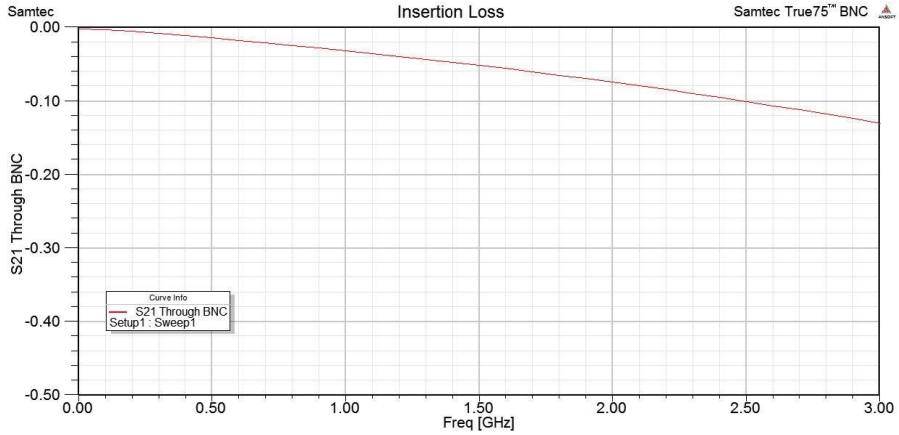


Figure 18. Simulated insertion loss of BNC and its footprint

Testing the BNCs with National's LMH0387

Now, the BNC footprints are optimized with the 3-D EM simulator. Several BNC types and their optimized footprints are implemented onto the LMH0387 evaluation boards for validating their system performance.

The LMH0387 is the industry's first single-chip adaptive cable equalizer and cable driver that enables one BNC to be shared as an input port or an output port. It has a built-in termination and return loss network to compensate the capacitance from the integrated circuit and simplifies high speed board layout for meeting SMPTE return loss with good margin.

Figure 19 illustrates the simplified circuit of the evaluation board. The LMH0387 is connected to the BNC through an AC coupling capacitor (4.7µF). To achieve good return loss, the LMH0387 is placed close to the BNC port, and connected to the BNC with a 75Ω trace. Ground relief technique is also used for the large landing pads of the 4.7µF AC coupling capacitor to minimize impedance discontinuity.

TDR impedance measurements and return loss measurements are performed at the BNC port. Figure 20 shows the photographs of two evaluation boards mounted with straight and right angle through-hole BNCs. Their impedance profiles measured with a TDR are shown in Figure 21. Figure 22 shows their return loss plots demonstrating 5-10 dB margin from the SMPTE limits.
Figures 23-25 are another set of measurement plots for edge-mount and surface-mount BNCs.

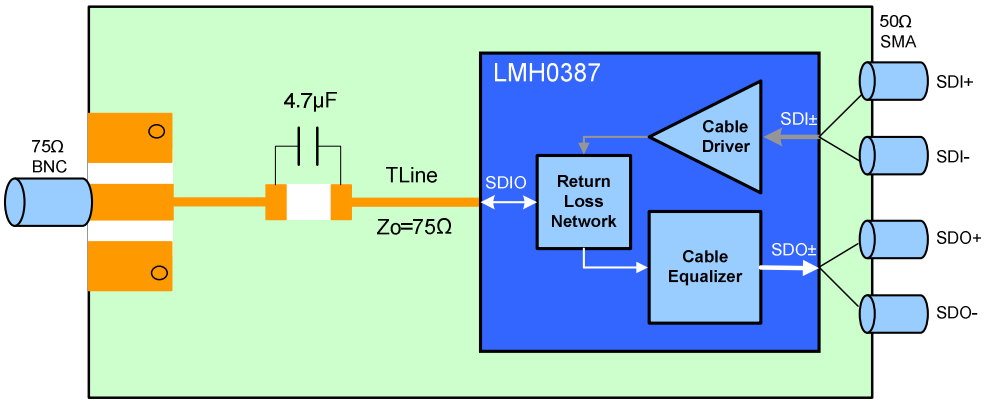


Figure 19. Simplified schematic for the LMH0387 Configurable IO

Performance Plots with the LMH0387 Configurable IO

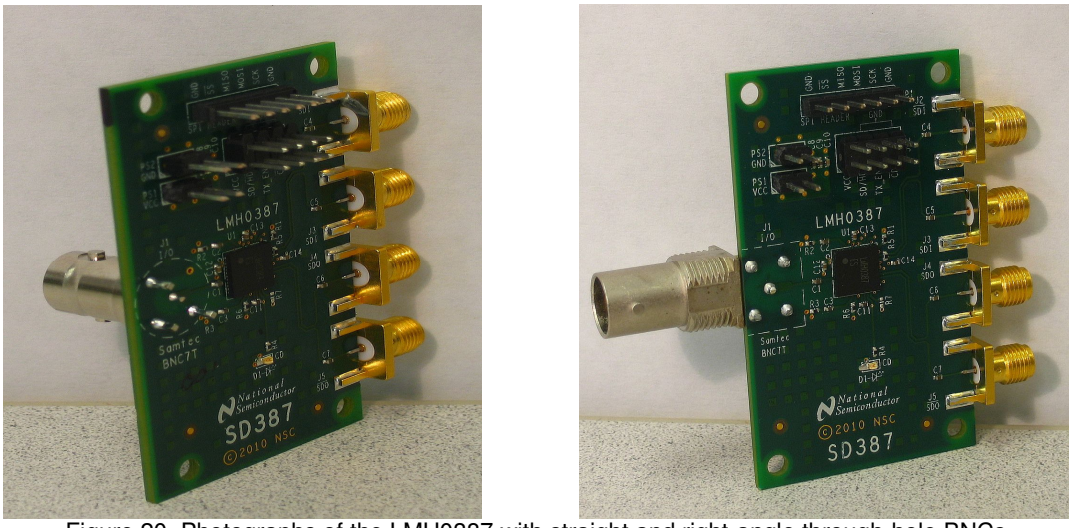


Figure 20. Photographs of the LMH0387 with straight and right-angle through-hole BNCs

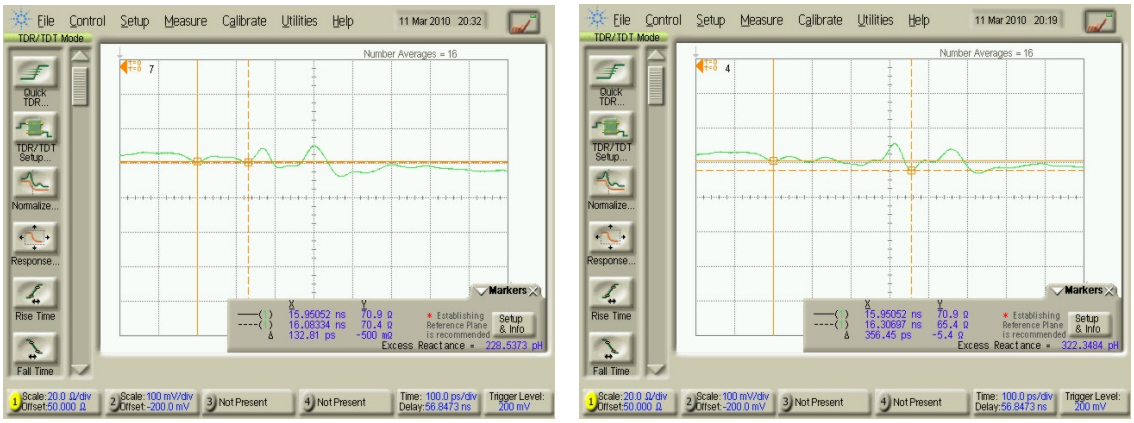


Figure 21. Impedance profiles of BNCs, footprints and traces to the LMH0387

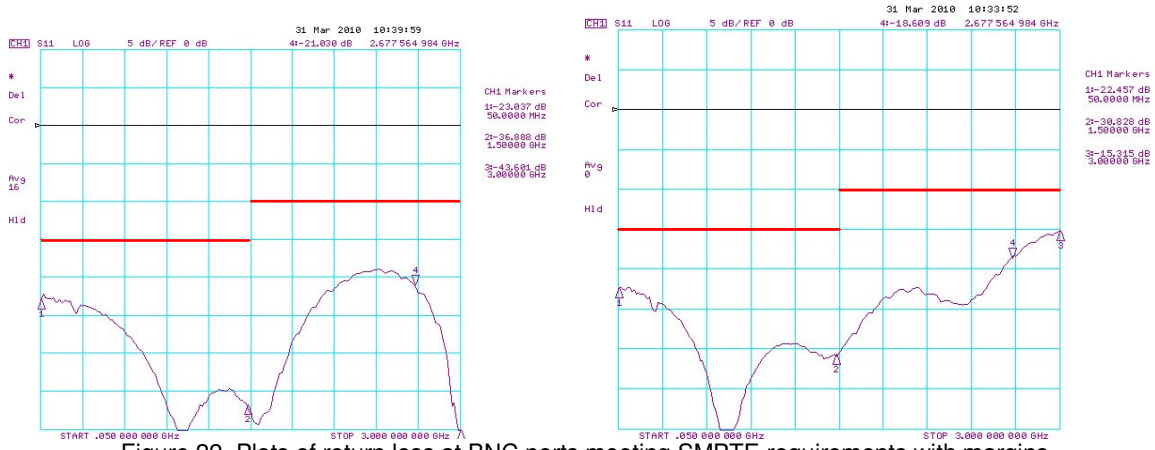


Figure 22. Plots of return loss at BNC ports meeting SMPTE requirements with margins

Performance Plots with the LMH0387 (cont'd)

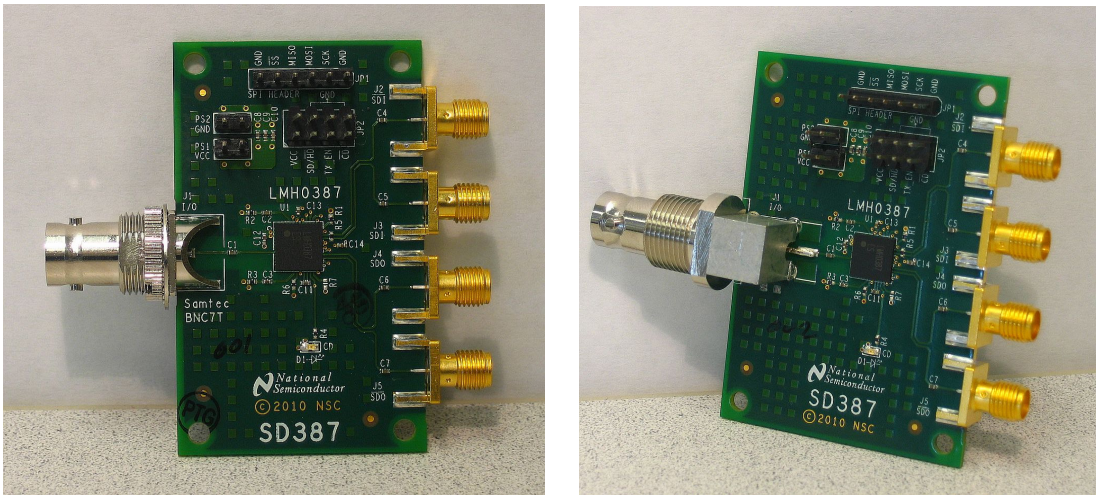


Figure 23. Photographs of the LMH0387 with edge-mount and right-angle surface-mount BNCs

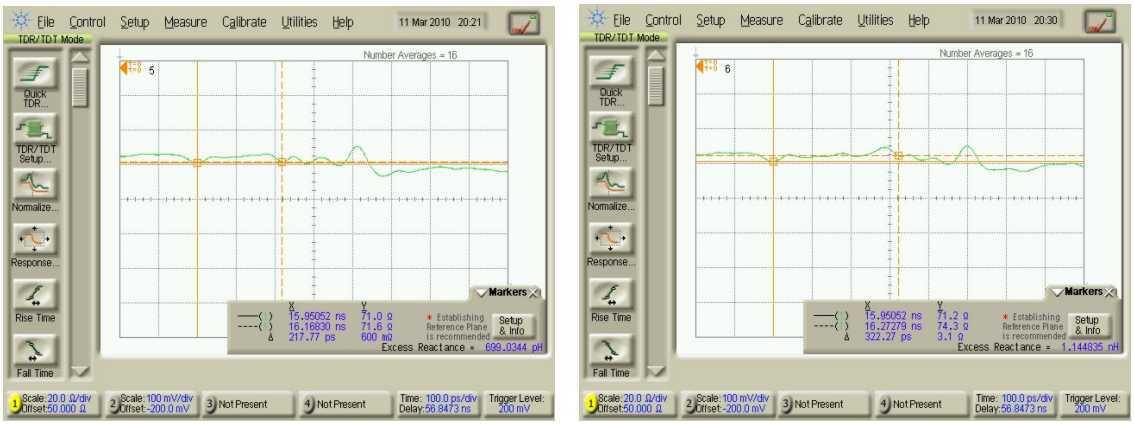


Figure 24. Impedance profiles of BNCs, footprints and traces to the LMH0387

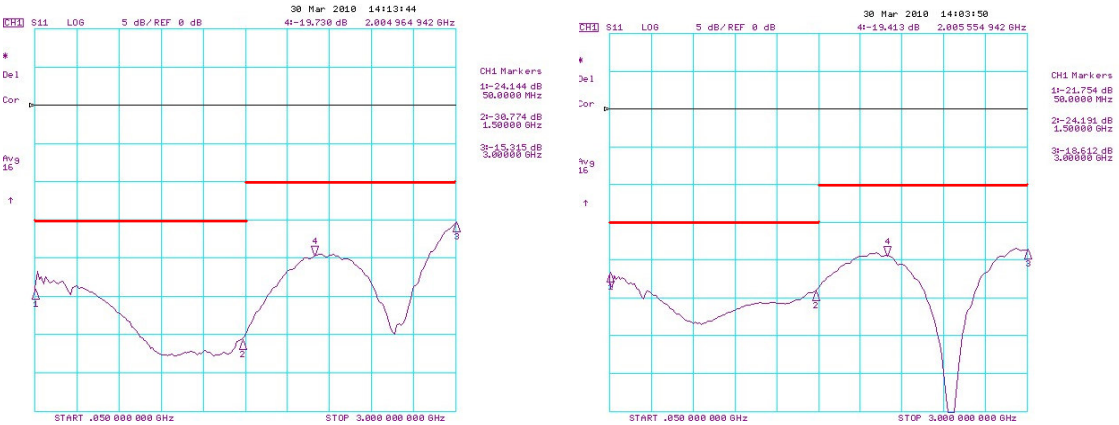


Figure 25. Plots of return loss at BNC ports meeting SMPTE requirements with margins

Conclusion

In this article, several common problems in BNC footprints are discussed, and several design techniques for transparent footprint designs are presented. The best design is the use of connectors with the smallest signal pin, so there is no need to design any special board structures. For connectors with larger signal pins, whether it is an edge-mount or a through-hole type, it is possible to design a controlled impedance footprint with good performance. Always use the smallest pad or smallest hole possible. Walk along the signal path, examine the board structure one by one, look for the parasitic inductance and capacitance along the path, and find ways to shave off the excess and bring the impedance to the target value.

While the principles used in this article apply to footprint designs, they are also valid for other component landing pads as well. High-speed board designs have gone beyond connectivity from point A to point B. There are many subtle layout decisions that have consequences in the electrical performance. Three dimensional electromagnetic simulation tools aid engineers in making the important layout decisions and achieving the target electrical behavior. The time domain reflectometer is a useful instrument for board debugging and identifying where the impedance changes occur. Good signal launch is a starting point to achieve good signal quality and meet return loss requirements along with other circuitry on the board.

Acknowledgement

The author would like to acknowledge the collaboration work with Travis Ellis of Samtec for running 3-D simulations to optimize the footprints for the Samtec True75™ BNCs used in the LMH0387 evaluation boards.

Reference

1. The Society of Motion Pictures and Television Engineers publishes many SMPTE standards on the serial digital video interface. Some of these standards are:
   - SMPTE 259M-2006: SDTV Digital Signal/Data – Serial Digital Interface
   - SMPTE 292M-1998: Bit Serial Digital Interface for High Definition Television Systems
   - SMPTE 424M-2006: 3Gb/s Signal/Data Serial Interface
2. United States Patent 6765298: “Substrate pads with reduced impedance mismatch and methods to fabricate substrate pads”
3. Some 3-D electromagnetic simulators: Ansoft HFSS, Agilent EMDS/ADS
4. Datasheets of LMH0384, LMH0303, LMH0387 and many other SDI devices can be found at www.national.com/sdi/
5. True75™ is a trade-mark of Samtec. Information on Samtec True75™ BNCs can be found in Samtec website: www.samtec.com/rfcable/Standard_RF_PCB_Components.aspx.