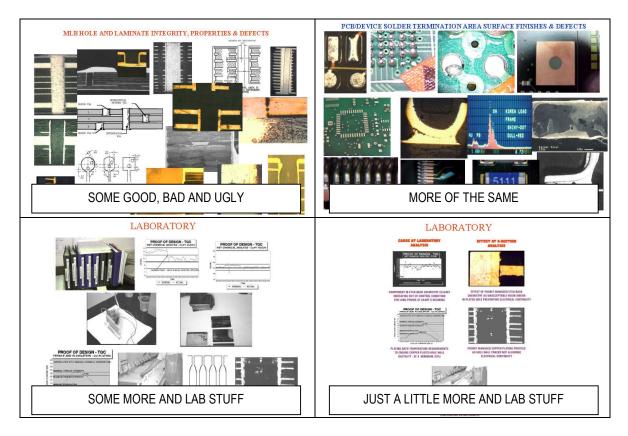
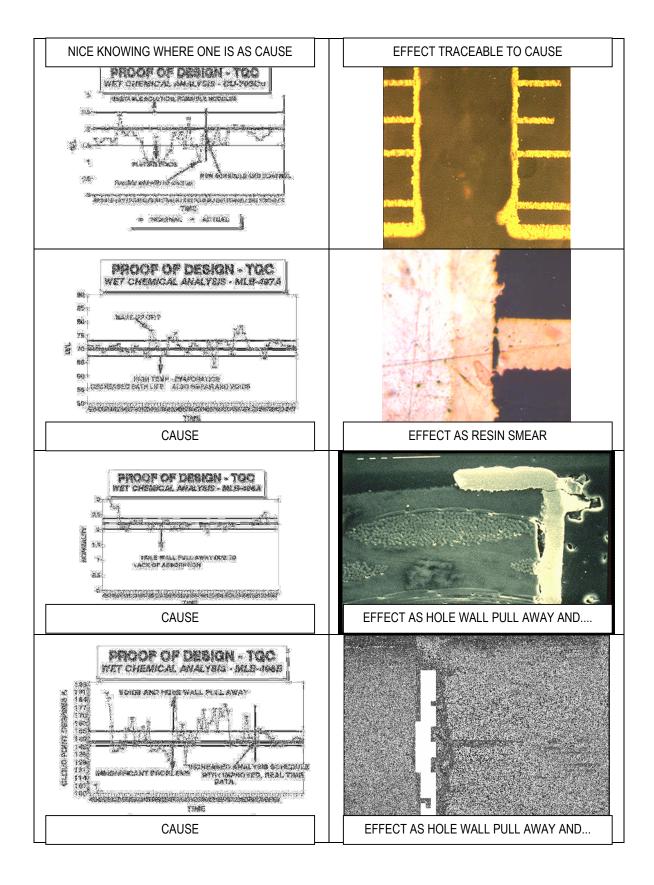
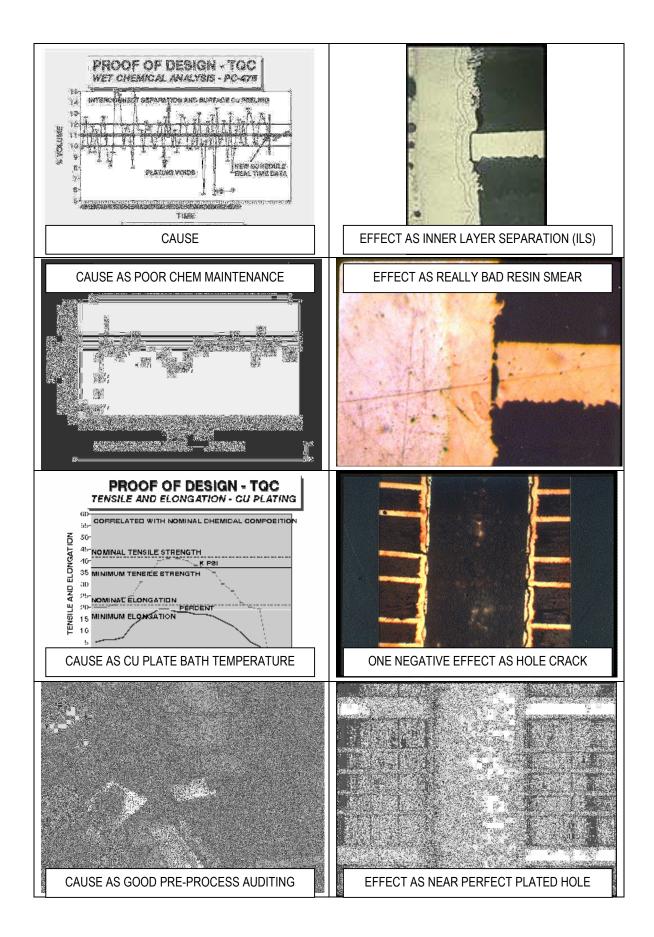
11.3.2 Printed Circuit Board Failure Analysis

As with all other F/A processes, PCB's occasionally need a little help from them. The following, just as the component process in Section previous, has been condensed from so many involvements over the past 35 years, I cannot remember - nor should I because they all could have been prevented with DFM/CE. However, the information presented, coupled with good DFM/CE and PCB process management provides an insight to the beast.

NOTE: FAILURE MODE AND EFFECT ANALYSIS (FMEA) IS THE TERM USED NOW TO BEST DESCRIBE AND DERIVE CAUSE AND EFFECT RELATIONSHIPS. IN THE WET CHEMICAL ANALYSIS PROCEDURES IN 11.3.1 (BEGINNING ON PAGE 210), IT IS MADE CLEAR HOW PCB CHEMISTRIES MUST BE ANALYZED, PRE-PROCESS AUDITED, CONTINUALLY MONITORED, AND EFFECTIVELY MANAGED TO ENSURE FAILURES ARE NOT FOUND. HOWEVER, IF A PROCESS GOES OUT OF CONTROL, SOME OF THE FOLLOWING INFORMATION IS USEFUL TO FIND ROOT CAUSE, CORRECT IT, AND PREVENT IT FROM RECURRING SO NO DEFECT IS FOUND AGAIN. THE FOLLOWING IMAGES PROVIDE CAUSE AND EFFECT RELATIONSHIPS WITH CAUSE ON THE LEFT AND EFFECT ON THE RIGHT. HOPEFULLY, THEY PROVIDE MOSTLY GRAPHIC/VISUAL INFORMATION WITH NEED OF FEW WORDS.



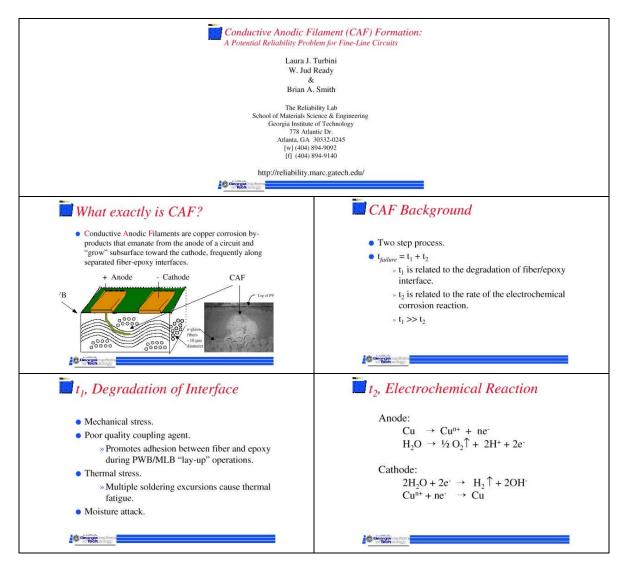


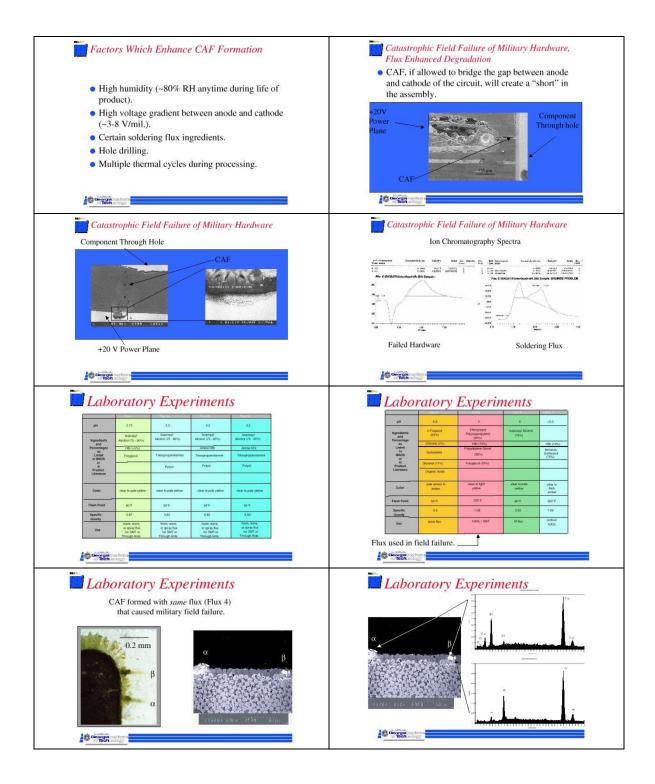


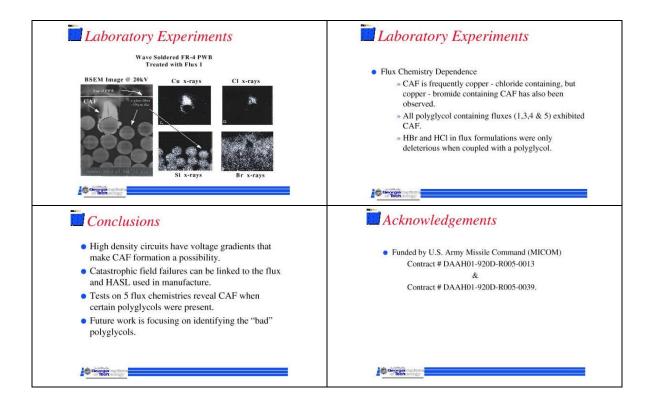
NOTE: THERE IS SO MUCH MORE TO TALK ABOUT HERE. HOWEVER, THE GOOD THING IS PCB FAILURE ANALYSIS IS STRAIGHT FORWARD. THAT IS, IT IS FAIRLY EASY TO DETERMINE CAUSE AND EFFECT RELATIONSHIPS FROM CHEMISTRY AND MATERIAL PROCESS MANAGEMENT THROUGH ALL PROCESSES FOLLOWING. THIS MEANS CORELATION BETWEEN FINDINGS, AS DEFECT, AND CAUSE ALWAYS CAN BE MADE.

IT'S CAF (CONDUCTIVE ANODIC FILAMENT) TIME

This brief but important series of images is provided courtesy of the folks at the Georgia Institute of Technology, at the time they were there (first image below). This brief provides a detailed insight into conductive anodic filament issues though saying little about its prevention even though the answers are there but must be uncovered. For that, see the MoonMan's information in Table II and his presentation on multilayer PCB requirements. In this information are found details that prevent most CAF occurrences from a multilayer construction perspective - especially using more resin rich materials. As far as certain flux chemistries go, that is another matter of vital interest.

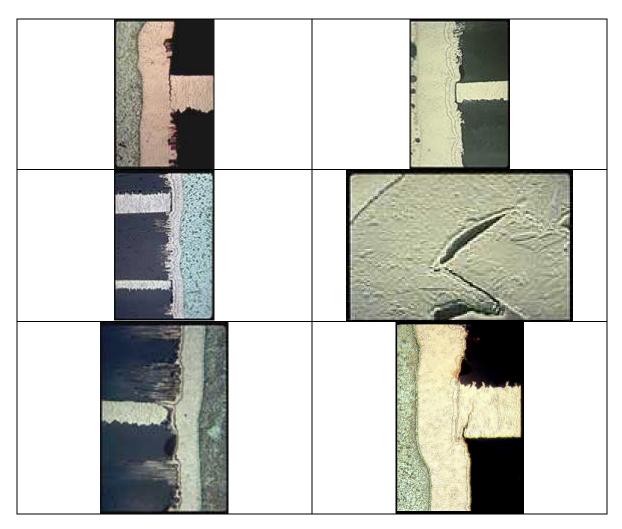






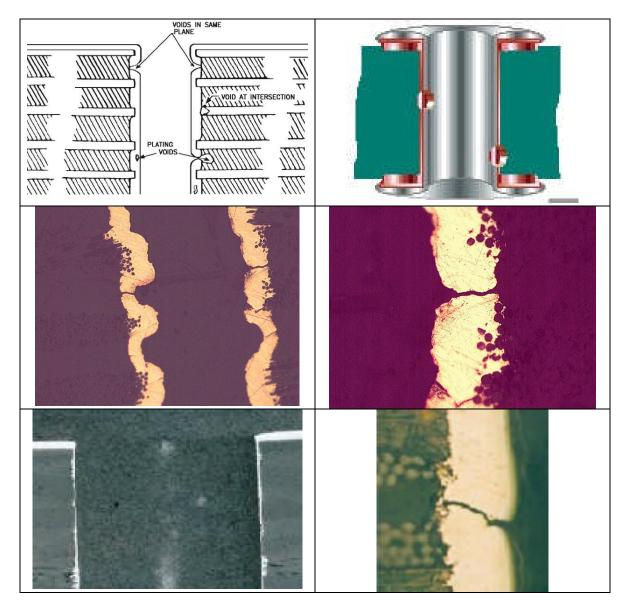
IT'S ILS (INNER LAYER SEPARATION) TIME

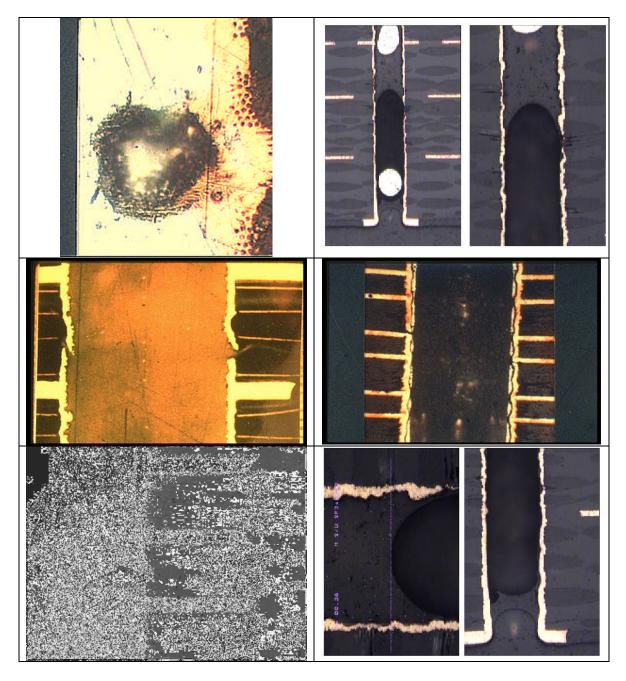
Inner layer separation images are in the following. ILS is easily prevented as indicated in the foregoing information concerning plating and other MLB required chemistries. There is no need to see any of this.



SOME PLATING VOIDS, IF YOU PLEASE

Again, managing plating chemistries prevent plating void occurrences as in the following. Read MoonMan's presentation on printed circuit basics as in the laboratory analytical, maintenance, and prevention section herein to ensure these little beauties do not come into your lives and wreak havoc. Remember what constitutes plating voids as in the first image, in MIL-P-55110, and the second in IPC - 600.





IMPORTANT NOTE: CORELATION OF EFFECT (DEFECT) FINDINGS ARE EASILY MADE DIRECTLY TO INITIAL LABORATORY ANALYSIS, IN 11.3.1 STARTING ON PAGE 210, AND TO EFFECTIVE, OR NOT, PROCESS, INSTEAD OF RESULTS, MANAGEMENT.