Micro Vias in Board Station

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This paper reviews the possible implementations of the Micro Via Technology within the Mentor Graphic's Board Station environment, specifically within the Librarian, Layout and Fablink applications. In this context, the definition of a Micro Via is constrained to Board Station's support of such technology and contains only generalized descriptions of the manufacturing processes that require Micro Vias.

Current Via Capabilities

Unknown to most users, Board Station, internally, has only one definition of a via (it has only one via structure in its database). The base definition being that:

- A via can have one or more layer connection rules (via rule)
- A via can have one plated/filled hole size, or no hole at all, which is drilled through each layer appearing within each defined via rule. If no hole, the connection is assumed between two layers, as specified by the via rule, via an external device.
- A via can have a different shape on each defined physical layer of the board.

Board Station, however, categorizes vias in order to simplify use by the user. Thus, Board Station currently supports the following categories of end-user via types:

- Thru-Via
  Has a hole and one system defined via rule starting at the top metal layer and ending at the bottom metal layer of the physical layer stackup, metal layers being layers of type Signal or Plane.
- Buried-Via
  Has a hole with multiple user defined via rules. The same hole size is propagated through all layers contained within each via rule.
- Two-Layer Via
  Has no hole, therefore connection is assumed to be made by an external device in contact with the two pads defined by a via rule. Via rules are limited to adjacent layer pairs.

Basic Micro Via Design

The definition of a Micro Via in Board Station is dependant on the context in which a via is used. Let's first dispense of the possible use of a two-layer via because it is not used in the normal routing of a Micro Via design.

Now let's look at a generic Micro Via design stackup. Routing on two or more layers of a physical layer stackup is generally limited to the use of smaller vias, narrower traces, and narrower spacing requirements. For this review, let’s refer to these layers as “micro” layers even though some manufacturers call them cover, transition or redistribution layers. In general, these *micro* layers are used to transfer Surface Mount Pin, BGA Pin or Bond Pad net connections down to an inner layer where the resultant spacing between connections (now vias instead of pins) are increased for routing. These *micro* layers may be composed of materials more accommodating to the small vias, narrow trace widths and spacing, but, is not a given. It’s also important to note that these micro layers are not necessarily the top or middle or bottom group of a physical layer stackup, nor is it limited to a single-sided board design (components may be mounted on both sides).

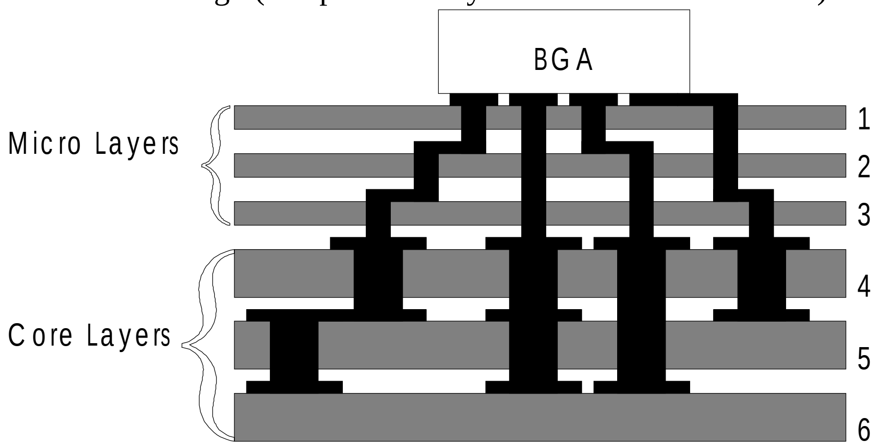

Figure 1. Basic Micro Via Layer Structure

Appearing above or below this *micro* group is another group of layers that require larger size
vias, holes, wider traces and probably wider spacing requirements. Let’s call these “core” layers. These *core* layers are generally used to minimize board cost by using the more common PCB materials and constraints.

In order to better understand the requirements Micro Vias impose on Board Station, we’ll examine a design from a “routing” point of view first, followed by the manufacturing output requirements.

Routing the Basic Micro Via Design

The following reviews the steps necessary to “route” this design in Board Station using two types of vias:

<u>Using Thru-Vias</u>

- Define thru-vias, each with all the required pad/shape size per *micro* & *core* layers.
- Allocate usage of these vias through net type rules.
- Assign trace width and spacing requirements through the net type layer rules – essentially defining different rules per layer.

<u>Using Buried-Vias</u>

- Define buried-vias, each with all the required pad/shape size per *micro* & *core* layers.

- In this example, we will allow use of each via from any layer of the design by defining a via rule for each layer pair of the physical layer stackup. Therefore, in a 6-layer design, we would define 5 via rules for each via to allow each to span from layers 1-2, 2-3, 3-4, 4-5, 5-6. Of course, this is not always the case one will encounter. Another common case would be to define layer pair rules that would enhance disbursement on the *micro* layers and lower the cost on the *core* layers even more. For example, if layers 1-3 are the micro layers and layers 4-6 are the core layers, each vias rule set may contain 1-2, 2-3, 3-4, and finally a 4-6 rule, emulating a thru-via through the *core* layers (4 via rules per via).
  NOTE: By setting the interactive routing via to one of these vias or by net type specification, the user can interactively route between layer pairs without ever having to manually change the interactive route via setting.
- Allocate usage of these vias through net type rules.
- Assign trace width and spacing requirements through the net type layer rules – essentially defining different rules per layer.

Thus far, routing is fairly basic and currently supported by Board Station automatically or interactively.

Obtaining the Required Manufacturing Output - The Problem

Now, for the really hard part – obtaining the required manufacturing outputs specifically the NC Drill data.

<u>Using Thru-Vias</u>

- In Fablink, we normally output Artwork & NCDrill data. Fablink will currently generate two NCDrill data files. One containing all the plated thru-hole drill data and another for the non-plated thru-hole data.

The problem here is that Micro Vias will require one hole size through the *micro* layers and a different, usually larger hole size for the *core* layers. Currently, vias can only be defined with one hole size in Board Station, therefore, the plated thru-hole data file output by the NCDrill generator is unusable. The locations are correct but the drill bit calls are wrong for either the *micro* layers or the *core* layers. The fix for this problem depends on the technology used to produce the *micro* layers. The following two sections will review two manufacturing processes that Board Station can address.

Dielectric Micro Thru-Via Layers….

If the micro layers are manufactured using dielectric material to separate each micro layer as well as the *micro* layer from the *core* layer, then the fix is not only simple but a required step in preparing the design for Micro Vias. Dielectric material is more common to the hybrid and mcm worlds and are used to separate metal layers (signal & power). Working from the bottom layer up in these types of designs, dielectric material is applied over the metal (pads, vias, fills & traces) which have been deposited on a base substrate or a previously applied dielectric layer. The methods vary but in one way or another, via holes that appear in the dielectric sheet pattern are cleared, leaving unobstructed holes to the metal layer beneath it. Applying metal on top of this sheet of dielectric material will fill the holes in the dielectric, thereby promoting the via connections up a layer to another via, pad, trace or fill.

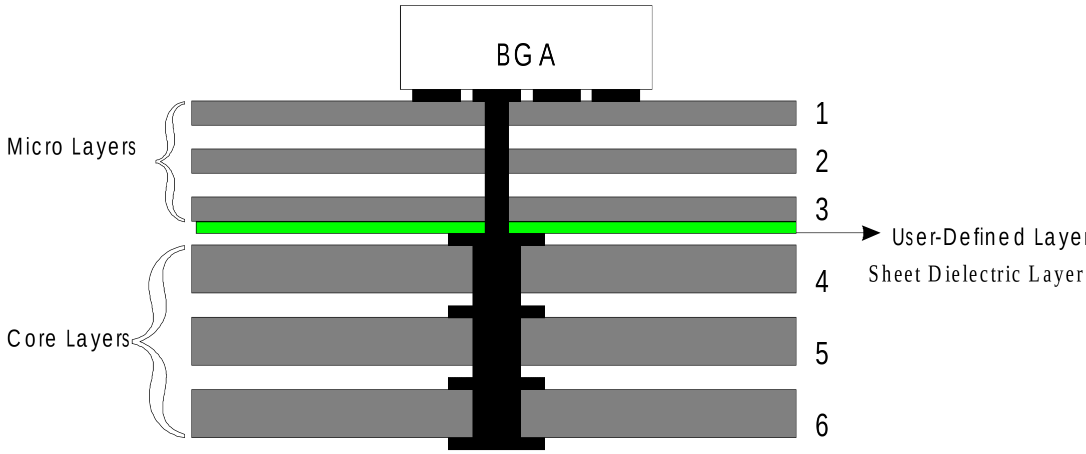

Figure 2. User-defined (Sheet_Dielectric) layers for Thru-Vias

In our Micro Via design, the *core* layer next to a *micro* layer would be the substrate referred to above. Thus, by

- inserting a user-defined layer between the *micro* layer & the adjacent *core* layer,
- and defining the proper size & shape hole for this layer in the via geometry,
- and specifying the *core* layer drill size for the via hole size

the manufacturing output can be obtained by both the artwork generator and the NCDrill generator. The artwork for the dielectric layer is photoplotted as a negative and is used to create the appropriate manufacturing mask for the layer. The NCDrill data will now be correct for the *core* layers since it will not be used for drilling the *micro* layers.

NOTE: The user-defined layer should be the same as that defined by the sheet_dielectric layer type appearing in the hybrids layer file (/idea/pkgs/pcb_base/data/hybrid_layer_file).

Drill Data required for both Micro and Core Thru-Via layers…

In this scenario, the solution defined above under "*Dielectric Micro Thru-Via Layers*" should be used but the dielectric artwork cannot be used directly as previously mentioned. Instead, the dielectric layer is used only to capture the hole sizes and locations of the thru vias from the *micro* layers. An AWK script, c utility or ample must be used to convert an ASCII Gerber output of the dielectric layer to an ASCII NCDrill data file. If a binary NCDrill data file is required, simply read the converted ascii data file using the "Drill->Open Drill Data" command, open the resulting geometry and execute "File->Save->Drill Data" command, specifying the binary option.

<u>Using Buried-Vias</u>

- In Fablink, we normally output Artwork & NCDrill data. As mentioned previously, Fablink will generate two NCDrill data files. One containing all the plated thru-hole drill information and another for the non-plated thru-hole information. In addition, it will output additional files for each via rule actually used in the design. Given this example, if all rules mentioned above (1-2, 2-3, 3-4, 4-5, 5-6) were actually used in routing, Fablink will generate an additional 5 drill files, one for each rule. If the rules were instead 1-2, 2-3, 3-4, 4-6 then the output would consist of only 4 additional files. Unfortunately, the current state of the NCDrill Generator requires the user to manually merge a drill "rule" file with the thru-hole drill file in order to produce one drill data file for a layer pair. This procedure must also be followed when overlapping rules exist. For example, a via might have a rule 1-5, and another might have a rule 2-5, and yet another via may have a rule 1-6. The resultant NCDrill files generated by the "Create Drill Data" command would be drill_1_5, drill_2_5 and drill_1_6. In order to produce the NCDrill file for layer pair 4-5, the user would have to carefully merge all three files. Appending the files is easy; sorting sequence is a little tougher.

This is not necessary if the use of multiple NCDrill data files to drill a layer pair is sufficient. This is due to the use of buried-vias in general and has nothing to do with Micro Vias. The buried via was originally introduced into Board Station to support MCM and Hybrid designs. Board Station's output for this technology (in most cases) is GDSII Stream Format Data, which is then used by a Pattern Generator to output the required manufacturing masks. The negative Gerber of the sheet dielectric layers could also be used. Hence, there was no requirement for NCDrill of Buried vias.

Dielectric Micro Buried-Via Layers….

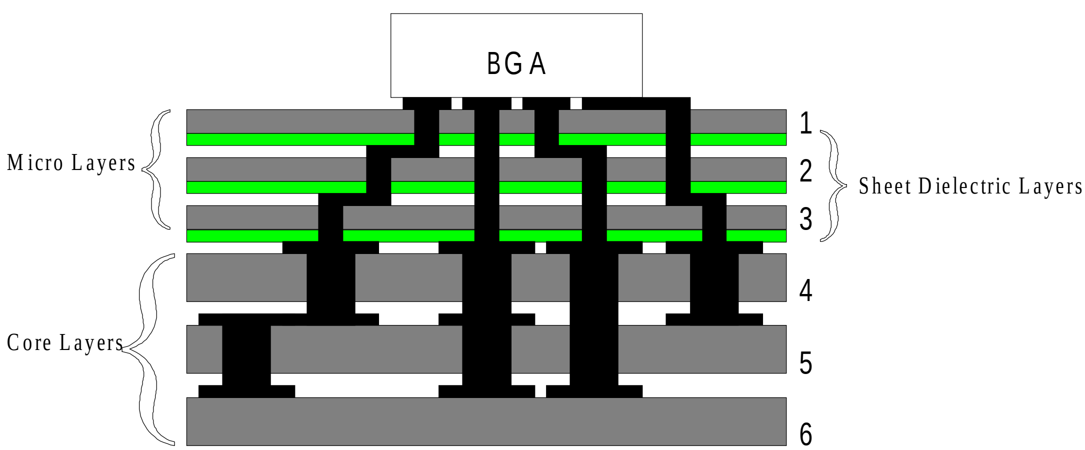

Figure 3. User-defined (Sheet_Dielectric) layers for Buried-Vias

The problem remains that of one hole size per via. If dielectric material is to be used between the micro layers and the adjacent core layer, use a solution similar to that described under
"Dielectric Micro Thru-Via Layers" with the following modifications:

- Insert a user-defined layer (sheet_dielectric) between <u>all</u> the *micro* layers & the adjacent *core* layer.

- Define the proper size & shape hole for <u>all</u> the sheet_dielectric layers in the via geometry,
- Specify the *core* layer drill size for the via hole size (no change).

The manufacturing output is still obtained by both the artwork generator and the NCDrill generator. The artworks for all the dielectric layers are photoplotted as negatives. The NCDrill data, after the manual merge described above, will now be correct for the *core* layers since it still will not be used for drilling the *micro* layers.

Drill Data required for both Micro and Core Buried-Via layers…

The solution defined above under "*Dielectric Micro Buried-Via Layers*" can be used but the dielectric artworks cannot be used directly as previously mentioned. Instead, the dielectric layers are used only to capture the hole sizes and locations. An AWK script, c utility or even ample can be used to convert a positive ascii gerber output of each dielectric layer to an ascii NCDrill data file. If a binary NCDrill data file is required, simply read the converted ascii data file using the "Drill->Open Drill Data" command, open the resulting geometry and execute "File->Save->Drill Data" command, specifying the binary option.

The methods described above are the safest way to implement micro vias in Board Station today with the current C.2 release. The situations reviewed above implemented Micro Vias with one common hole size through the *micro* layers and a larger but common hole size through the *core* layers – leaving only two hole sizes to deal with for each via.

Additional Output Requirements – Drill Schedules & Drawings

In Fablink, the normal procedure to create a drill drawing is to:

- Create a drill schedule
- Initialize a drawing
- Place the drill schedule & board/panel into the drawing
- Execute Popup->Change This Geometry->Setup Drill Symbol Rules to display the drill symbols for the corresponding drill schedule.

For designs that employ only thru-hole technology, the above procedure is no problem, but for designs utilizing buried/blind pins/vias, producing the drill drawing per layer pair (adjacent layers) is a little tricky. Again, this is inherent to Board Station and blind/buried pins & vias in general. There is a disconnect between the "Create Drill Schedule" and "Setup Drill Symbol Rules" output. It is the user's responsibility to setup the drill symbol rules on a drawing to match the drill schedule previously created and resultantly placed within the drawing. These two items should match although there is nothing to force such a rule. Having said that, and having converted dielectric artwork to NCDrill files and/or "merged" the necessary NCDrill "rule" data files per layer pair as mentioned previously, the problem is now the proper creation of the Drill Schedules and matching Drill Drawings.

If a drill drawing is required for the *micro* layers and a drill schedule is generated for those layer pairs, the drill size must be edited in the resultant drill schedules to properly reflect the hole sizes. These drill sizes, if the procedure in this document were followed, will reflect the hole size through the *core* layers when generated by the "Create Drill Schedule" command. Remember too at this point that the symbol for the two sizes will be the same. Since the drawing is not intended to support *core* layer drilling, this should be okay once the schedule is edited.

If NCDrill "rule" files were merged, drill schedules output by the "Create Drill Schedule" command would also have to be merged to produce drill drawings corresponding to each drill "rule" data file. The "Setup Drill Symbol Rules" command allows the user to combine multiple drill "rule" data to view but the "Create Drill Schedule" command allows only one drill "rule" data.

The section below entitled "Exceptions and Alternatives" describes alternate methods of incorporating exceptional uses of Micro Vias.

Exceptions and Alternatives

When Small meets Big

This refers to the via that propagates from the micro layer through to the core layer, where the small micro-via hole meets the larger core-via hole. The manufacturing process which "caps" the larger hole will allow the micro-via hole at the same exact center location (*Coincident Vias*). Implementing the methodologies described above supports this process.

The process that does not "cap" the larger hole will require the smaller micro-via hole to be offset from the center of the larger hole to prevent the metal applied to the micro-via from free-flowing down the larger hole. Normal routing in this "no-cap" case would simply offset the vias, creating a minimum stub length between the vias but clearing each other by a minimum same-net via clearance. However, these stubs eat up expensive real estate and increase metalization costs. One way to minimize stub usage is simply to overlap the via pads, create *Adjacent Vias*. Or, the smaller micro-via is placed within the annular ring of the large core-via so that when the metal is applied to the micro-via, the metal flows through the smaller hole directly onto the larger via's pad, missing the larger hole completely or in part. This technology sometimes employs "landless" vias, vias which essentially have no pads, only a hole which allows metal to flow directly into an encompassing trace, fill or pad, and limited to use on the *micro* layers. Let's call these vias *Inset Vias*.

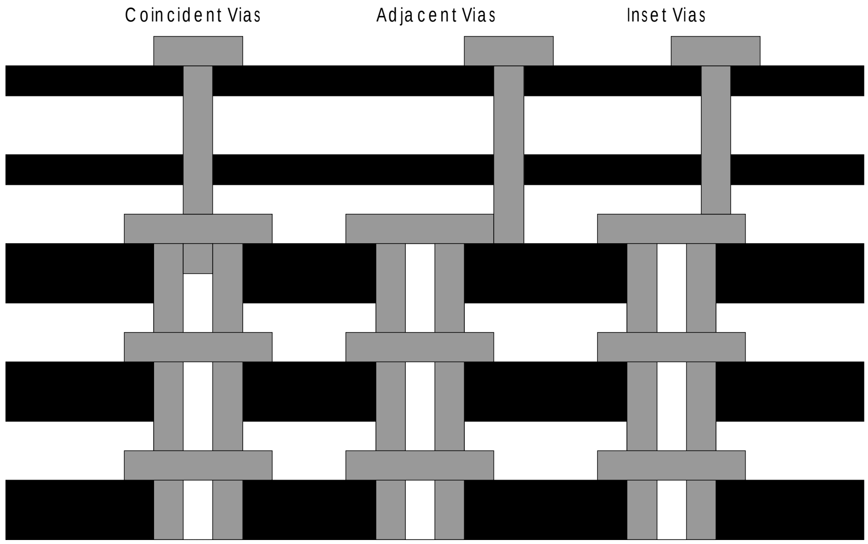

Figure 4. Micro Via Types

In order to place *adjacent* and *coincident* vias, today's Board Station user must turn same-net pad to pad checking off. This is done through the builtin function "$$set_via_grid_checking()", not usually available through a user interface. This function requires three arguments. The first argument relates to the reported condition. The third argument controls the printing of error messages. The second argument enables/disables the same-net pad-to-pad checking.

By setting the second argument to "@nocheck", Layout will allow the user to place two <u>different</u> vias - of the same net and differing hole sizes - at the same (*coincident*) or *adjacent* locations, otherwise disallowed by Layout. Obviously, no auto-router will do this so this procedure is meant as an interactive aid. When using this work-around, it is advised that this checking be disabled only at the point of entry and re-enabled immediately thereafter because it does affect all same-net checking processes for the whole design. When executing check traces, disallow the "Check Same Net Pad to Pad Clearances" option in the Check Traces dialog. This will execute the same procedure mentioned in this paragraph prior to the check, returning it to the "@check" state on exit – regardless of the option. The user should also perform the check with the option allowed to double check those intentional placements against true violations.

The *inset* via poses a bigger problem to Board Station. Board Station will not allow placement of *inset* vias, but by using a combination of the methodology mentioned in the preceding paragraph and the methodology described previously using user-defined (sheet dielectric) layers, the user can achieve the same results. By defining a set of vias with sheet dielectric holes defined in 4 locations (for orthogonal entries) or 8 locations (to include 45 degree entries), this technology can be implemented. To clarify, that is one via per location.

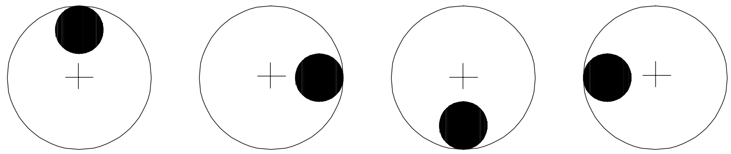

Figure 5. Four Inset Vias with sheet dielectric holes for orthogonal entries – larger circle represents the large pad of the coincident via and not defined in the via itself.

When placing an *inset* via, the user would follow the same procedure to place a *coincident* or *adjacent* via but the via selected must correlate with the current trace segment being routed. This will result in the trace over-shooting the dielectric hole, but only towards the center of the via pad which should be of no consequence because the hole and the overlapping trace segment will be drilled out. This sheet dielectric is then used as the output artwork for the sheet dielectric layer or used as input to convert to an NC Drill data file.

The procedures mentioned here are best implemented through an ample function. This ample can be smart enough to know which layer the user is currently routing on, which vias and via rules are available to transition from this layer for the current net type, automatically pick a new via or allow user to select the via and the rule, execute the "$$set_via_grid_checking()" command to turn same-net pad-to-pad checking off, place the via and turn same-net pad-to-pad checking back on. It could also be written in a way that it automatically chooses the correct inset via depending on the current direction of travel.

Coincident Vias

Even though this procedure will allow coincident or adjacent via placements, I question whether it is necessary if the methodologies previously described are followed (using user-defined/sheet dielectric layers). The usage of coincident vias is primarily the need to extract two different hole sizes at the same or adjacent location. At this writing, there is only one foreseeable condition that this occurs and that is when Small meets Big – where a *micro* layer is adjacent to a *core* layer – and where, what would appear the same via, needs to pass through both layer types. Proper definition of the physical layer structure, including insertion of the user-defined/sheet_dielectric layers, proper via construction and definition of the via rules, and, possible conversion of the sheet_dielectric artwork files to NCDrill data files, should dispense the need for coincident vias. However, inset vias do require employment of both methods.