Good Product Quality Comes From Good Design for Test Strategies

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Abstract:
Product quality can be improved through proper application of design for test (DFT) strategies. With today's shrinking product sizes and increasing functionality, it is difficult to get good test coverage of loaded printed circuit boards due to the loss of test access. Advances in test techniques, such as boundary scan, help to recover this loss of test coverage. However, many of these test techniques need to be designed into the product to be effective. This paper will discuss how to maximize the benefits of boundary scan test, including specific examples of how designers should select the right component, connect multiple boundary scan components in chains, add test access to the boundary scan TAP ports, etc. A discussion of DFT guidelines for PCB layout designers is also included. Finally, this paper will include a description of some advanced test methods used in in-circuit tests, such as vectorless test and special probing methods, which are implemented to improve test coverage on printed circuit boards with limited test access.

Background:
Classical test technology, principally bed-of-nails in-circuit test (ICT), is seeing a reduction in effectiveness due to the loss of test points on the products. In classical ICT, stimulus and responses are driven and received from the board-under-test through probes on a fixture connecting the tester to the board-under-test. In this way, the ICT can measure discrete devices and test ICs.

ICT is threatened by tech drivers like device or board miniaturization, increased component density on PCBs or high-speed interconnection layout rules which manifest in the removal of test points due to the lack of PCB real estate, the need for controlled impedance on high speed interconnecting traces or the use of SMD devices like BGAs, flip chips instead of through-hole devices, to name a few reasons. ICT requires probe access to drive the device inputs and listen to the outputs, the removal of test points reduces the adequacy and diagnostic accuracy of ICT.

Test technology innovations that preserve the test coverage even after the loss of test access to the nodes of the product are needed. Below is a review of some of these innovations.

Boundary Scan
In the late 1980's, a collection of companies, weighted by Telecoms, decided to take advantage of Moore's law and start building test facilities into the ICs themselves.

The result of their efforts was a standard, IEEE 1149.1, released by IEEE in 1990, describing how the physical test probes placed on the test points on the nodes of the product were replaced by boundary scan test cells within the device, connected to each pin of the IC. During the normal operation of the device, these test cells allow data to pass through them transparently, but during the boundary scan test, these test cells can be configured to drive or receive data independently from the functionality of the pin it is attached to. The test cells within the device are linked and controlled by a test access port (TAP) controller within the IC using the TCK and TMS pins. Data can be serially input into each test cell through the TDI pin and output through the TDO pin on the TAP controller. The data can also be output in parallel through the pins and received by another boundary scan supported device on the other side of the trace on the board. This action of transferring data between boundary scan devices does not require physical test probes on the interconnecting nodes between the devices. By connecting the boundary scan supported devices together in a daisy chain, it is possible to control all of the devices in the chain using just one set of test access port signals.

Similarly, if a non-boundary scan supported IC is placed in the circuit such that all its pins are connected to the interconnecting network within the boundary scan chain, it is possible to drive and receive signals to and from the device. This way, the functionality of the non-boundary scan device can be simulated using the surrounding boundary scan devices.

The standardization of boundary scan test method enables computer aided design (CAD) tools to include features to assist component designers or PCB layout designers to design boundary scan into their devices or PCBs. Test systems include features to automate the development of boundary scan tests whenever they are detected in the PCB design. The standards enable boundary scan tests to be generated without the need to know the functionality of the component. Board designers may be able to develop and execute the tests themselves on their prototypes, thus providing additional test and diagnostics during design validation tests. This brings the benefit of designing boundary scan into the products back to the designers, not just the manufacturers.

Design for Boundary Scan testing
Boundary scan test capabilities need to be designed into the product. For example, the components selected must be boundary scan compliant, the boundary scan compliant devices are chained together and there are test points assigned to the TAP pins controlling the boundary scan devices. Let's take a deeper look at these areas.

Selecting boundary scan compliant components
In order to implement boundary scan testing, it is required to first select boundary scan supported integrated circuits (ICs). These ICs can be easily identified by the TAP pins, TDI, TDO, TMS, TCK and sometimes TRST#. Today, there are many ICs that are boundary scan enabled or have boundary scan supported alternatives of the same IC.

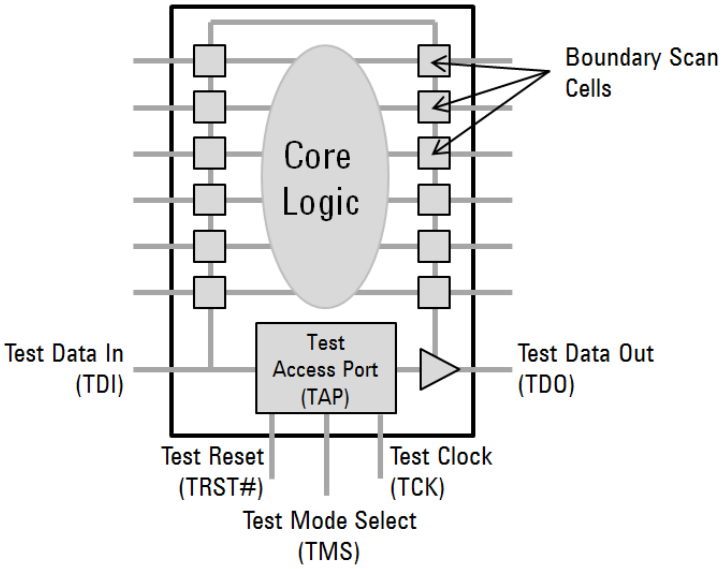

Figure 1: Block diagram of a boundary scan supported device

There are ICs that require a special condition before it will function in "boundary scan mode", these ICs should be avoided where possible. The IEEE 1149.1 standard defines that any special compliance condition must be specified in the boundary scan description language (BSDL) file for that IC. The BSDL file describes how boundary scan is implemented in the IC, all the types of test cells assigned to each pin, the sequence of how the test cells are chained in the IC and the conditions required to enable compliance. However, not all compliance conditions implemented by component designers follow the IEEE 1149.1 standards. A device may require a special pattern of digital vectors instead of static logic levels to be exerted to special compliance enable pins, or in some cases to the TAP pins, to enable the device to become IEEE 1149.1 compliant. These special patterns may not be described clearly in the BSDL file, as required in the standard, posing a challenge for test engineers. These special patterns may be described in the datasheet, user reference manual, application notes or errata instead. This is not compliant to the IEEE 1149.1 standard and would require extra care and effort from the test engineer for the implementation. When designing the IC, It is best to stick to the static logic levels exerted to specific pins on the device as described by the IEEE 1149.1 standard or not require any compliance patterns at all.

```
--    Compliance enable description
      attribute COMPLIANCE_PATTERN of SLT ; entity is
            "(PWRGOOD, DPRSTPD) (11)";
```

Figure 2: Compliance_Pattern section in BSDL file compliant to IEEE 1149.1 standard

When designing custom application specific ICs (ASICs), remember to design boundary scan into the IC so that boundary scan can be used to test the device and the board that it is assembled on. The test cells defined for each pin of the ASIC should preferably be bidirectional or self-monitoring cells to enable better controllability and observability during test. The CAD tool used in the ASIC design would be able to automate the insertion of the boundary scan cells into the ASIC. When completed, a BSDL file should also be automatically generated. This should eliminate the likelihood of errors inserted through manual processes.

The last but not least step in the component selection process is to verify that the boundary scan devices are compliant. According to the IEEE 1149.1 standards, at the minimum, boundary scan compliant devices need to include the TDI, TDO, TMS, TCK pins and support the basic instructions for SAMPLE/PRELOAD, EXTEST and BYPASS. The boundary scan components should be tested to ensure that the BSDL file matches the silicon.

Chaining boundary scan supported components
Once the boundary scan components are selected, the boundary scan components should be connected to each other in chains to enable test coverage of the interconnection nodes and so remove the need for test points on these nodes.

The boundary scan components are daisy-chained together by connecting the TDO of the first boundary scan device in the chain to the TDI of the second device and the TDO of the second device to the TDI of the third device, and so on. The TCK and TMS pins on all the devices on the same chain are connected in parallel [1].

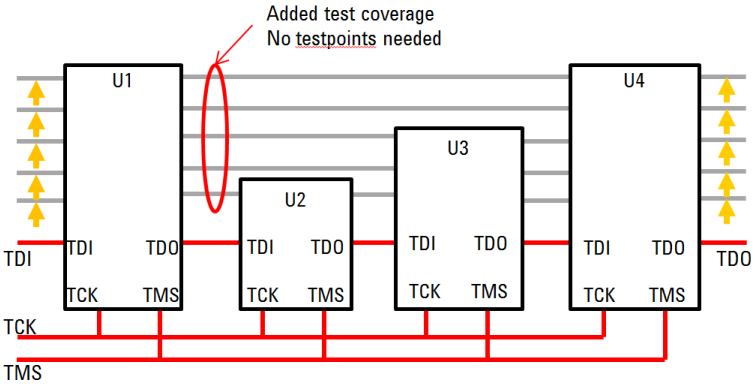

Figure 3: Chain boundary scan devices to save on testpoints

The states of the boundary scan test are all edge triggered. The state of TDO changes on the falling edge of TCK, while data present at TDI are clocked into the test cell on the rising edge of TCK. The state machine in the TAP Controller is controlled by the TMS pin. Control signals driven to TMS are changed on the falling edge of TCK and are clocked in on the rising edge of TCK. Therefore, it is important to keep the skew of the parallel TCK and TMS signals on all the ICs in the chain to a minimum (less than ¼ TCK clock period). Most boundary scan tests are executed with TCK set at about 1 Mhz to 2 Mhz. We usually increase the TCK frequency for Flash programming via boundary scan to shorten the programming time. Here, TCK is set as high as the circuit allows for a stable test. This is limited to the tester capability commonly below 100 Mhz. It is best to treat the TCK and TMS signals like high-speed signals and layout the TCK and TMS traces accordingly so that the TCK and TMS signals appearing at each device are aligned, especially for long chains. This allows TCK to be set as high as possible during testing to reduce test time. For long chains, it may be required to buffer the TAP signals to address fan-out issues, especially TCK, TMS and TRST#, since they are connected in parallel to the devices in the chain.

Where there are boundary scan devices of different logic levels on the same board, chain the devices of the same logic levels together. This will result in multiple boundary scan chains on the board-under-test. This minimizes the complexity of adding level shifters within the chain to transition between the logic levels. The trade-off is that more TAP connectors are needed on the board and circuitry is added, possibly in the fixture, to join the chains together externally in order to get the same test coverage from the interconnections between the chains. The boundary scan tester used for testing usually has multiple ports to connect to the multiple chains. Through software settings the multiple chains can be connected, within the tool itself, to form a single long chain. The boundary scan tester will also handle the different logic levels internally, too.

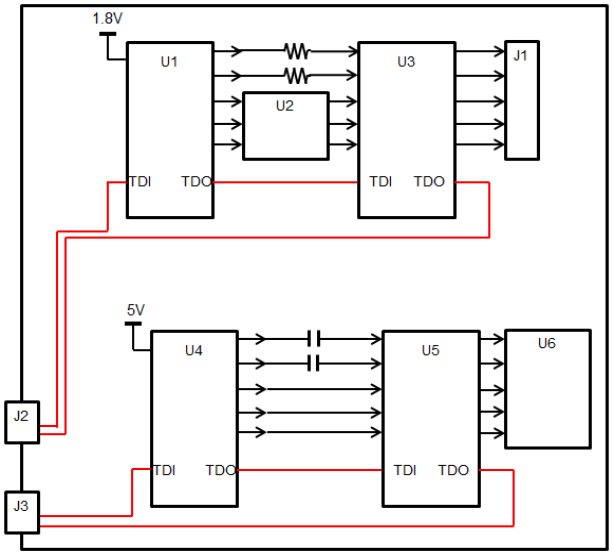

Figure 4: Chain boundary scan devices of same logic levels together

Another consideration when deciding on chaining up boundary scan devices is related to the programming of flash device through an adjacent boundary scan device. This boundary scan device should be separated from any chain and placed on its own. This helps to reduce the programming time because the chain length is reduced, so the number of clocks needed to push the data through the chain to the boundary scan device controlling the flash is minimized.

Test point assignment
Firstly, all the boundary scan test access port pins (TAP pins) which includes the TDI, TDO, TMS, TCK and, where available, the TRST pins should have a test point assigned to their respective nodes on the circuit.

The test point is preferred to be a through-hole connector located close to the edge of the board or an SMD connector or a test pad or test via on the trace in that order. Connectors are preferred for stand-alone boundary scan testers. If test pads or test vias are assigned, a fixture with test probes is required to connect the tester to these nodes.

When designing in connectors, each chain should have one TAP connector assigned. Through-hole connectors are preferred because the connector pins can be probed on a fixture. This gives the flexibility to execute the boundary scan test on an ICT or on a stand-alone boundary scan tester. The smallest connector is a 10 pin connector. The five TAP pins should be alternating with ground pins. TCK should be placed away from TDO so that they do not crosstalk. Ground pins should all be connected directly to the board ground. With the TAP connector assembled as part of the product, the product can be tested with boundary scan in the field, possibly during repairs. This can be part of the fault diagnostics tools used by the repair operators.

When designing in test pads or test vias, they should all be accessed from the same side of the board, preferably, from the bottom side of the board. This is because probes to the top side of the board requires long transfer wires to connect back to the tester resources located at the bottom of the board. These long wires will attract noise and the test engineer will also have to manage the skew in the signals if the TAP pins are located on both sides of the board.

Add pull up or down resistors
To ensure that the boundary scan device is at a stable, known state, it is important to include pull-up or pull-down resistors to the TAP pins, even if the device already has pull-up or pull-down resistors within the IC. Pull up resistors should be assigned to TDI, TDO and TMS. These resistors would be 1.2k ohm in value tied up to the source voltage. TCK should be tied low through a 50 ohm to 100 ohm resistor. TRST#, if available, should also be tied high.

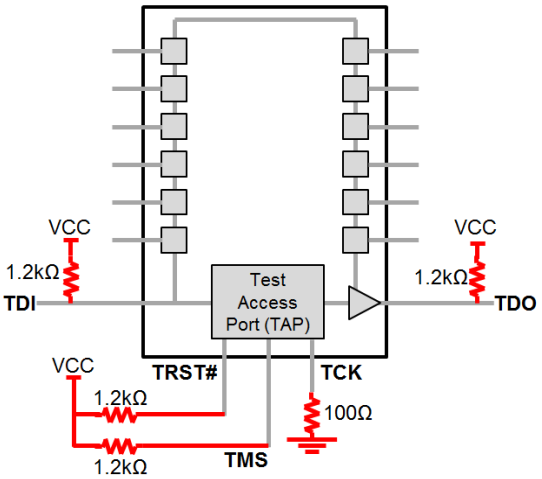

Figure 5: Pull up or down resistors for TAP pins

Use of latest boundary scan standards
New extensions to the boundary scan standard are constantly being developed, such as IEEE 1149.6 for testing ac-coupled high-speed differential signals, or IEEE 1581 for testing memory integrated circuits or IEEE 1687 to access and control embedded instruments within the device. These new standards provide new methods to mitigate issues with implementing test coverage on the product. The product should be designed to enable these tests where needed.

Vectorless testing with boundary scan
Vectorless testing with boundary scan is an advanced test method that pairs vectorless testing techniques with boundary scan test to enable testing of ICs or connectors without test points. Vectorless testing is a test method that is able to test that the IO and control pins of an IC or connector are soldered properly on the PCB without the need to write digital test vectors for that test.

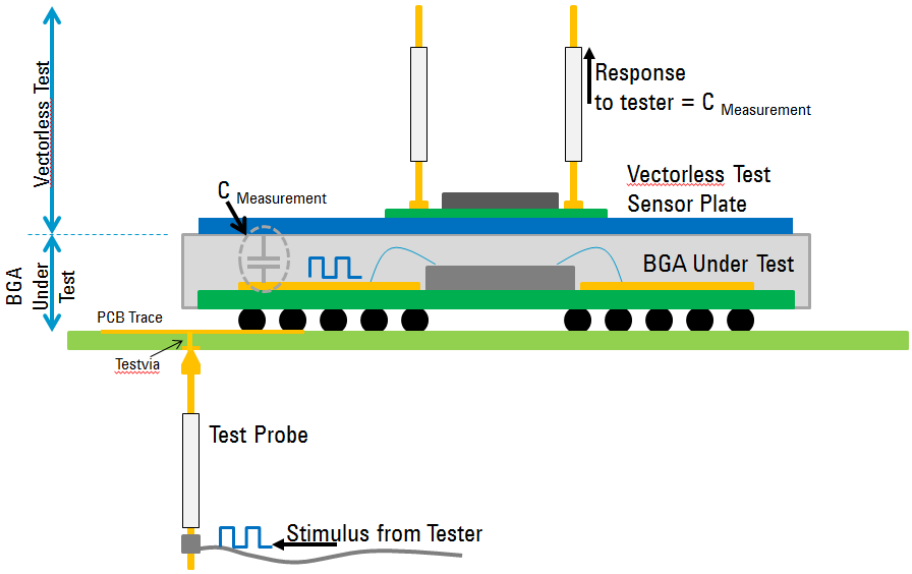

Figure 6: Vectorless test method using ICT

By stimulating an AC signal into the IO pin of the device, if there is a good electrical connection of that pin to the solder pad on the PCB, the strong stimulus at the pin can be detected via a sensor plate placed on top of the device. This sensor plate acts as the second plate of a capacitor while the component pin is the first plate. By comparing the very small capacitance that is detected against a known good reading, the test is able to differentiate between a good contact of the device pin under test to the solder pad on the PCB or not. In ICT, the stimulus is driven into the device pins through probes. But if we can send a toggling signal to that same device pin through the adjacent boundary scan device connected to the same nodes, we can detect this signal using the sensor plate on the device under test in the same way [2].

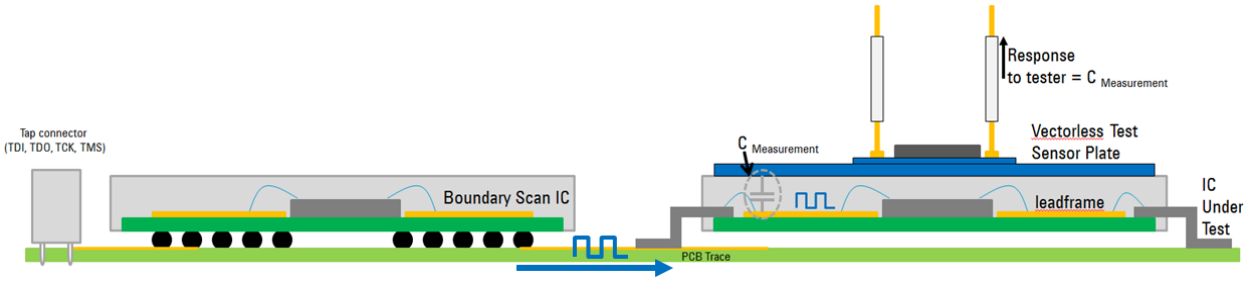

Figure 7: Vectorless test method using Stand-Alone Boundary Scan Tester

The benefit of this test method is that it is vectorless, meaning that the test engineer does not need to fully understand the function of the device to drive the required stimulus for the desired responses. The test equipment that supports this test method will also have software that automates the test generation, so that the test engineer does not need to figure out, for instance, how many clocks are required to send the test stimulus through the boundary scan chain.

This is a quick way to test connectors or ICs that have pins connected to a boundary scan chain. The test does not require test points on the interconnecting nodes between the boundary scan chain and the device. The device would otherwise be untested if the test points were missing. By designing in boundary scan into the product, the device can now be tested.

Special Probing methods

In-circuit testing requires test access to the nodes on the circuit. While test innovations have been developed to get around the loss of the test access, there are some trade-offs with all of these innovations. Nothing beats the actual probing of the test point during the test.

One reason why test points need to be removed on high-speed interconnecting traces is because of the noise the test pad or test via attracts when it is placed next to the trace. The test pad or test via are usually 3 to 6 times wider than the traces. For example, the diameter of the test pad can be 30 mils compared to a 5 mil trace it is attached to. The test points present a lumped capacitance somewhere in mid-trace. This causes impedance mismatch on the high-speed traces which results in reflections. The effort to balance the traces and the risk of malfunction of the circuit has caused the removal of the test points on these traces.

The innovation here is to change the physical characteristics of the test point such that it does not load the trace. The test point is so small that it is only the width of the trace. Enough solder is placed on the test point to form a bump on the

trace. Instead of using a sharp probe that pokes into the solder on the test point for electrical contact, a flat head probe rests on the solder bump flattening it slightly.

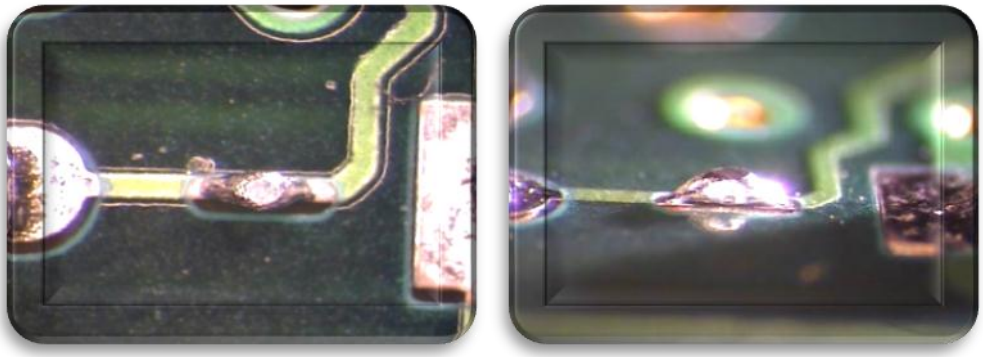

Figure 8: Special Probing on small solder bump on trace

Shrinking the test point to this size reduces its loading effect drastically. Tests have shown that even with 30 of such test points on the same trace, the high frequency performance of the 2 GHz signal through that trace is maintained [3]. The tests executed at the in-circuit tester will not reach such high frequencies, but this means that the test points required for the in-circuit test can be placed on the traces and left there without affecting the operation of the product.

Handbooks and guides have been developed to describe the dimensions of these test points [4]. To the PCB layout designer, it is as if they are creating a point on the trace that is not solder masked. The manufacturing process is not changed. The stencil used in the solder pasting process will have a void at the test point location on the trace. The same solder pasting process will layer solder paste on the test point location and the solder bump will form during the reflow process.

This innovation applies only to traces found on the top or bottom layers of the PCB. To get the most of this innovation, the high-speed traces need to be routed to the top or bottom layers of the PCB. This also means that enough keepout space is required for the probes. So, placing the test points within a forest of tall components may make it difficult for the probe to touch the test point without hitting the surrounding components and possibly damage them in the process.

Conclusion:

Advanced test methods such as boundary scan, vectorless testing or special probing methods, derived from test innovations are constantly being developed to overcome the issues with implementing proper testing on today's products. However, the products need to be designed specifically for the implementation of these advanced test methods. Design engineers should think ahead about how the product is to be tested. Collaboration between R&D and test is crucial to ensure that products are tested adequately in mass production so that there is enough confidence in their quality before they are shipped customers. This is how good product quality comes from good design for test strategies.

References:

[1] "Easing Boundary Scan Into In-circuit Testing", Adrian Cheong, ECNMag, Jun 2011.

[2] "Augmenting Boundary-Scan Tests for Enhanced Defect Coverage", Dayton Norrgard and Kenneth P. Parker, International Test Conference, Oct 2008, Santa Clara CA.

[3] "Implementation of Solder-bead Probing in High Volume Manufacturing", M. Doraiswamy and J. J. Grealish, International Test Conference, paper 5.4, Oct 2006, Santa Clara CA.

[4] "Applying a New In-Circuit Probing Technique for High-Speed/High Density Printed Circuit Boards to a Real-Life Product", Chris Jacobsen and Kevin Wible, APEX 2005, Feb 2005, Anaheim CA.

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Agenda

Summary of Advanced Test Methods

Design for Test Guidelines

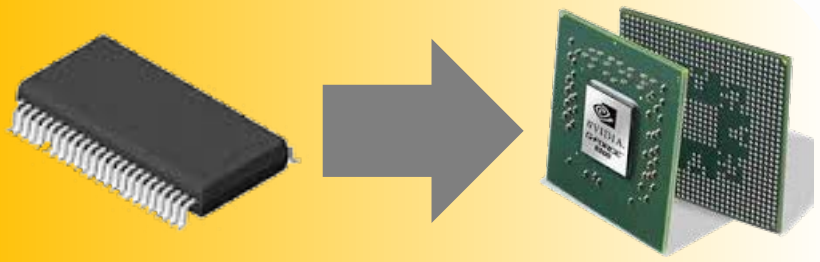
Other Advanced Test Methods

Effects of Product Trends

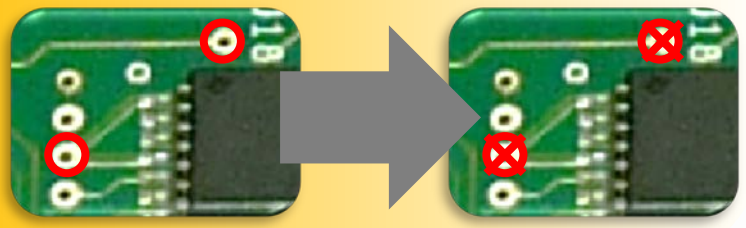
Customer Needs

- Easier
- Faster
- Smaller
- Smarter
- Richer

Products



Components



PCB Design

Product Miniaturization
Higher density PCB
High-speed interconnections

Loss of test points
Loss of test coverage
Loss of confidence

Advanced Test techniques

- Boundary scan
- Vectorless test methods
- Special Probing methods

IEEE 1149.1 BOUNDARY SCAN

IEEE 1149.6
IEEE 1149.8.1
IEEE 1581
IEEE 1687
… etc

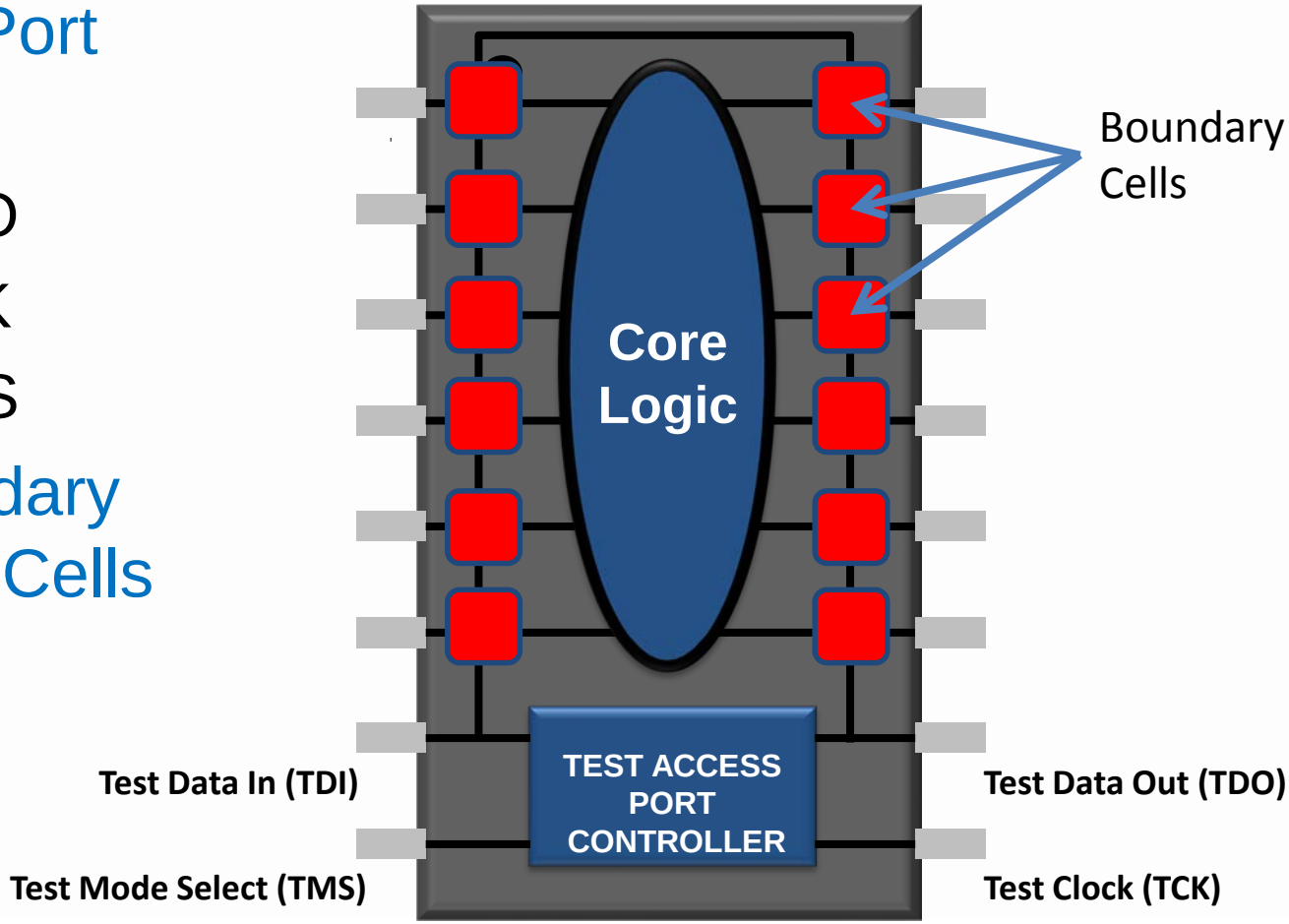
Boundary Scan Design Guidelines #1

- Select boundary scan compliant devices

TAP Port

- TDI
- TDO
- TCK
- TMS

Boundary Scan Cells



Boundary Scan Design Guidelines #2

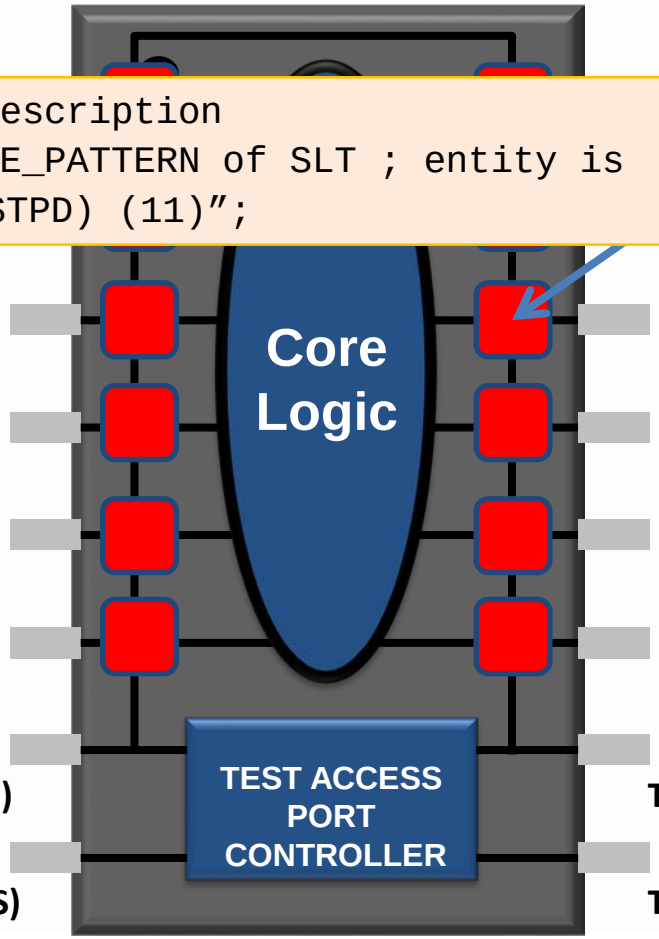
- Devices which require Compliance Patterns

BSDL File

```
--   Compliance enable description
     attribute COMPLIANCE_PATTERN of SLT ; entity is
          “(PWRGOOD, DPRSTPD) (11)”;
```

Non-Standard:

- Datasheet
- Errata
- Reference manual
- Application Note

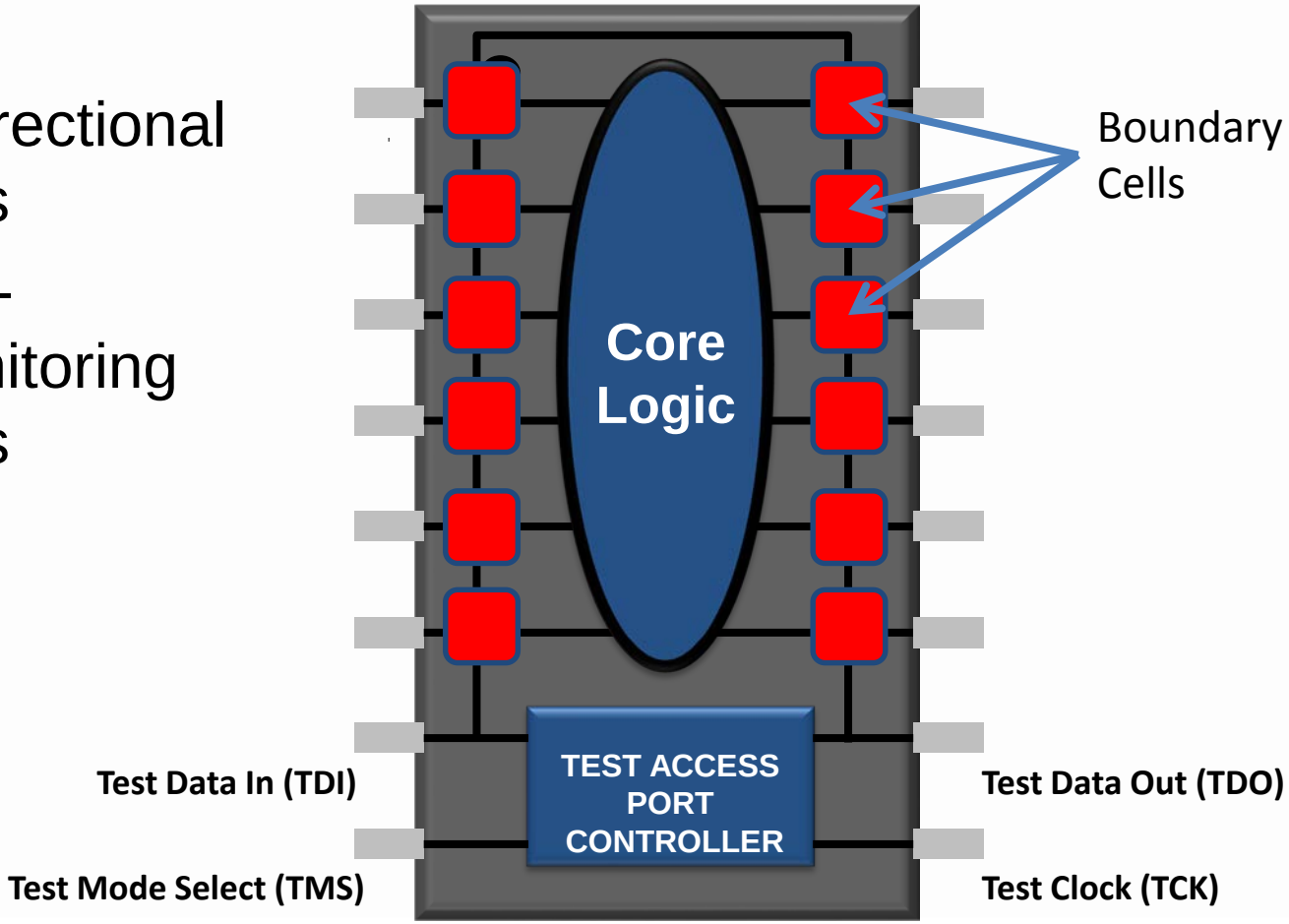


Boundary Scan Design Guidelines #3

- Enable ASICs with boundary scan

Use

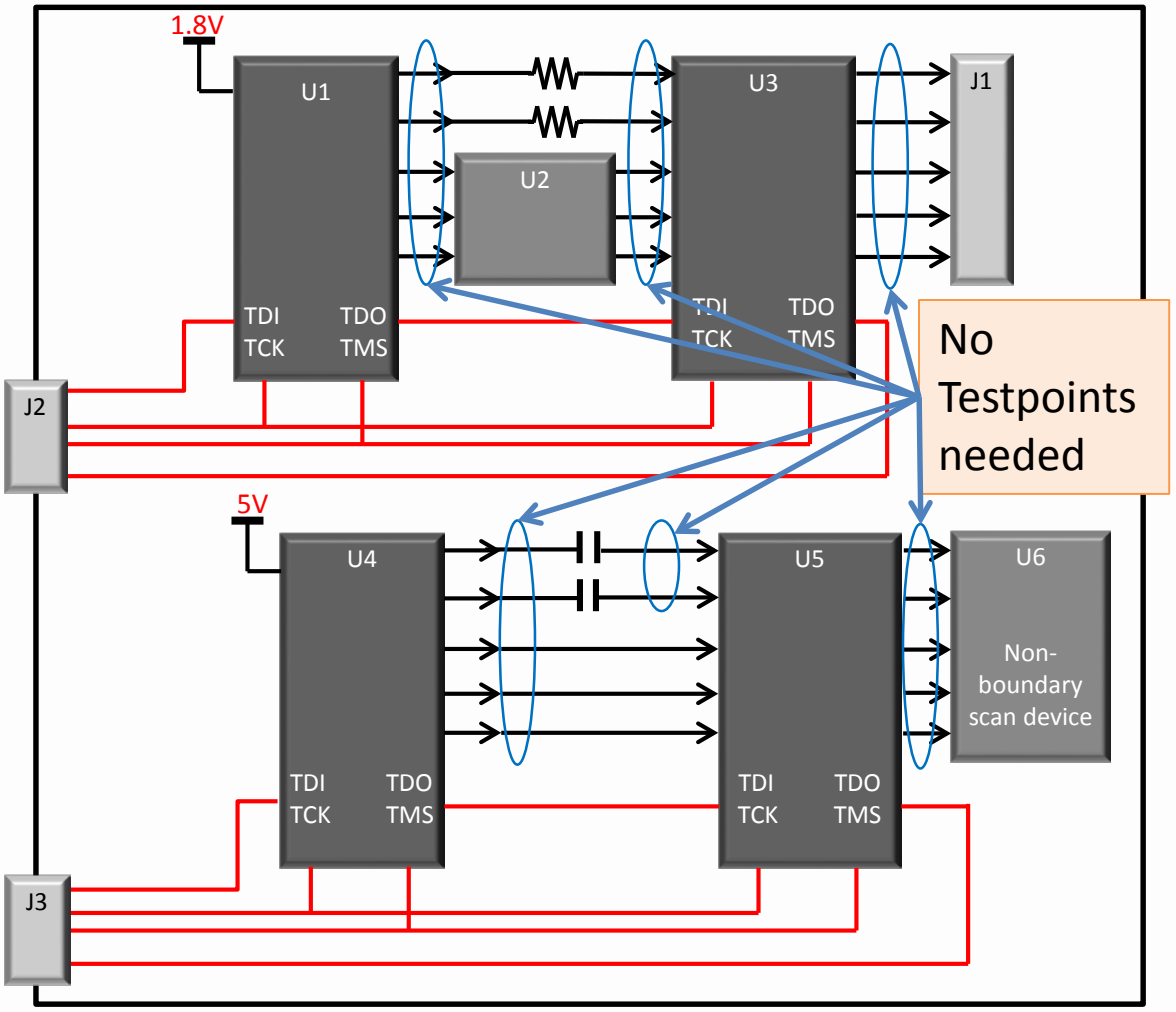
- Bidirectional cells
- Self-Monitoring cells



Boundary Scan Design Guidelines #4

- Chaining boundary scan devices

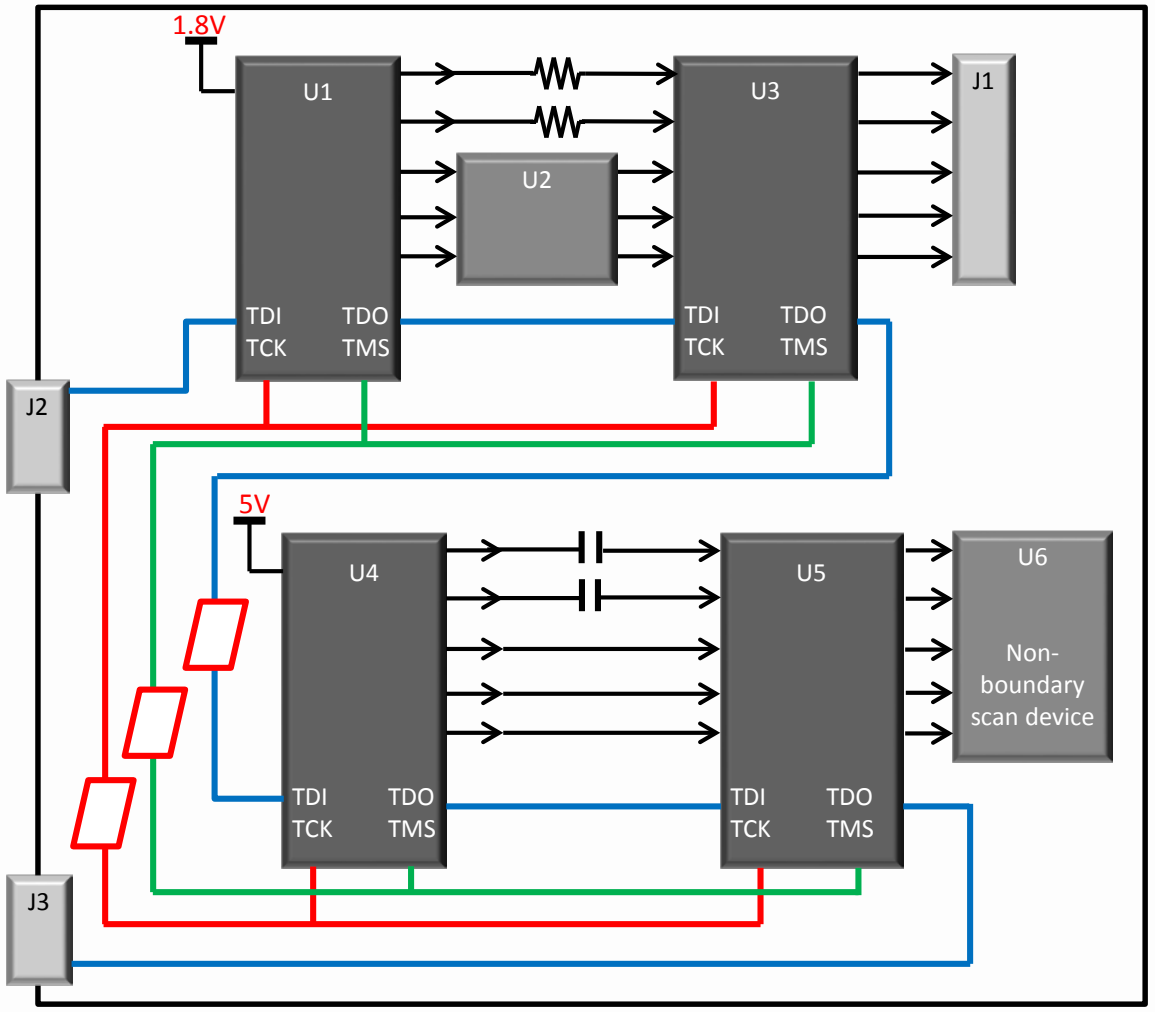
- Daisy Chain
- Testpoints on interconnecting nodes can be removed
- Treat TCK and TMS like high-speed traces
- In long chains, add buffers (on TCK, TMS, TRST#)



Boundary Scan Design Guidelines #4

- Chaining boundary scan devices

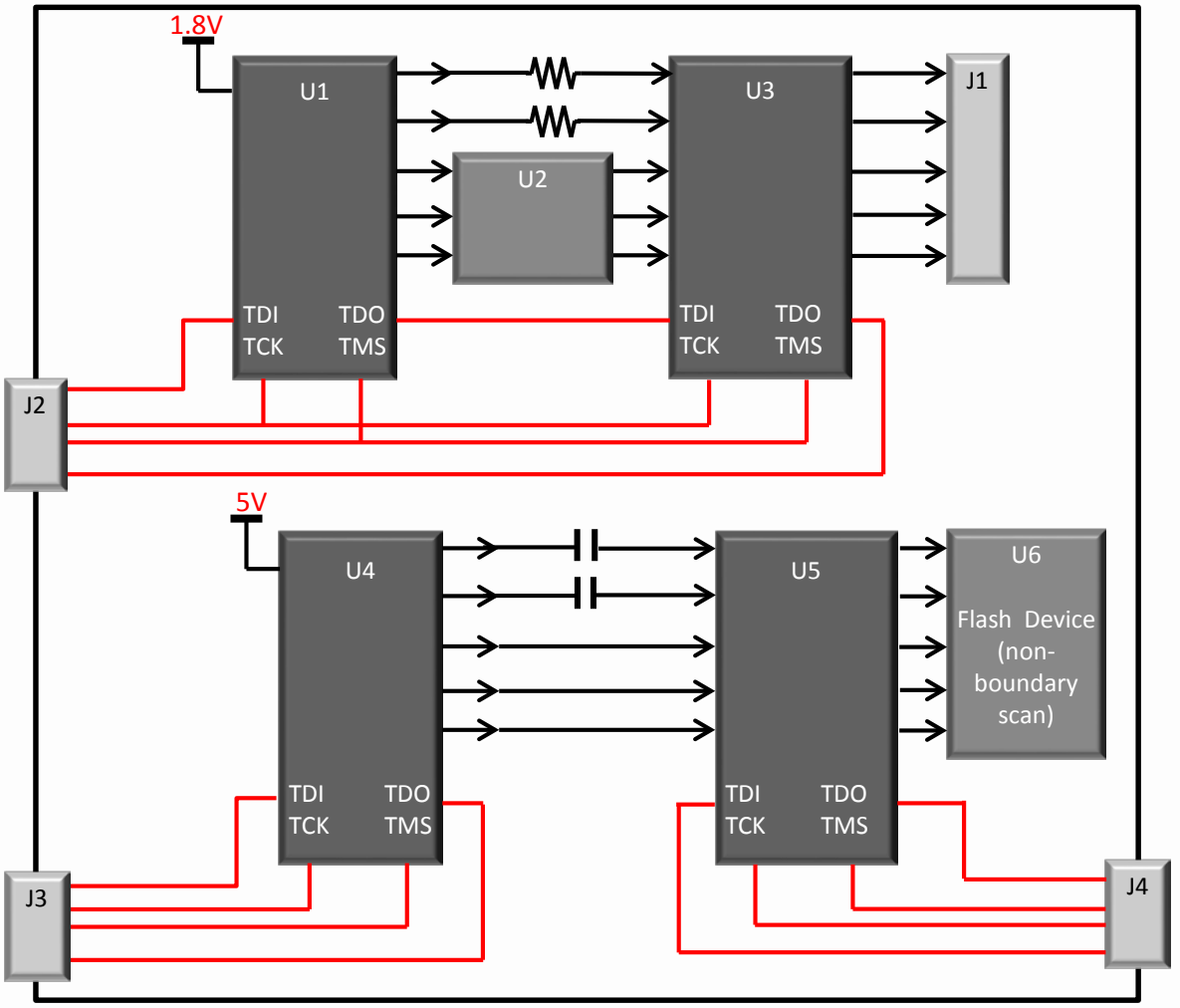
- Group devices of the same logic levels together
- Or use level shifters



Boundary Scan Design Guidelines #4

- Chaining boundary scan devices

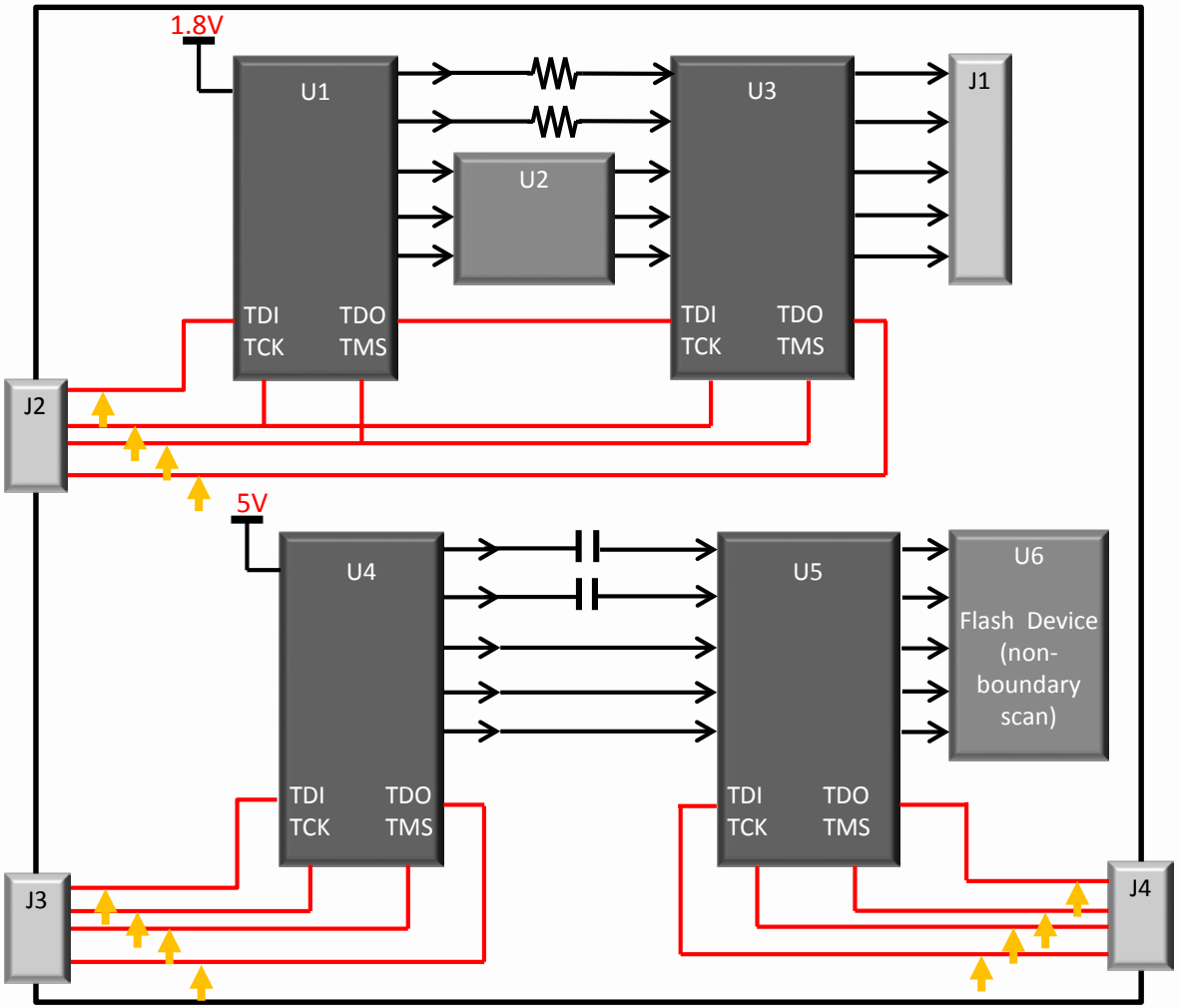
- Separate Flash Programming



Boundary Scan Design Guidelines #5

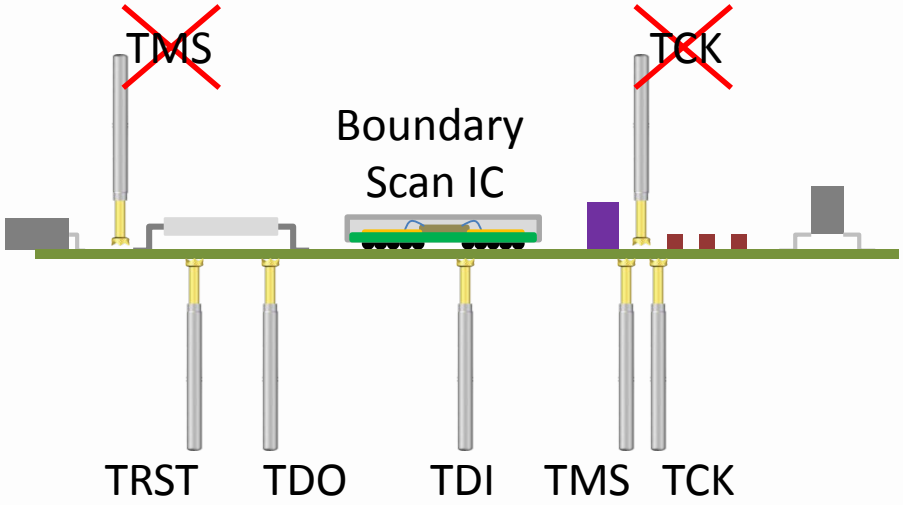
- Testpoint assignment

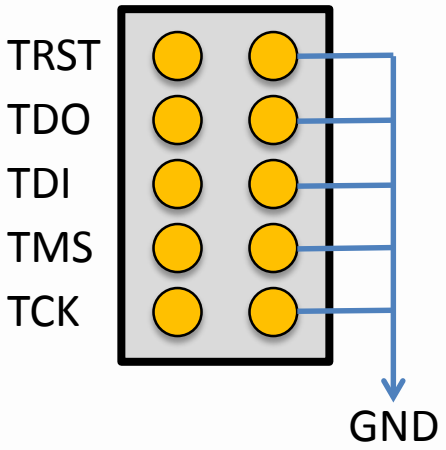
- Each TAP pin on each device
- Connector and/or Testpad



Boundary Scan Design Guidelines #5

- Testpoint assignment





- Testpoints on same side of PCB
- Testpoints on bottom side of PCB
- On connector, alternate signal with GND
- Place TCK away from TDO
- Leave connector on PCB for field repair

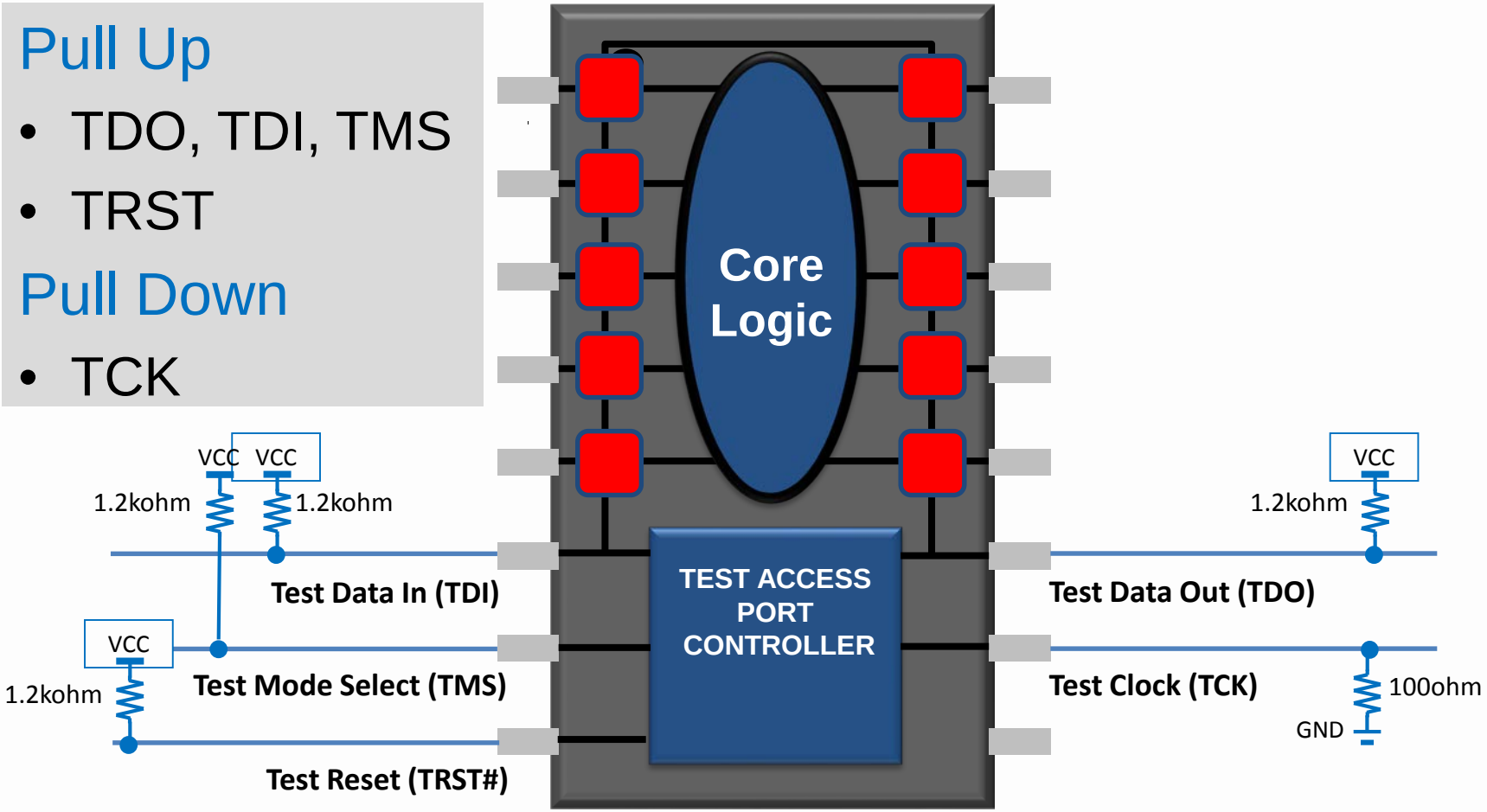
Boundary Scan Design Guidelines #6 - Assigning Pull up / down resistors

Pull Up

- TDO, TDI, TMS
- TRST

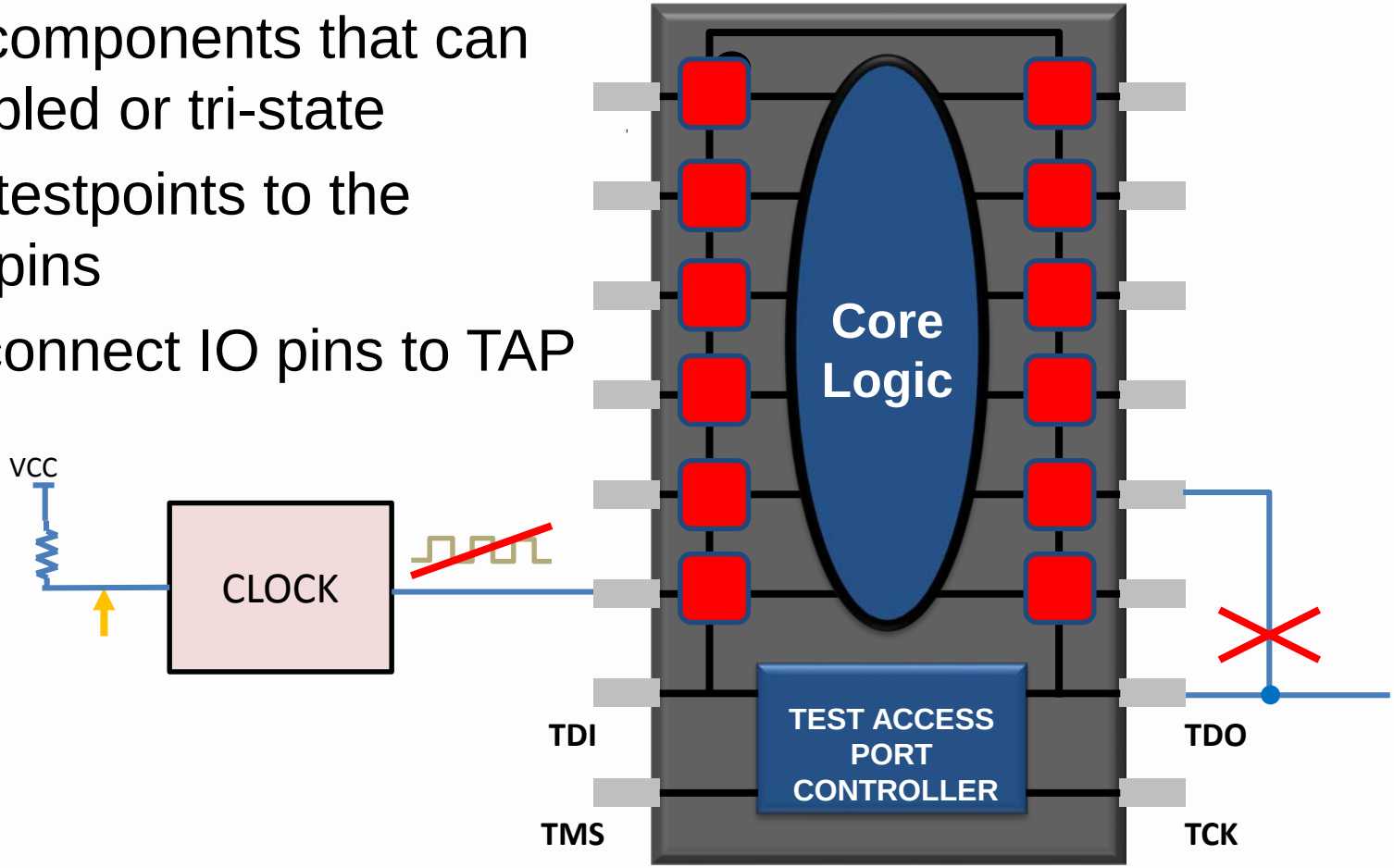
Pull Down

- TCK



Boundary Scan Design Guidelines #7 - Disable upstream devices

- Select components that can be disabled or tri-state
- Assign testpoints to the enable pins
- Do no connect IO pins to TAP pins.

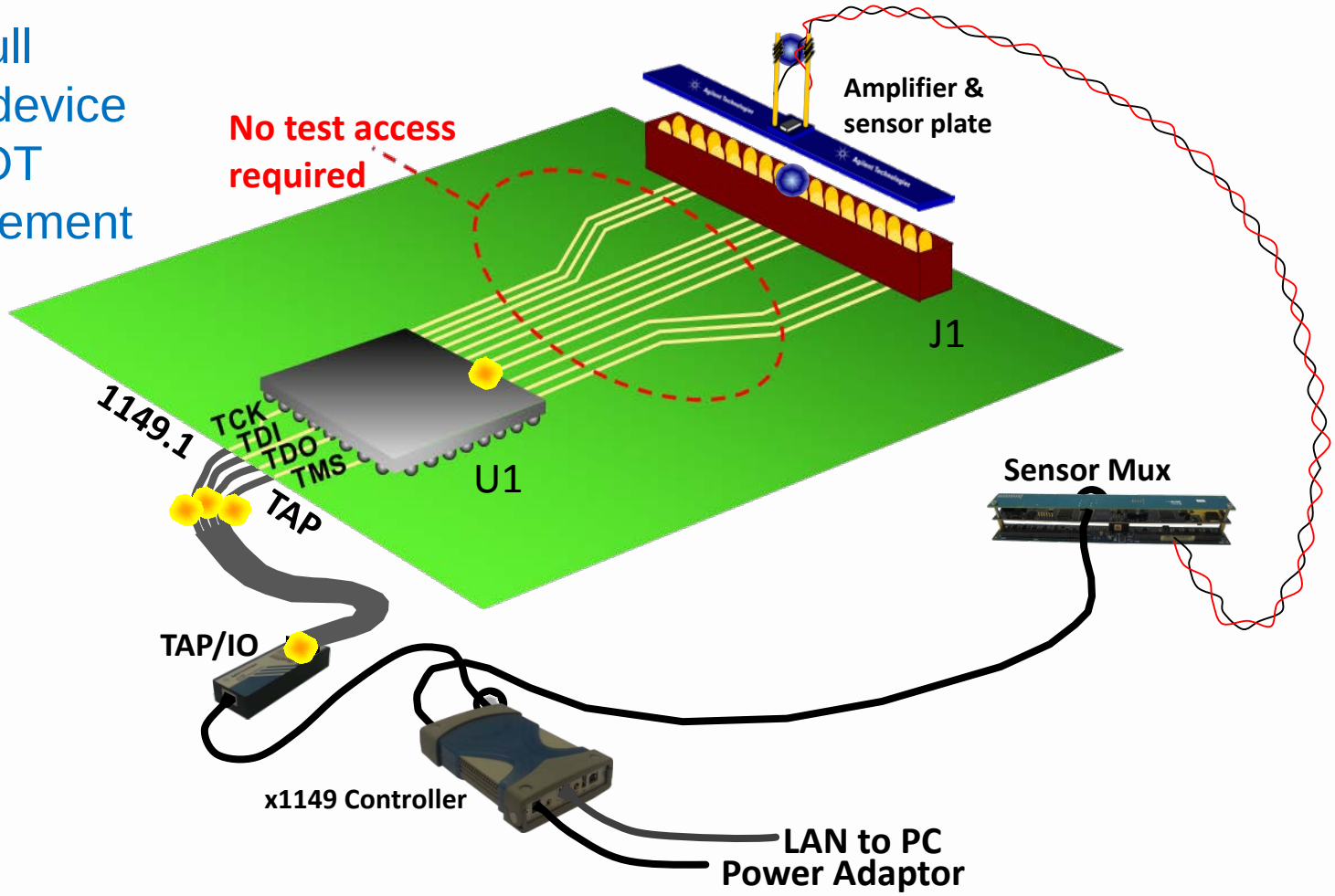


IEEE 1149.1

BOUNDARY SCAN & VECTORLESS TEST

Other Advanced Test methods
- Vectorless Testing with Boundary Scan

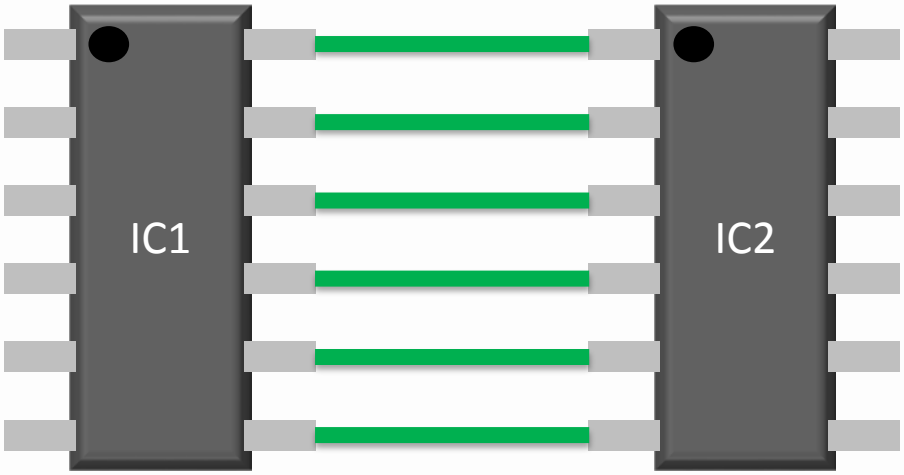
Knowledge of full functionality of device under test is NOT required to implement this test



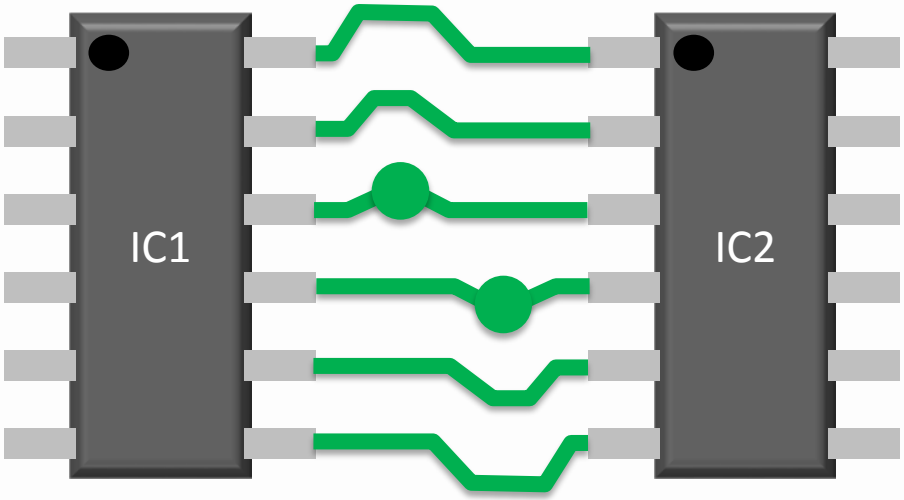
SPECIAL PROBING METHODS

Other Advanced Test methods
- Special Probing Method

- Testpoints cause noise on high-speed traces
- Effort needed to adjust traces to fit testpoints, yet ensure balance



No test points, ideal layout

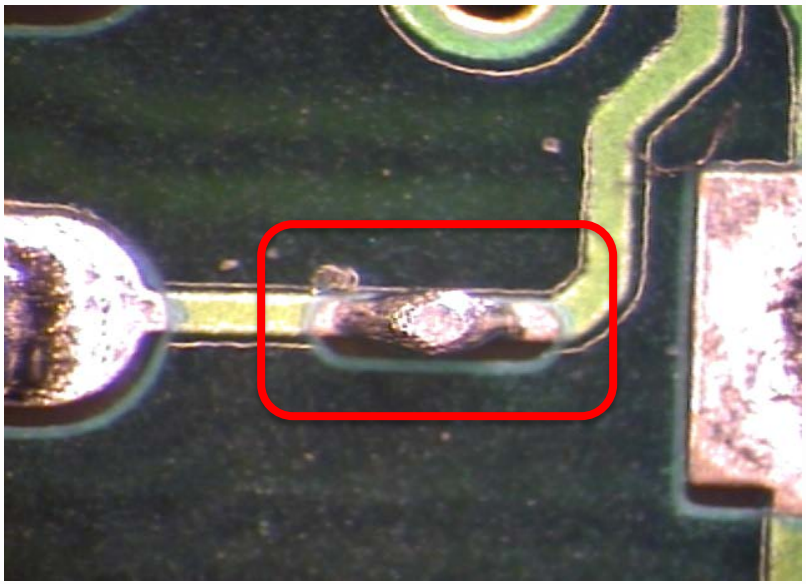


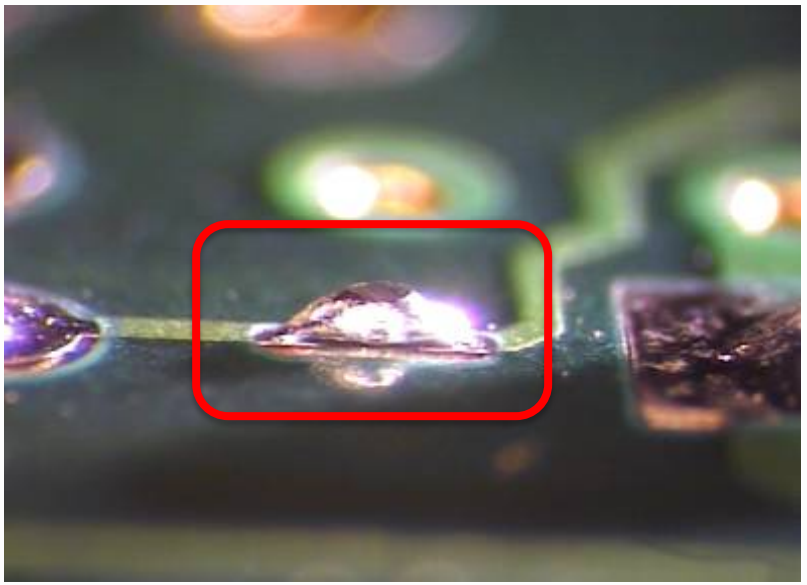
Two added test points

Other Advanced Test methods
- Special Probing Method

Shrink the testpoint

- Same width as the trace
- Minimize solder

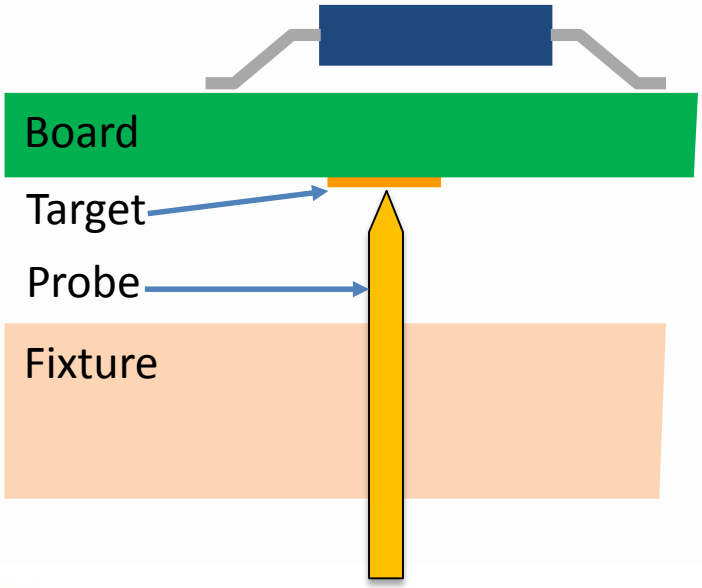




Other Advanced Test methods
- Special Probing Method

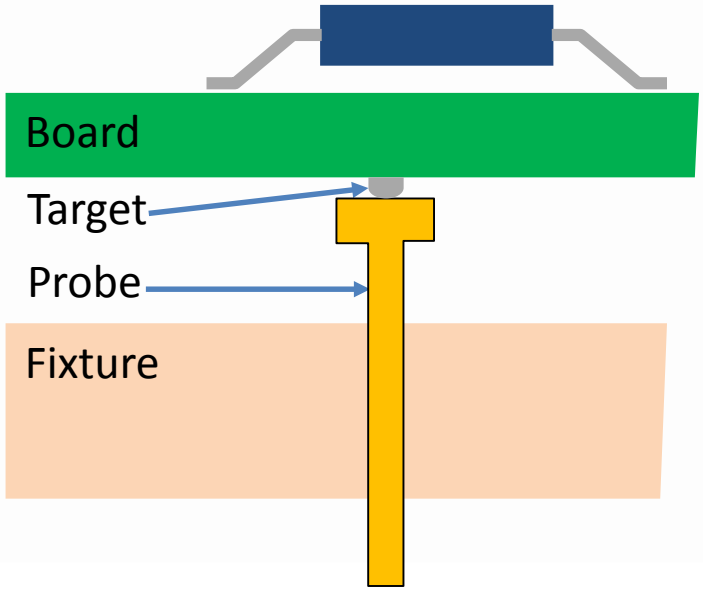
Old Way (Close Up):

- Place target on the Board
- Hit it with a pointed probe in the Fixture

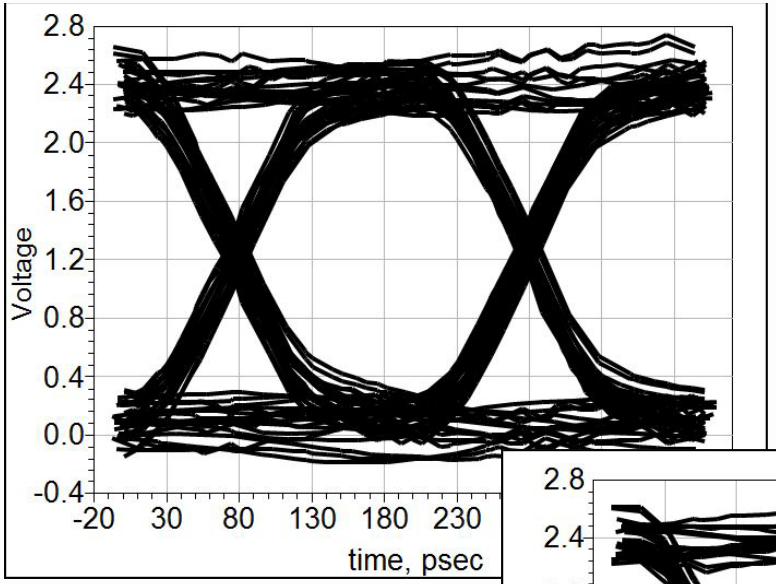


New Way (Close Up):

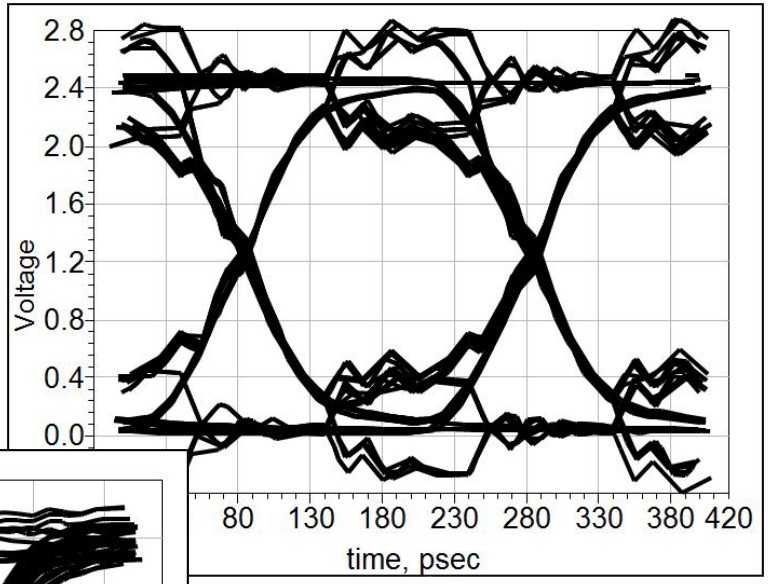
- Place target in the Fixture
- Hit it with a pointed probe on the Board



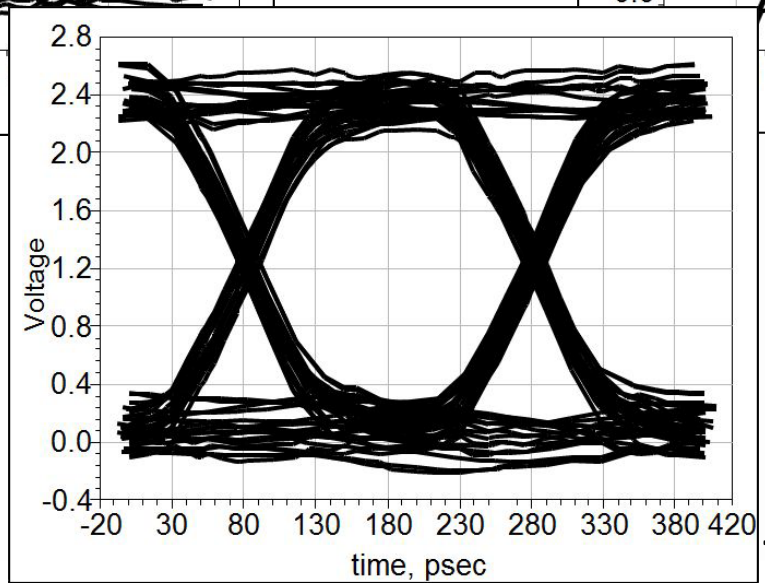
Other Advanced Test methods
- Special Probing Method



Ideal Trace



Trace with 35 mil test target



Trace with 9 bead probes

Source: "A New Probing Technique for High-Speed/High-Density Printed Circuit Boards", K. P. Parker, International Test Conference, paper 13.1, Oct 2004, Charlotte NC.

Conclusion

Advanced test methods

→ Mitigate issues resulting from loss of test access

→Requires test to be designed into the product

Collaboration between R&D and Test is crucial

→Ensure products are tested adequately

→Confidence to ship good quality products

Good Product Quality comes from
Good Design for Test Strategies

Thank You!

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The End