♦ Silicon Microelectronics Technology

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Two inventions—the bipolar transistor and the integrated circuit—have fundamentally revolutionized the technology of mankind. Within a period of fifty years, the microelectronics industry has increased the number of transistors fabricated on a single piece of semiconductor crystal by a factor of about 100 million, that is, 1.0e10^{+8}, a productivity phenomenon unparalleled in the history of technology and mankind. This paper begins with a historical review of that revolution—from the first integrated circuit to modern very large scale integration (VLSI) technology—and then reviews the development of present-day microelectronics manufacturing technology, based on the concept of the "planar process." The topics covered include silicon crystal technology, crystal dopant techniques, silicon oxidation development, lithography, materials deposition processes, pattern transfer mechanisms, metal interconnect technology, and material passivation technology. The paper concludes with a review of the major technical and economic issues that face the microelectronics industry today and discusses the future technical and economic paths that the industry may take.

The Past

This section presents a historical review of the technology revolution, from the invention of the first integrated circuit (IC) to today's very large scale integration (VLSI) technology.

Introduction

The invention of transistor action (electrical signal amplification) in semiconducting material was a monumental accomplishment that has revolutionized the world. As with many inventions, the structure of the original invention has not only evolved, but has also led to new structures. The first demonstration of transistor action, the original point-contact transistor, was soon followed by the invention of the junction bipolar transistor. This second structure is viewed as the basis of modern microelectronics, because it laid the foundation for the concept of building an entire electrical circuit on a single piece of semiconducting material. It is interesting to recognize, however, that the junction bipolar transistor and the technology that was developed to fabricate it led to another type of transistor, the metal-oxide semiconductor (MOS) transistor. Both the theory of MOS transistor operation and the technology associated with its fabrication were derived from the classic junction bipolar structure and related research. Today, however, the MOS transistor is the structure primarily used in the continuing exponential growth of modern microelectronics.

Early Work on Bipolar Integrated Circuits

The dramatic technological revolution that occurred in electronics between 1948 and 1958 created a new world. With the invention of the junction transistor in 1948, the "killer" technology of the vacuum tube emerged. The elimination of filaments, with their high power consumption and low reliability, allowed electronics to be applied to almost every aspect of human life.

The existence of the junction transistor as a single-element device could not survive for very long. The new goal was to fabricate several transistors and connect them together on a single piece of semiconduct-

ing material, thereby creating an electrical circuit, now called the integrated circuit. It took just ten years for this to happen. In 1958 J. Kilby, employed at the research laboratories of Texas Instruments, Inc., demonstrated the first working bipolar integrated circuit. The concept of the integrated circuit created the "Silicon Age," filled with exponential growth in science, technology, and commerce.

Figure 1 shows a cross section of a junction bipolar transistor. Its electrical characteristics are primarily determined by the bulk (interior) properties of the semiconductor crystal. Therefore, extensive materials research and development was conducted to produce high-quality semiconductor crystals with extremely low levels of crystal defects and undesirable impurities.

After the initial demonstrations of the bipolar transistor and the integrated circuit, early attempts at reproducible fabrication clearly indicated that the chemical and mechanical treatment of the transistor crystal surfaces near the active electrical regions could vary the quality of the semiconductor devices. A surface passivation technology and its associated theory was needed. This led to extensive research into the physics of semiconductor surfaces.

During the 1950s, scientists were investigating the question of which semiconducting material would be most useful for fabricating general bipolar transistors. Two Group IV elements from the Periodic Table—silicon (Si) and germanium (Ge)—became the leading candidates, along with several Group III/Group V compounds—gallium arsenide (GaAs), indium phosphide (InPh), and cadmium sulfide (CdS).

Because of its electrical, mechanical, and thermal properties, Si emerged as the dominant material. Si had a unique property; it could be easily oxidized to form a smooth layer of silicon dioxide (SiO_2). This material acted as both a chemical diffusion barrier during device fabrication and a surface passivation material for electrical operation. The combined use of SiO_2 and Si was described by J. Hoerni[1] in 1960 and became known as the "planar process." During the early 1960s, a family of bipolar transistor products—called "transistor transistor logic" (TTL)—was designed and manufactured. These bipolar transistor products became the industry standard for system design.

Panel 1. Abbreviations, Acronyms, and Terms

A/D—analog-to-digital converter
CCD—charge-coupled device
CdS—cadmium sulfide
CMOS—complementary metal-oxide semiconductor
CMP—chemical–mechanical polishing
CVD—chemical vapor deposition
D/A—digital-to-analog converter
DRAM—dynamic random access memory
DUV—deep ultraviolet
EBES—electron beam exposure system
GaAs—gallium arsenide
Ge—germanium
I300I—International 300-mm Initiative
IC—integrated circuit
IGFET—insulated gate field-effect transistor
InPh—indium phosphide
MOS—metal-oxide semiconductor
MOSFET—metal-oxide-semiconductor field-effect transistor
PVD—physical vapor deposition
Si—silicon
$SiCl_4$—silicon chloride
SiN—silicon nitride
SiO_2—silicon dioxide
TiN—titanium nitride
TTL—transistor transistor logic
VLSI—very large scale integration

The Invention of the Si Gate MOSFET Transistor

The concept of the insulated gate field-effect transistor (IGFET), which predates the research on the junction bipolar transistor, can be traced back to the 1926 research of J. Lilienfeld[2] and the 1935 work of O. Heil.[3] Both attempted to create a device that used a capacitor structure to modulate the majority carriers in a semiconducting material.

A series of key events culminated in the demonstration of the first Si-based metal-oxide-semiconductor field-effect transistor (MOSFET). In 1955 I. Ross proposed the concept of the minority carrier MOSFET, and in 1960 M. Atalla proposed the Si-based MOSFET. The extensive research on the Si junction bipolar transistor also resolved many of the technological properties of SiO_2 and the Si/SiO_2 interface. Finally, in 1960, D. Khang and M. Atalla demonstrated the first Si-based MOSFET.

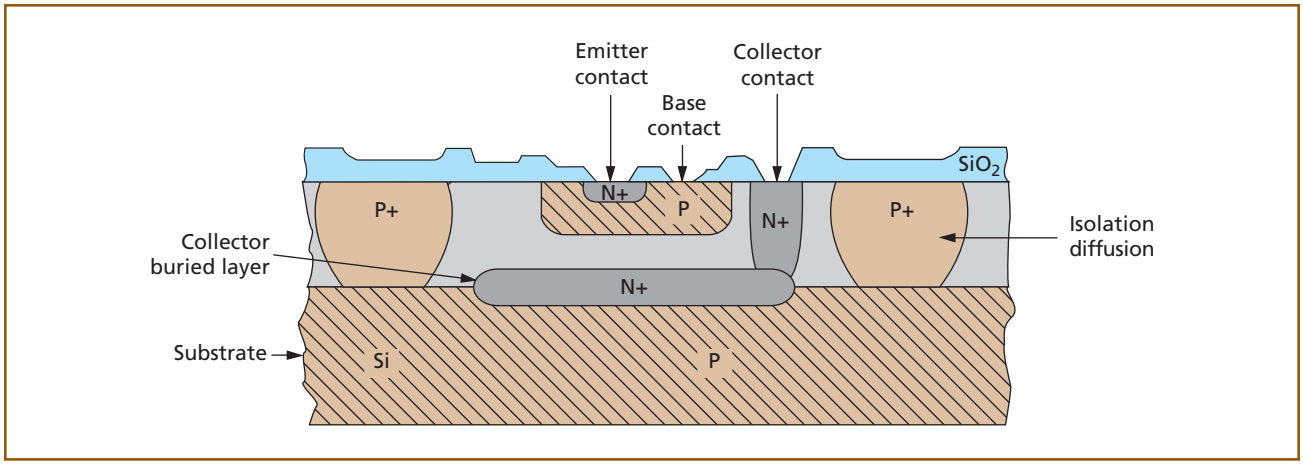


Figure 1.
The n/p/n junction isolated bipolar transistor.

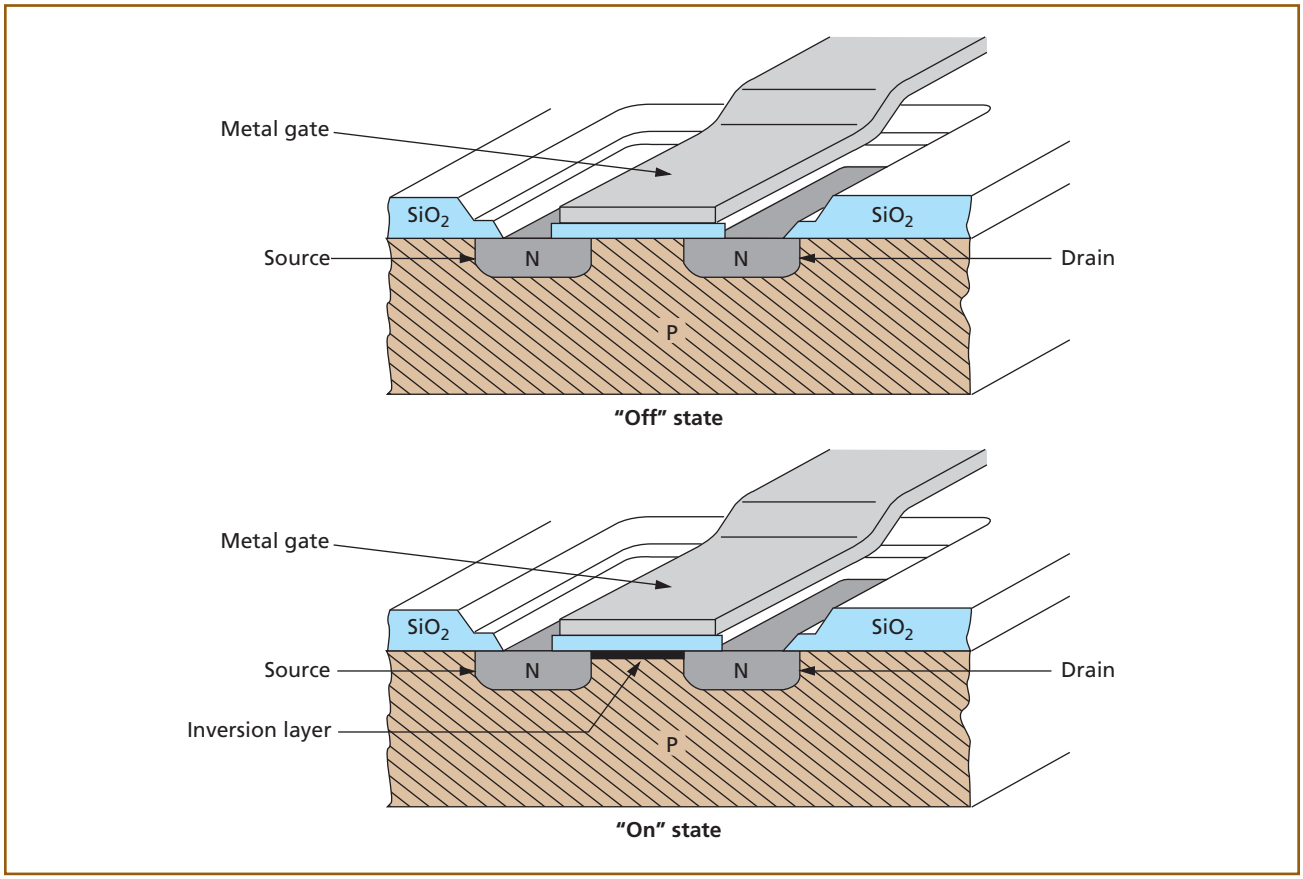


Figure 2.
"Off" and "on" states of the n-channel Si MOSFET.

The basic structure of the silicon MOSFET, as illustrated in **Figure 2**, is two isolated p/n junctions in a silicon surface, overlaid first with a thin SiO_2 insulator and then with a conducting metal layer. Applying a voltage to the top conducting metal layer (gate) modulates the electrical properties of the Si surface between the p/n junctions to electrically connect the n-type parts of each junction. These source and drain junctions then become the contacts for current flow in the transistor. Varying the gate voltage modulates the con-

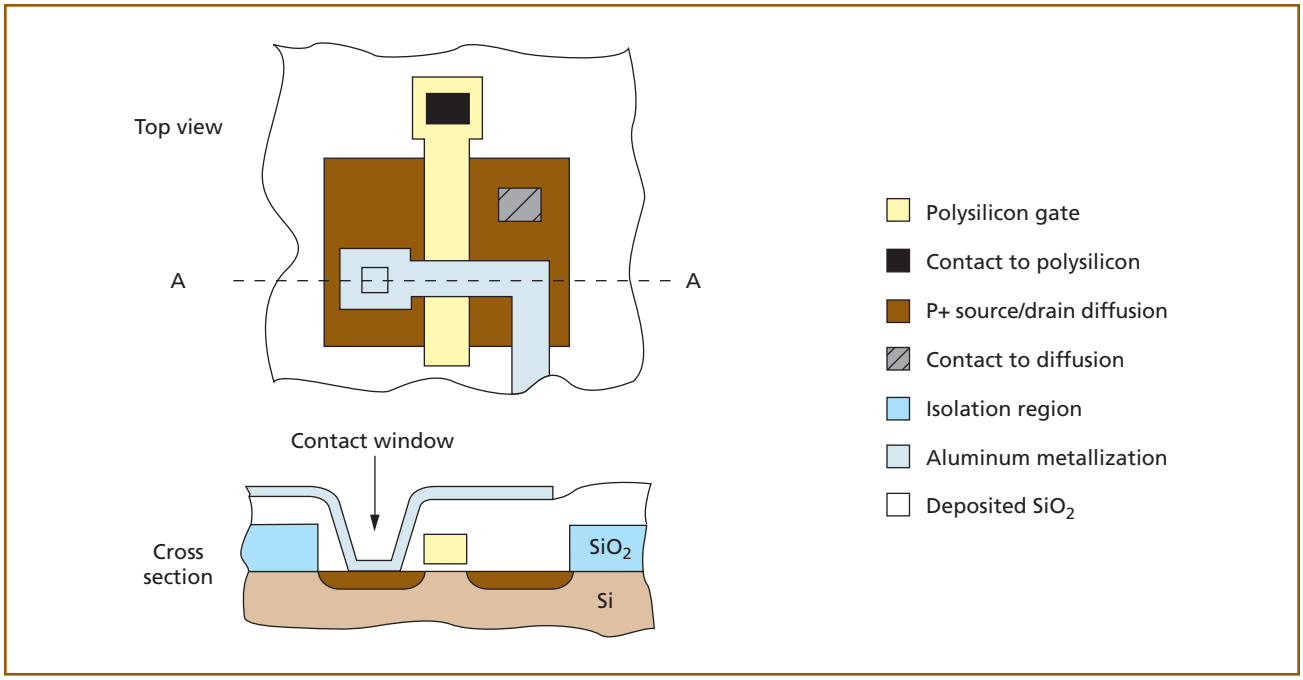


Figure 3.
The transistor structure of the p-channel Si gate.

ductance between the junctions, thereby amplifying the electrical signal on the gate. This type of silicon transistor was simple to build, and its manufacturability depended only on an electrically reproducible Si/SiO_2 interface.

During the next several years, the scientific community engaged in a major technological race to create the smallest, most cost-effective MOSFET, given the available materials, chemistry, and patterning capabilities. In 1967 the Si-gate MOSFET was invented. This device replaced the conducting metal gate of the earlier Si MOSFET with a layer of conducting polycrystalline silicon, a major technological advance for MOSFETs and their use in ICs. Polycrystalline silicon is a refractory material that allows high-temperature thermal processing to be conducted after the formation of the gate and also makes possible self-aligned source and drain diffusions (to the gate) and overcoating of the active transistor with high-temperature insulators. The metal interconnects and contacts could then be optimally placed to improve circuit density. With such a structure, a complex IC could be built with just four basic patterning steps. The landmark Si-gate MOSFET patent was finally granted to R. Kerwin et al.[4] of Bell Labs.

The first Si-gate MOSFETs were p-channel devices, as shown in **Figure 3**, with p-type source and drain regions in an n-type Si substrate. This structure was initially preferred because the Si/SiO_2 interface tended to have a net positive charge, which did not seriously affect the transistor and actually helped suppress deleterious surface effects exterior to the active device region.

Yield and Scaling Theory

In 1964 B. Murphy wrote a comprehensive paper examining the economic issues of IC yield and packaging.[5] He observed that, if a random defect were to occur during the process of fabricating an array of ICs on a single Si wafer, one of the ICs in the array would fail to function. Therefore, not all sites in an array would yield working ICs. Because all processes of fabrication were subject to random defects, the yield of good ICs would decrease exponentially with the size of the IC, thereby linking the concepts of yield and electronic function cost with defect density in manufacture. To fabricate increasingly larger and more complex ICs, the defect density would have to be decreased. What followed was the concept of ultraclean manufacturing technology.

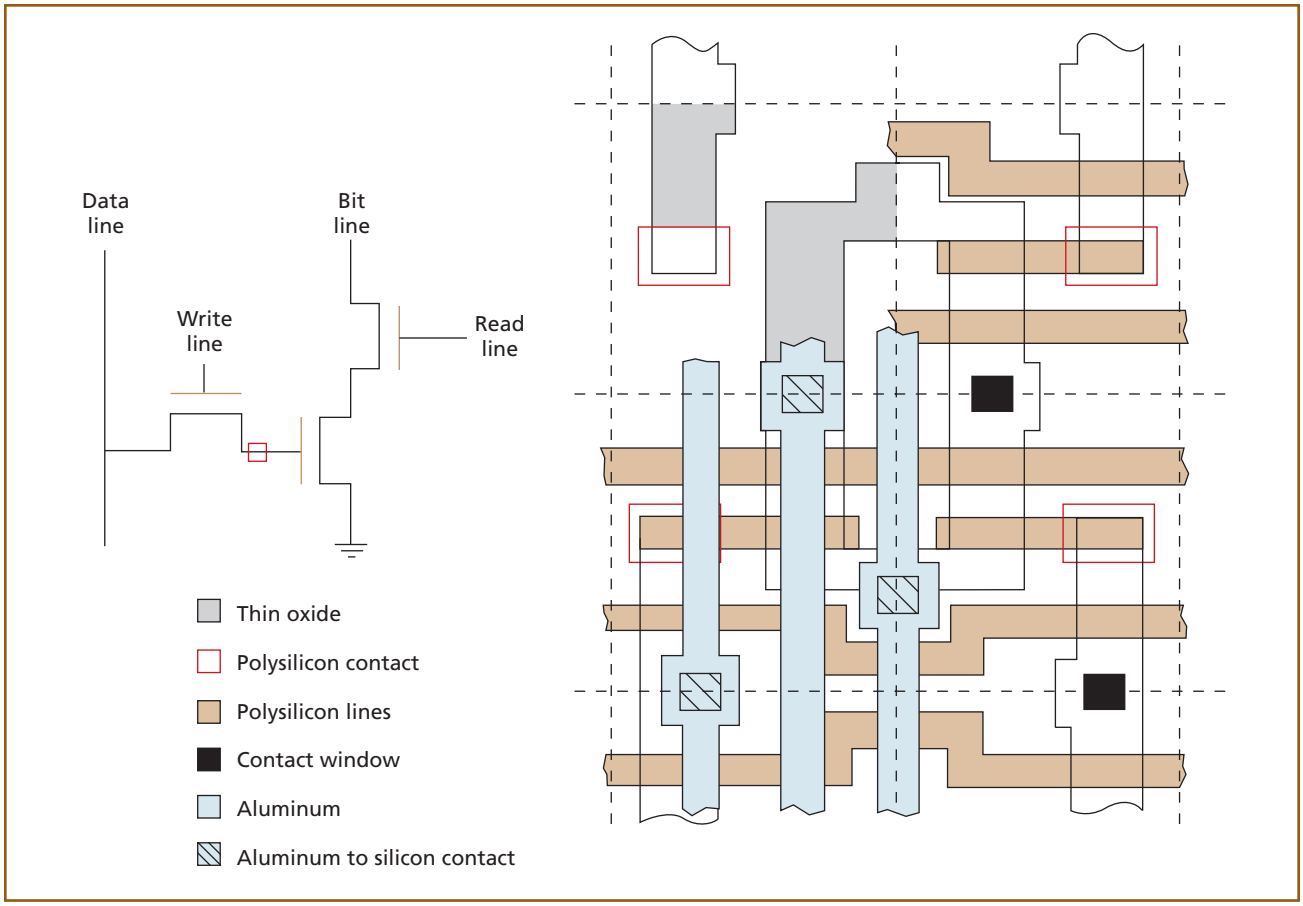


Figure 4.
Schematic and physical layout of the three-transistor cell.

In 1974 R. Dennard approached the question of the feature size used to manufacture ICs. To further reduce the cost per electronic function, it became obvious that smaller dimensions would produce smaller ICs and increased yield. His analysis of how MOSFET structures would evolve, as feature size decreased, led to his classic paper on device scaling, detailing the device physics of the MOSFET transistors and the resultant performance benefits.[6] By 1974 the basic technical and economic foundations for the exponential growth of the Si MOS IC industry had been established.

Growth of Si MOSFET Technology

From the late 1960s to the present (approximately thirty years), the Si MOS IC industry has been growing exponentially both in technical complexity and economic impact. About 1970, while many corporations were developing specific bipolar and MOS IC products, a small start-up company—Intel Inc., founded by R. Noyce, G. Moore, and A. Grove—introduced two generic IC products, built from a p-channel Si gate MOSFET IC technology. The first IC was a small 4-bit microprocessor, named the "4004," and the second was a memory circuit, the "1103." The 1103 memory circuit comprised 1,024 completely independent memory cells. Each cell contained three transistors, including a p/n junction, which was used to store charge. The memory states were considered to be either a "1" or a "0."

Figure 4 illustrates how four memory cells of a p-channel IC are constructed using the planar process. The upper left-hand memory cell in Figure 4 shows the first two masking layers, which form the active regions of the MOSFETs and a contact for a polysilicon gate to a drain in the Si substrate. The polysilicon features that form the active gates of the transistors and interconnects among the transistors are shown in the upper right-hand corner. The lower right-hand corner

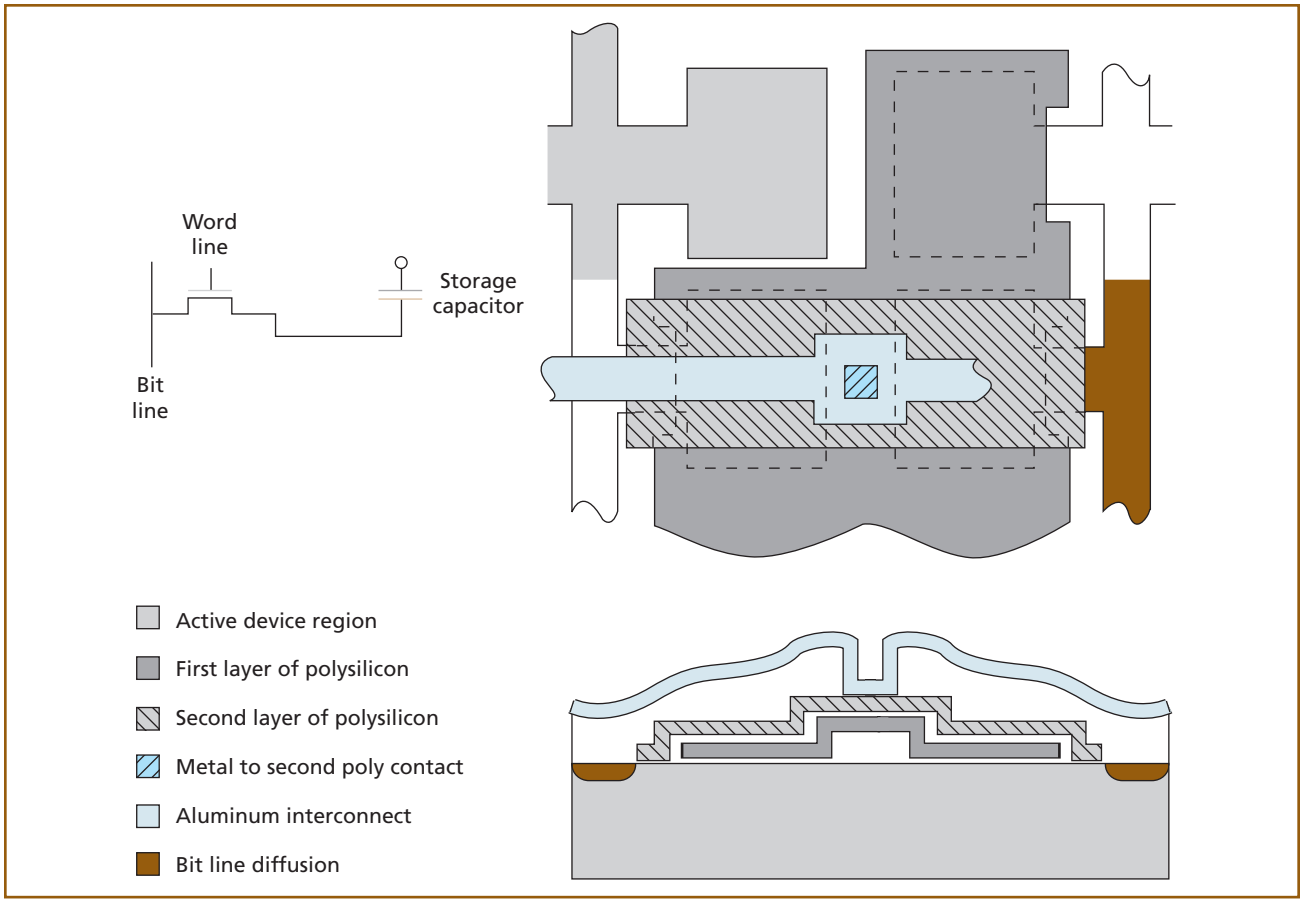


Figure 5.
Schematic and physical structure of the one-transistor cell.

shows the contact windows defined in the insulator, which overlays the polysilicon gates; the lower left-hand corner shows the metallization contacts and interconnects that complete the cell structure of the IC.

Because Si p/n junctions have a small current flow when reverse biased, the information in the cell has to be refreshed every few milliseconds. Although this time interval may seem short, it was very long in terms of the clocking frequency of the circuit, about 5 MHz. The 1103 memory circuit—called a dynamic random access memory (DRAM)—contained about 5,000 transistors and introduced the concept of large scale integration. The initial microprocessor and memory circuit became the fundamental building blocks of the modern computer and changed the world forever.

In 1974 Intel introduced a 4,096-bit DRAM, fabricated in n-channel Si-gate technology. The technological problems that had first limited MOS to p-channel structures had been overcome, and superior circuit performance followed. To allow higher packing density, the memory cell was changed from a three-transistor structure to a single transistor and a capacitor.

The designers of the 4K DRAM used a cell constructed from a double-layer poly-Si structure, shown in **Figure 5**. The double-layer structure was first developed for the fabrication of another important device structure, the charge-coupled device (CCD), a variation of the MOSFET. The CCD is the critical imaging IC device in most electronic video systems.

Several more generations of n-channel DRAMs followed, increasing the memory bit count by a factor of four every three years. Then, about 1980, the first high-performance circuits using Si-gate complementary metal-oxide semiconductor (CMOS) technology were introduced. In CMOS technology, both p-channel and n-channel transistors are fabricated on the same Si IC. L. Parrillo and R. Payne introduced a CMOS Si-gate process technology, called *twin tub* technology, and CMOS became universal.

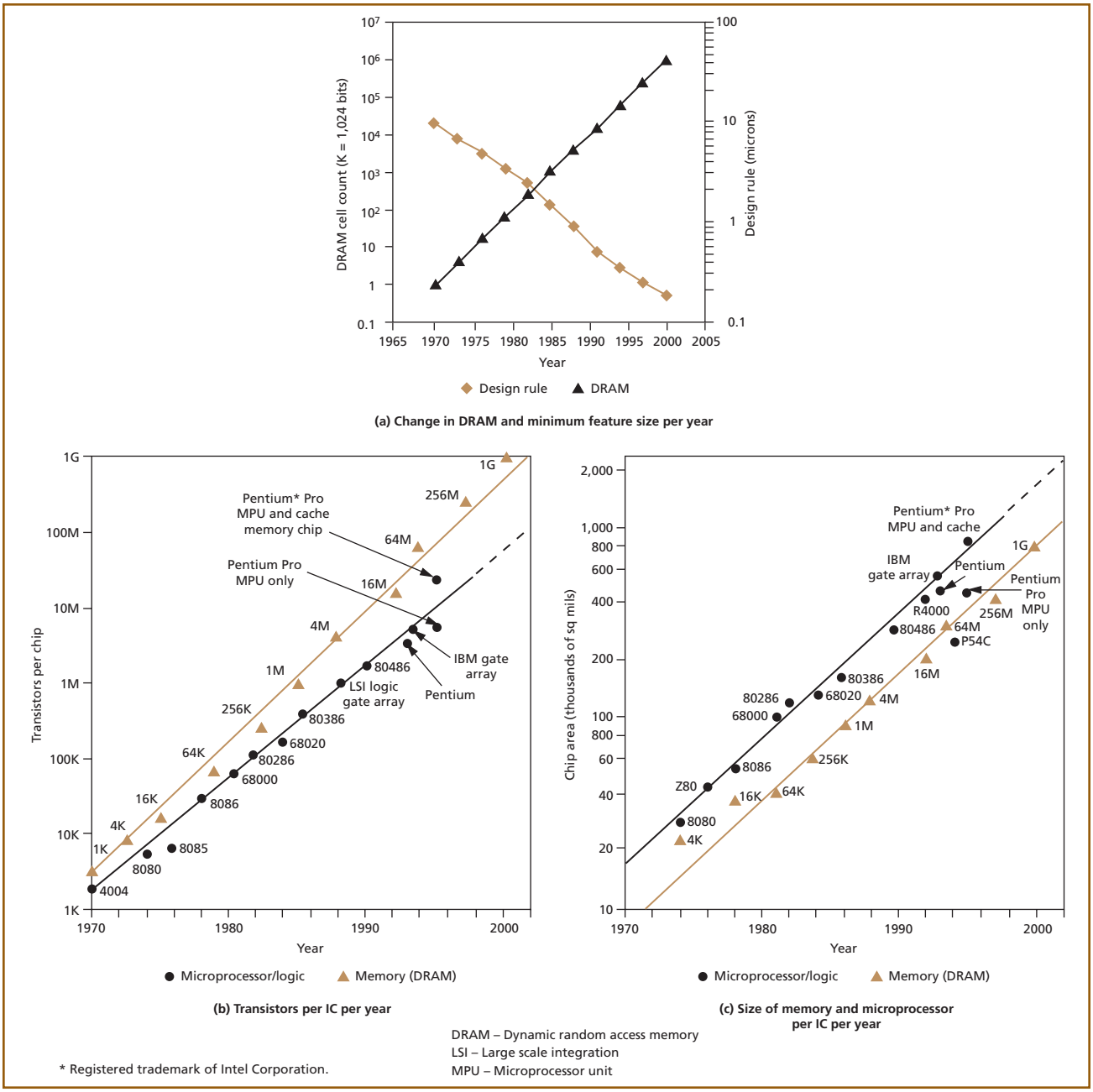


Figure 6.
Examples of the "Moore curve."

The ability to use complementary p-channel and n-channel transistors in circuit designs greatly reduced power consumption and simplified circuit designs. CMOS was quickly introduced into all memory and logic ICs, and by 1984 the first million-bit DRAM circuits were being fabricated. The era of VLSI began and the growth rate of DRAM circuit complexity continued at a factor of four increase every three years.

In the 1970s, G. Moore pointed out the general exponential growth of Si ICs, and the famous "Moore's Law" came into existence.[7,8] Among the various ways of plotting a "Moore curve," as illustrated in **Figure 6**, is a method that shows the DRAM storage increase and minimum feature size decrease as a function of time (see Figure 6a). Another method plots the increase in the number of transistors per chip for advanced ICs

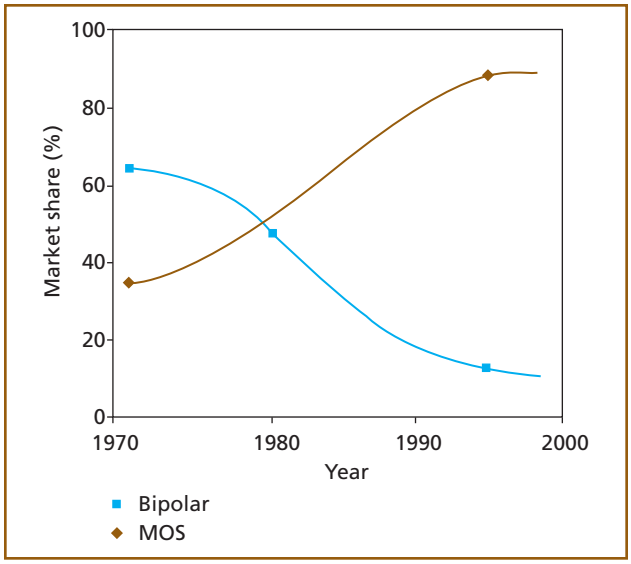


Figure 7.
Market share of ICs by technology.

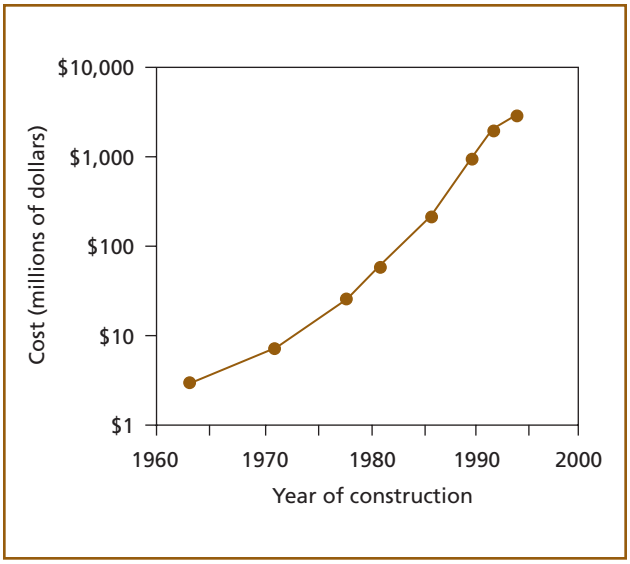


Figure 8.
Cost of IC manufacturing clean rooms as a function of time.

against time (see Figure 6b). A third method depicts the evolution of IC circuit size for DRAMs and logic-type ICs against time (see Figure 6c).

Slowly, but surely, during the past thirty years the semiconductor industry has migrated from using primarily junction bipolar IC technology to using MOS IC technology, as illustrated in **Figure 7**. The bipolar transistor laid the theoretical and technological foundation for creating the MOSFET and its many varieties of transistors. However, the benefits of reduced power consumption, lowered cost of manufacture per electronic function, and flexibility of device structure have made Si MOS the mainstream technology of modern electronics.

The World of VLSI

Today, as in the early 1970s, the Si MOS industry and its related products fall into two major categories: memory and logic. Each category, in turn, incorporates major families of products:

- Memory:
  - Dynamic random access memory,
  - Static random access memory, and
  - Nonvolatile random access memory.
- Logic:
  - Microprocessors,
  - Digital signal processors, and
  - Custom logic.

A third minor market segment for VLSI ICs is the broad class of analog and semi-analog circuits, such as analog-to-digital converters (A/Ds), digital-to-analog converters (D/As), and high-speed modems for PC interfacing to analog telephone networks. The final segments are niche markets, which incorporate power devices and high-voltage applications.

The major VLSI technology drivers—DRAMs and microprocessors—and their applications reside in the digital arena, because data acquired from our analog world is immediately converted into digital data that can be easily computed, compressed, transmitted, restored, error corrected, and converted back into an analog signal, if necessary. Modern electronics is a predominantly binary world, and digital circuits—in the form of memories and logic—perform all the storage and computational functions. Prime examples of this principle range from a wide variety of consumer products, to modern mainframe and personal computers, and, ultimately, to the digital worldwide telecommunications networks.

The VLSI IC semiconductor industry now exceeds $150 billion in sales and represents about 17% of the value included in all electronic equipment sales. To design, manufacture, and sell in this highly competitive industry, the "clean room" manufacturing facilities must be capitalized on the order of $1.0 billion increments, as shown in **Figure 8**.

The Present

This section reviews the development of the manufacturing technology of present day microelectronics, based on the "planar process." It describes silicon crystal technology, crystal dopant techniques, silicon oxidation development, lithography, materials deposition processes, pattern transfer mechanisms, metal interconnect technology, and material passivation technology.

Introduction

Today, the manufacture of a leading-edge IC is an extremely complex procedure, as shown in the sample VLSI IC in **Figure 9**, a photomicrograph of a typical VLSI IC circuit—a modern digital signal processor. The circuit design and the electrical performance of such an IC are intimately linked to the technology of IC fabrication through the electrical properties of the active transistors, as well as the parasitic electrical components of resistance and capacitance associated with the materials and processes used to construct the IC. With respect to the design and manufacture of leading-edge products, such as DRAMs and microprocessors, an element essential to the success of the final IC is the effective communication process that must take place between the design and technology research and development teams.

Today, 0.25-μm CMOS technology is being introduced into manufacture by the major semiconductor corporations on an international basis. Active development is also under way on the next-generation manufacturing technology, 0.18-μm CMOS process technology, scheduled for mass production in the year 2000. Variations of it will be used to fabricate DRAMs and logic. It is important to understand, however, that many of the materials and processes used to fabricate the wide variety of ICs are generic to all types of circuits, and thereby form the core of a given generation of technology. The sections that follow describe the materials and processes that are used to fabricate a modern IC.

The Planar Process

An earlier section of this paper referred to the "planar process." **Figure 10** illustrates this concept with a cross section of a modern VLSI IC structure.

The IC structure is fabricated on a silicon crystal substrate by a process of successive sequences that, in general:

1. Deposit a specific material or layers of specific materials,
2. Generate a desired lithographic pattern array on the Si wafer surface,
3. Perform a transfer process,
4. Remove the lithographic patterning material, and
5. Prepare the surface for the next processing sequence.

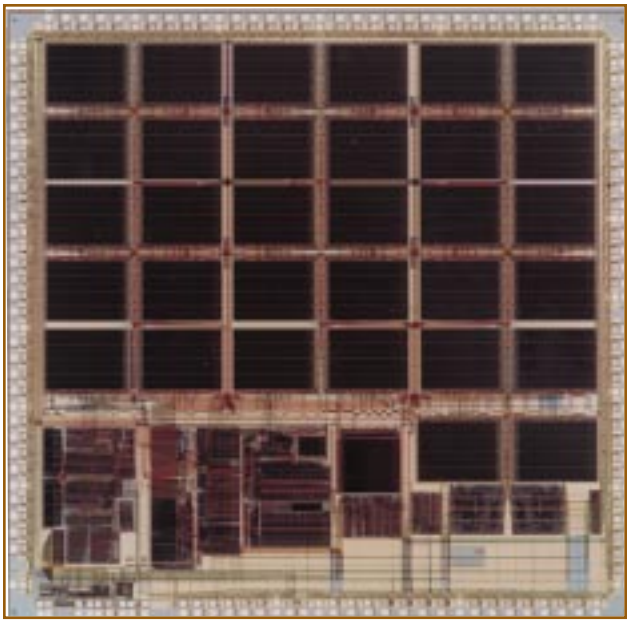


Figure 9.
A modern VLSI circuit—a digital signal processor.

Figure 11 is a photograph of a typical 8-inch-diameter Si crystal substrate. An array of VLSI ICs is formed on the wafer. When device fabrication is finished, the wafer is cut into the individual ICs by a very thin diamond saw (about 0.003-inch thick). The individual working ICs are packaged using a wide variety of techniques, depending on their final application.

It is customary to outline the VLSI process according to the patterning levels in the overall sequence of fabrication. **Table I** lists the primary levels being developed for the 0.18-μm CMOS technology.

Si Crystal Technology

All Si VLSI technologies start with the fundamental material, a silicon crystal. Many excellent references relate the history of the development of Si

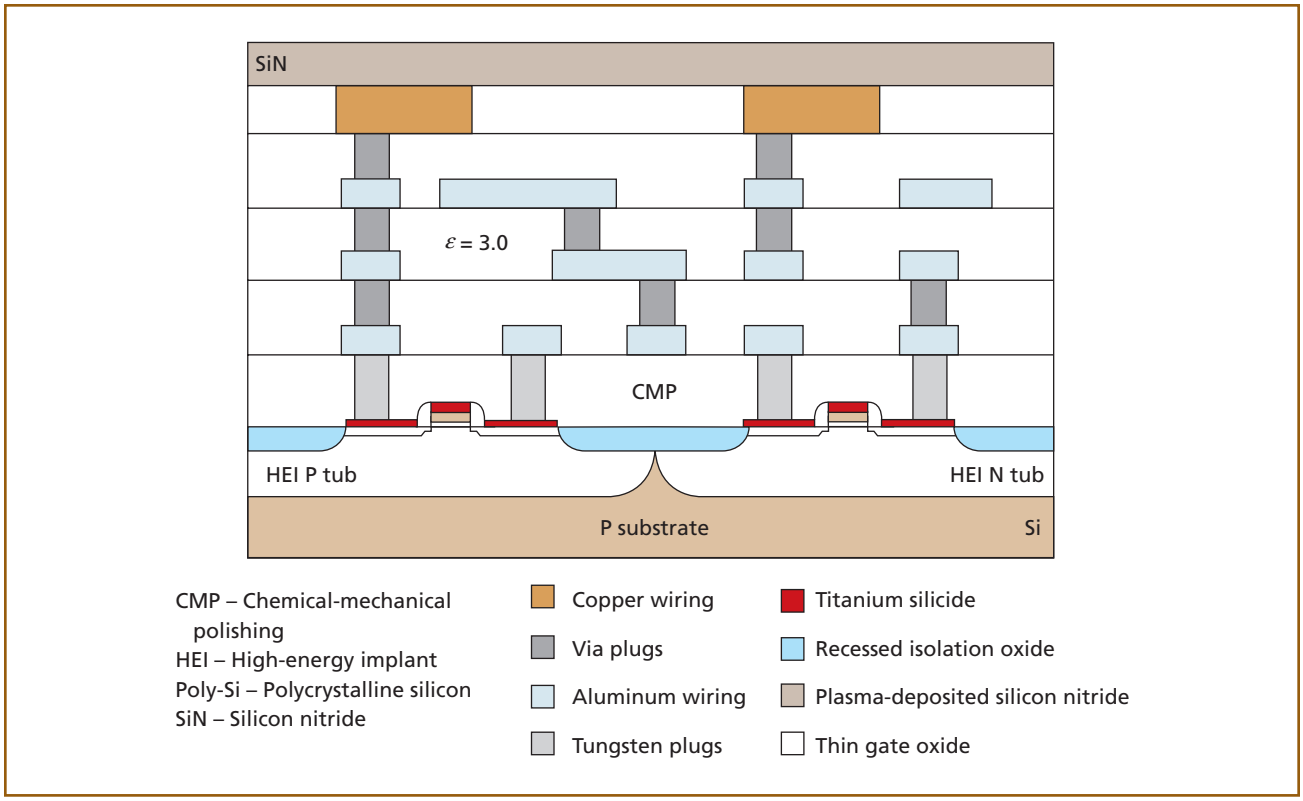


Figure 10.
Cross section of 0.18-μm VLSI CMOS technology.

crystals used to fabricate ICs.[9] Today, the principal method of growing a large silicon crystal is the Czochralski technique.[10] The process has undergone continual improvement and refinement, and the diameters of the crystals have increased steadily over the years, as shown in **Figure 12**. The process, however, remains fundamentally the same.

A small seed crystal of Si is used to draw a single cylindrical crystal of Si from a quartz crucible filled with molten Si. The seed crystal is inserted into the molten silicon and then rotated and slowly withdrawn from the bath, producing a pure, essentially defect-free crystal. The rotation and withdrawal rate determine the diameter of the crystal, and the fracture strength of the seed crystal ultimately defines its length. This is an important issue, because as the diameter of the crystal is increased to improve overall VLSI IC production efficiency, the length of the crystal decreases with the square of the diameter. This significantly reduces the total number of wafers produced per crystal.

The molten Si is created from a high-purity poly-

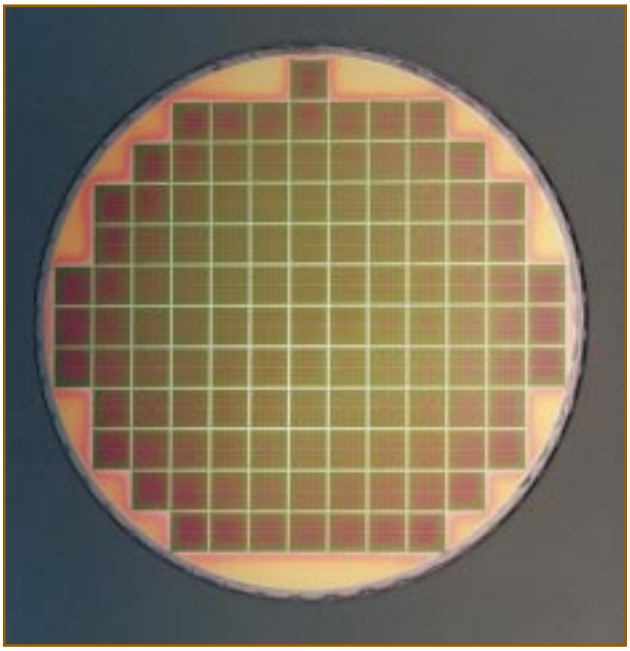


Figure 11.
A fully fabricated 8-inch Si wafer.

Table I. Photolithographic patterning levels for 0.18-μm CMOS technology.

Patterning level	Description
1	Thin oxide regions
2	Tub regions = p type
3	Tub regions = n type
4	Selective threshold voltage adjust = n channel
5	Selective threshold voltage adjust = p channel
6	Polysilicon doping = n type
7	Polysilicon doping = p type
8	Polysilicon gate definition
9	Lightly doped drain = n-channel transistor
10	Lightly doped drain = p-channel transistor
11	Source/drain doping = n channel
12	Source drain doping = p channel
13	Source/drain contact window
14	Window doping = n type
15	Window doping = p type
16	Metal 1 definition
17	Metal 1—Metal 2 via definition
18	Metal 2 definition
19	Metal 2—Metal 3 via definition
20	Metal 3 definition
21	Metal 3—Metal 4 via definition
22	Metal 4 definition
23	Metal 4—Metal 5 via definition
24	Metal 5 definition
25	Passivation vias

crystalline Si charge, produced using a sophisticated process of chemically reducing silica (sand) into silicon. Compounds of silicon are formed—such as silicon tetrachloride ($SiCl_4$)—and purified through chemical distillation. The silicon compounds are then reduced to form the highly pure polycrystalline charges. To maintain purity, the polycrystalline Si charge is melted by induction heating. To eliminate any impurities, the charge has to be placed in a high-purity SiO_2 (fused silica) crucible. Silicon melts at about 1,415°C, and at this temperature molten silicon will react with most materials. As the crystal grows, specific chemical elements may be added to the silicon melt to achieve the proper electrical characteristics—n-type or p-type silicon. This is called *doping* the crystal.

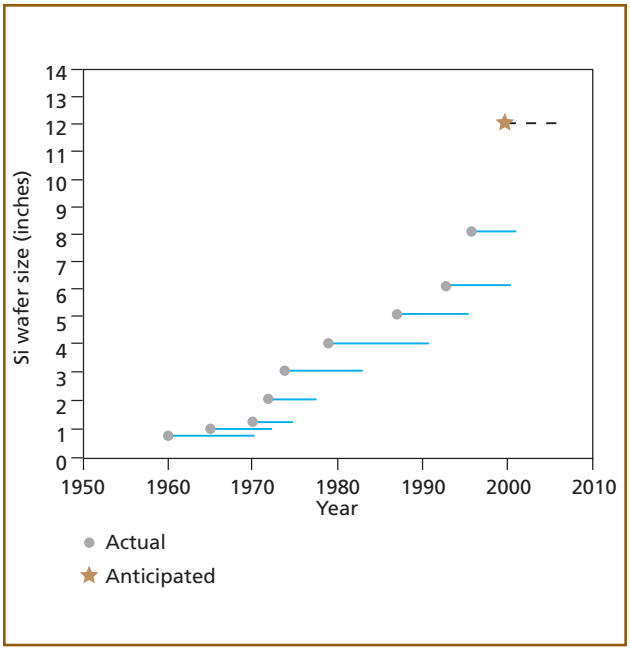


Figure 12.
Wafer size as a function of time.

The common dopant elements are:

- For p-type silicon: boron, aluminum, gallium, and indium; and
- For n-type silicon: phosphorus, arsenic, antimony, and bismuth.

In n-type silicon, electrical conduction is associated with the motion of free electrons; in p-type silicon, conduction is associated with "holes," which are missing free electrons.

Figure 13 illustrates the process of fabricating crystals. The silica crucible itself is a primary source of contamination—oxygen. During the crystal pulling period, the interior silica surface slowly dissolves, introducing oxygen into the molten Si bath and the final crystal. While oxygen is soluble in silicon at very low levels (about $5.0e10^{17}$ atoms per cm^3), the oxygen concentration has to be carefully controlled, not because it affects the electrical properties of the silicon, but because it can supersaturate the crystal as it is being formed, creating internal SiO_2 precipitates and crystal defects.

After the crystal is cooled, it is cylindrically ground

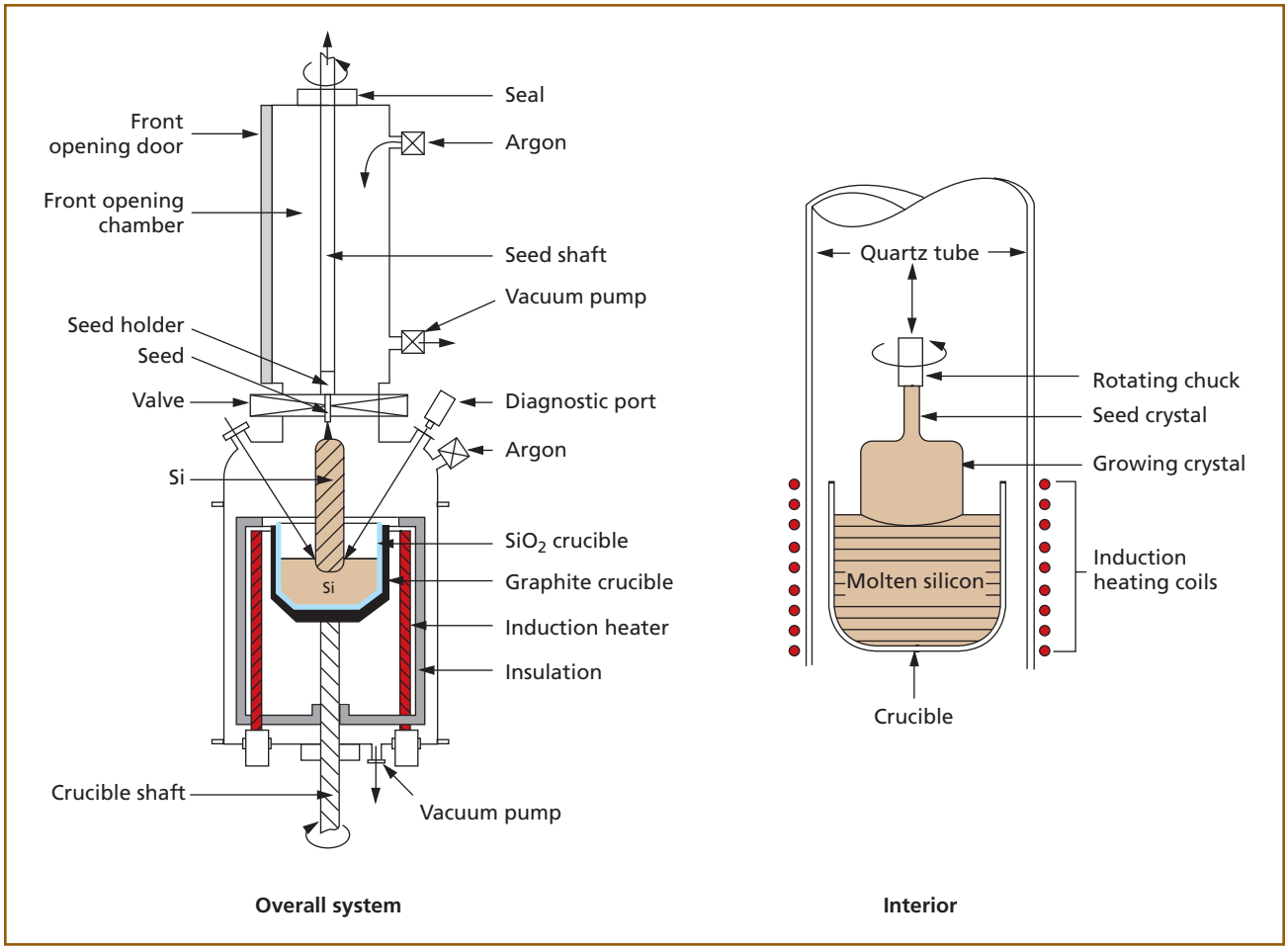


Figure 13.
Growth apparatus for Si crystals.

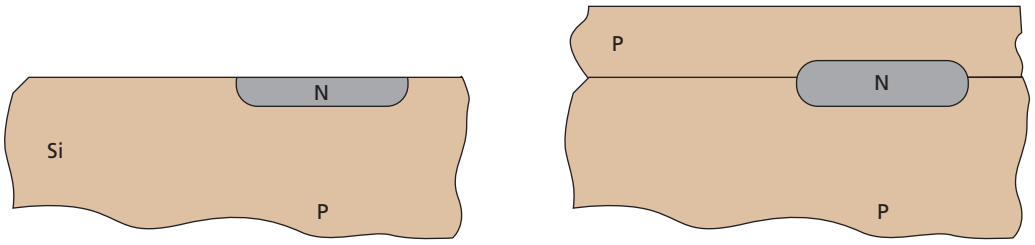
to specified dimensions, sliced very carefully with a diamond saw along the desired crystal plane, and formed into circular wafers. These wafers are then etched and polished to remove any crystal damage created by the grinding and slicing processes. Finally, one side of the wafer undergoes a chemical–mechanical polishing (CMP) process that essentially renders it atomically smooth. The silicon wafer is then ready for the "planar process" of forming ICs.

To achieve a desired impurity profile, another silicon growth process—called *Si epitaxial growth*—may be performed. In this process the Si wafers are heated in a sealed chamber. Specific gases, such as silane (SiH_4), dichloro-silane (SiH_2Cl_2), or $SiCl_4$—diluted in a nitrogen/hydrogen carrier gas mixture—are passed over the wafer. Impurity gases—such as phosphine (PH_3), arsine (AsH_3), and diborane (B_2H_6)—may also be added to determine the impurity level in the growing layer. By specifically balancing the overall chemical reaction, a thin layer of precisely doped silicon can be crystallographically grown on the surface of the substrate silicon wafer, as shown in **Figure 14**.

Silicon Oxidation Technology

Probably the most unusual feature of silicon is its ability to oxidize. The oxidation phenomenon has been extensively studied and documented by M. Atalla,[11] B. Deal and A. Grove,[12] and also by J. Ligenza.[13] Silicon can be oxidized in either dry oxygen (O_2) or pure steam (H_2O) over a wide range of gas pressures and temperatures. Thermal SiO_2 can be grown in very uniform thicknesses, and the growth process creates an almost atomically smooth interface.

At least forty years of research and technology



Epitaxial Si grown over an Si wafer with a patterned impurity profile, a common process in bipolar technology.

Figure 14.
Cross section of epitaxial Si growth on a bipolar Si substrate.

development have enabled manufacturing processes to grow thermal oxide films with very low defect density at thicknesses ranging from 2.0 μm (10^{-6} meters = 1.0 μm) to 2.0 nm (10^{-9} meters = 1.0 nm.). A 2.0-nm film is approximately 7 atomic layers thick.

Initially, silicon oxidation proceeds in a linear fashion, with the growth rate determined by the oxidation reaction rate at the Si/SiO_2 interface. As the oxide layer becomes thicker, the growth rate is controlled by the diffusion of the oxidizing species through the SiO_2, to the Si/SiO_2 interface. After the oxide is grown to its desired thickness, it can be annealed in either a neutral gas, such as argon, or chemically active gases, such as nitrogen or hydrogen. Technologically, a properly annealed Si/SiO_2 interface essentially will be perfectly atomically matched, chemical bond to chemical bond. A residual number of excess Si bonds will exist, however, on the order of 10^{+9} to 10^{+10} per cm^2. These represent approximately one unpaired bond for every 10^{+5} paired bonds. At this low level, transistor characteristics are no longer influenced, and ideal MOSFET device characteristics are obtained.

In the early 1980s, E. Poindexter and his coworkers[14] performed the definitive work that showed that active Si interface states consisted of excess Si 2P orbital bonds, which had three possible electronic charge states— +1, 0, or -1.

Silicon oxidation incorporates two interesting mechanisms. First, the oxidation mechanism creates interstitial, or "free," Si atoms that diffuse into the Si crystal. H. Shiraki[15] found that if the Si surface oxidizes too rapidly, a large fraction of the Si interstitial atoms cannot diffuse away from the surface fast enough and, instead, will aggregate and form crystal defects. Called *stacking faults*, these defects can be detrimental to final electrical device operation. Later diffusion studies showed that excess silicon interstitial atoms can also affect dopant diffusion rates by electronically coupling with the dopants and affecting their diffusion rates in the silicon crystal.

As the oxidation proceeds, the dissolved oxygen in the Si crystal diffuses to the continuously restructuring Si/SiO_2 interface and reduces the oxygen concentration in the top surface of the Si crystal. A *denuded zone* is formed, and this can be very beneficial to the quality of devices formed in the Si surface.

Lithography

Lithography, a complex process used to produce an IC pattern, has evolved considerably since the early 1960s. The lithographic process has two major components: the production of the masks, which are used to produce the patterns on the silicon wafer as it is processed; and the actual technology of printing the patterns on silicon wafers.

From 1960 to 1970, ICs contained few elements, making it possible to manually produce a drawing of each layer used in the fabrication process. The drawing was photographed to produce a master reticule used in an optical reduction camera to print an array of each layer on a master glass plate. The master plate was then reproduced, and production quantities of masks were made for the wafer fabrication process. A typical working mask was used from 25 to 50 times. During each printing, the mask was pressed against the silicon wafer to ensure accurate pattern reproduction. Because of repeated physical

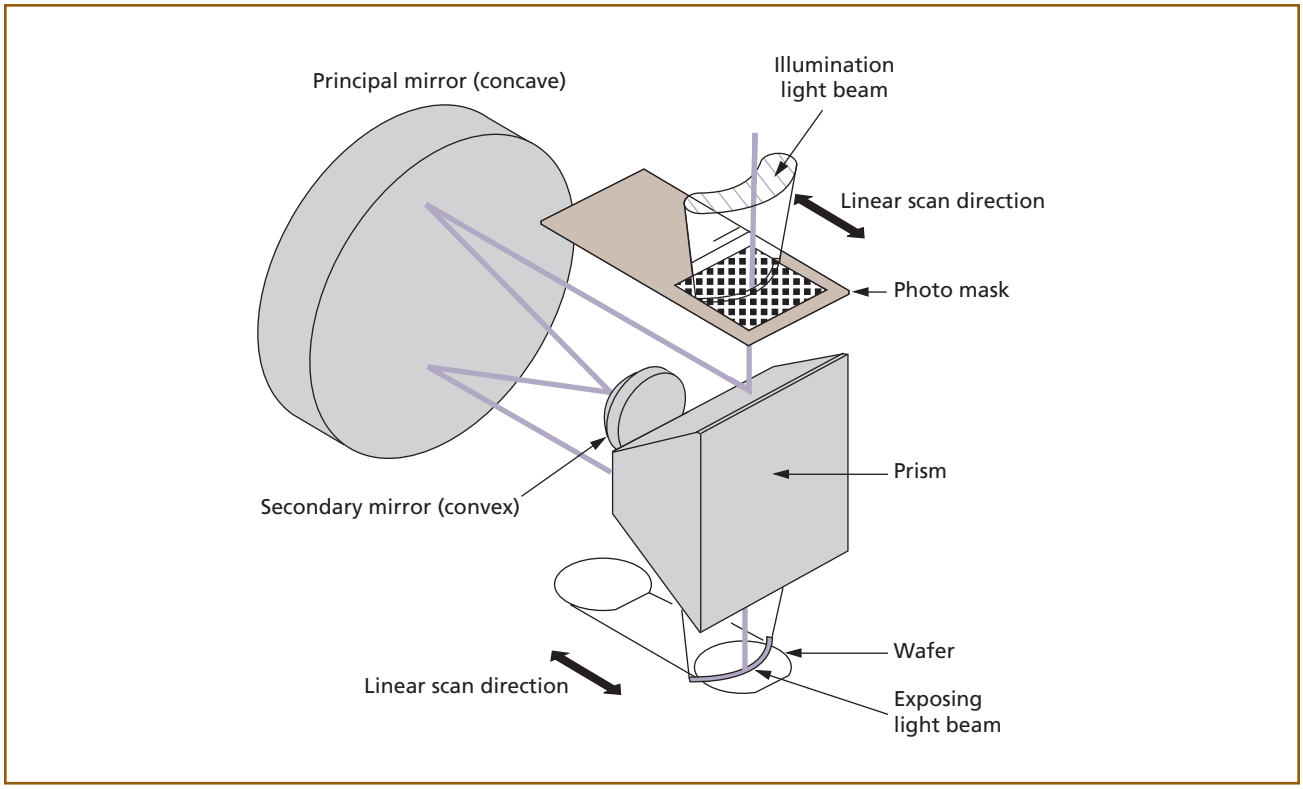


Figure 15.
Optical system of a scanning projection printer.

contact with the wafer, the mask became so contaminated with defects that it had to be discarded.

In the late 1960s, the complexity of ICs grew, making it exceedingly difficult to manually produce each master drawing. Clearly, a new technology was needed. In the early 1970s, D. Herriott led a team of scientists and engineers who designed and built the first computer-controlled mask writing machine.[16] This machine, known as an electron beam exposure system (EBES), focused a beam of electrons into a small circular spot (about 1.0 μm). Using electrostatic and magnetic deflection lenses, the beam could then be moved over a surface to an exact location. With such a machine, it became possible to encode each IC patterning level in a digital format, store it in a computer format, and then feed the information into EBES for direct writing of a pattern layer onto the mask reticule, or the master mask. EBES became an industry standard; it has been extensively refined during the past twenty-five years, but it still remains the basic machine for all present-day mask fabrication.

To complete this electron beam technology, new organic materials were researched and developed. These materials, which became soluble after exposure to electron radiation, were named electron beam resists. Pioneering work in this area was conducted by L. Thompson and his coworkers at Bell Labs.[17]

The next major advancement in lithography was the development of the projection printer, shown in **Figure 15**. The basic concept was to project an image of the mask onto the silicon wafer's surface without physically touching the surface with the mask. As a result, manufacturers were able to dramatically reduce the defects on a silicon wafer and eliminate the production of thousands of working masks. Both actions greatly reduced the cost of IC manufacture.

The first projection printing machine, developed by the Perkin-Elmer Corporation, came into widespread use in the mid-1970s. Using a ringfield scanning mode, it projected the master mask image onto a wafer with unity magnification and could print more than 60 wafers per hour.

By 1980, Perkin-Elmer dominated the lithographic exposure tool industry. However, another "killer" technology was being introduced. The GCA Corporation had also developed a projection machine. The new machine was a "step and repeat" tool that projected the image of the master reticule directly onto the wafer. The critical element in the stepper was a high-quality refractory lens with 5X reduction. As steppers became the new industry standard, they were manufactured by several major corporations, including GCA, Nikon, Canon, and Ultratech.

In partnership with Perkin-Elmer, IBM researchers developed the next-generation tool, which combined stepping and scanning. Modern versions of the step and scan system are now manufactured by several major corporations, including SVGL, Nikon, and Canon.

Advances in lithography resolution were made in various ways. In addition to mechanical and optical improvements in the printing machines, the photosensitive emulsions that were applied to the wafer for the initial imaging were extensively improved. At first, materials were borrowed from the newspaper printing industry, but they lacked the resolution needed for IC features. The research and development of photoresist materials became an international technical issue. The chemistries involved, which are extremely complex, are described in detail by W. M. Moreau.[18]

The third area of improvement in lithography was research and development in the wavelength (λ) of the exposing light. To manufacture silicon wafers in high volume, it was convenient for the exposing wavelength to be in the ultraviolet range. High-pressure, high-intensity mercury light sources were available, and the lithography industry concentrated its research and development efforts at the "G-line" (λ = 432 nm) of the mercury light spectrum. This approach was viable, but researchers began to explore submicron dimensions for fabricating MOSFETs (L > 1.0 μm). Using G-line light, basic optical theory limits printing resolution to about 0.50 μm. In the early 1990s, to print 0.35-μm feature sizes, the lithography industry was required to make an intermediate shift in exposure wavelength to the "i-line" of mercury light (λ = 365 nm).

In the early 1980s, however, a team of researchers at Bell Labs designed and built the first deep ultraviolet (DUV) optical stepper, using a krypton fluoride laser as the light source (λ = 248 nm). Today, DUV step and scan tools and associated photoresist materials are emerging as the production lithography process for 0.25-μm IC technology.

Advances in optical lens materials, optical imaging techniques, mechanical tool design, and organic photoresist materials are now required to emerge as rapidly as all other aspects of the IC technology. Exposure systems and resist materials based on argon fluoride laser illumination (λ = 193 nm) are now under active research and development for the manufacture of 0.18-μm CMOS technology.

Materials Deposition Technology

During the fabrication of an IC, many process steps require the deposition of specific materials, from metals to insulators. Their deposition must be uniformly controlled in chemical composition, mechanical properties, thickness, and defect level over the entire wafer.

The deposition processes fall into two major classes: the chemical vapor deposition (CVD) technique and the physical vapor deposition (PVD) technique. Each class subdivides into subclasses that require particular deposition methods for each material.

In the major field of CVD, a chemical reaction takes place during the deposition. Reactant components, in a gas phase, are brought together in a reactor, and the reaction usually proceeds in a heterogeneous manner. In a heterogeneous gas reaction, the active compounds react selectively on the surface of the wafer, and, possibly, on the interior surfaces of the reactor chamber. A homogenous gas reaction is avoided, because it leads to particle buildup in the gas phase and, ultimately, to deposition of these particles on the surface of the wafer. During subsequent process steps, these particles will become defect sites and severely limit the IC yield. Many CVD processes are thermally activated, and the chemical reactions need to be carefully characterized to ensure that the process is optimized.

Another type of CVD process is performed via plasma deposition chemistry. This process creates a gas

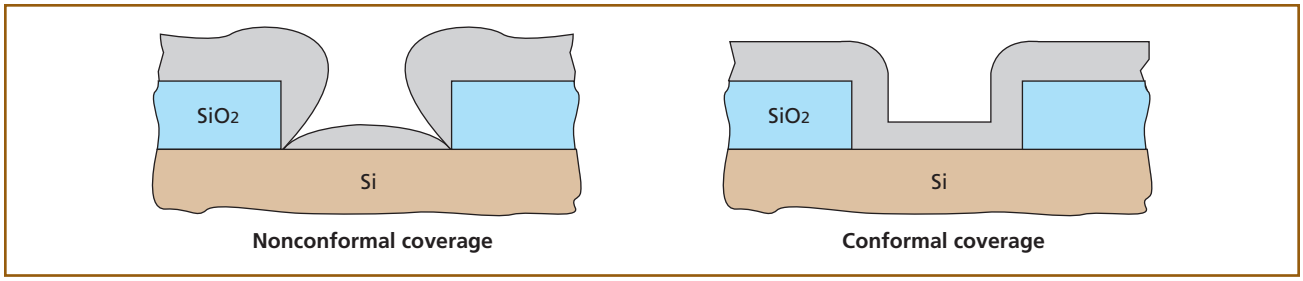


Figure 16.
Conformal and nonconformal step coverage.

plasma, such as nitrogen or argon, into which reactant gases are introduced. After the gas molecules are ionized and fractionated into various radicals, the reaction (recombination of radicals) occurs on the wafer surface and, possibly, on the chamber walls. The reactions and subsequent materials properties depend on the wafer temperature and the plasma (including such dependent variables as plasma density, radio-frequency power, DC bias, and chamber geometry).

An important consideration of CVD processes and the materials deposition is the degree of uniformity, or *conformal coverage*, that is achieved on the silicon wafer surface during deposition, as shown in **Figure 16**. CVD processes are carefully characterized with respect to molecular surface mobility, the resultant degree of conformal coverage, and the mechanical stress resident in the deposited films. If the film stress is highly tensile, films will crack after a given thickness is deposited. On the other hand, if the stress is highly compressive, the deposited film can delaminate from the silicon wafer surface. Typical materials that can be deposited by CVD for IC fabrication include polycrystalline and/or amorphous silicon, silicon dioxide (SiO_2), glasses (phosphosilicate and borosilicate), silicon nitride (Si_3N_4), titanium nitride (TiN), tungsten (W), and aluminum (Al).

In the major field of PVD materials processing, deposition involves physically moving the material from a source and depositing it uniformly on the wafer surface. One of the earliest examples of PVD processes was the evaporation of metal films. Typically, a metal charge of aluminum was heated in a vacuum chamber, and the evaporated aluminum coated the entire wafer surface. The methods of heating the aluminum were electron guns, induction heating, and filament evaporation.

The electron gun system is no longer used, because the x-rays it created caused chemical bond breaking in SiO_2 and electrical damage to the active device structures. An important discovery arose, however, from the use of electron guns. In this system, the aluminum charge resided in a water-cooled copper holder. As the aluminum evaporated, the copper slowly alloyed with the molten aluminum during deposition and was incorporated into the deposited aluminum film, creating a copper concentration of about 0.4%. Technologists discovered that aluminum deposited in this fashion was much more reliable than pure aluminum. Today, aluminum alloys containing 0.4% copper are still routinely used.

The old PVD systems have now been almost completely replaced by plasma sputter deposition systems. In these systems, a small plasma of argon or nitrogen is created near the material source. The gas ions hit the target and vaporize the material by molecular collision. Proper engineering of the targets and the vacuum system geometry enable the final material to be uniformly deposited on the silicon wafer.

PVD has one potential disadvantage. The deposited material usually does not have enough energy and surface mobility to uniformly cover a steep topology. In modern CMOS technology, device structures may have aspect ratios on the order of 2 to 1. The non-uniform coverage of materials can lead to failures in manufacturing or, in the worst case, decreased reliability. Typical problems associated with PVD processes are incomplete material coverage of steep walls, as shown in **Figure 17**, and failure to act as a continuous materials and/or barrier layer.

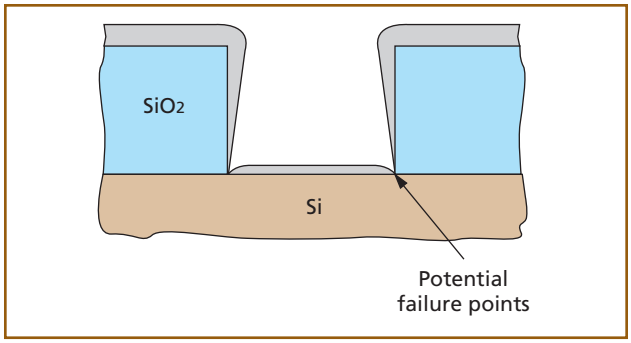


Figure 17.
Poor materials step coverage by a PVD process.

Pattern Transfer from Photoresist Material into Device Materials

In the process of fabricating ICs, the pattern is transferred to the materials on the silicon wafer by etching, as shown in **Figure 18**. Initially, ICs had rather large horizontal dimensions—on the order of 10.0 µm—and the films to be etched were on the order of 0.50 µm, as shown at the top of Figure 18. A wet chemistry technique, which has many beneficial aspects, was used to perform the early patterning. The etchant chemicals can be produced with extremely high purity, interact with the specific material on the silicon wafer at the atomic level via a chemical reaction, and consequently show very minor geometrical effects or residual contamination. Chemicals such as phosphoric acid, hydrofluoric acid, hydrochloric acid, nitric acid, and potassium hydroxide were and are still commonly used in modern silicon processing. Because of environmental concerns, many of these chemicals are either recycled or neutralized for safe disposal.

Using wet chemicals for pattern transfer has a major drawback, however. The wet chemicals will etch the material in an isotropic manner (see Figure 18), undercutting the masking material. With present lithographic geometries on the order of 0.35 µm, isotropic undercutting will completely eliminate the pattern. Feature size control became a major issue in the 3.5-µm VLSI technology, and researchers began working on methods to eliminate the undercut.

At the same time, scientists were conducting research on using plasmas to etch materials. Their major goal was to eliminate the inconveniences that extensive wet chemistry brought to the manufacturing facility. In one of the first applications of plasma etching, scientists used oxygen plasma to strip organic photoresist layers from silicon wafers. At that time, most wet strippers contained biphenyl compounds, which were found to be carcinogenic. Technologists found that by adding certain chlorinated or fluorinated chemicals to the etching plasma, they could achieve an anisotropic etching effect, as shown at the bottom of Figure 18. Analysis indicated that depositing etchant byproducts on the sidewalls of the feature edges as the material was being etched inhibited lateral etching. The solution to vertical pattern transfer had been discovered. For each material to be etched, technologists had to develop a specific chemistry and a set of plasma operating conditions. However, complex plasma etching enabled IC technologists to con-

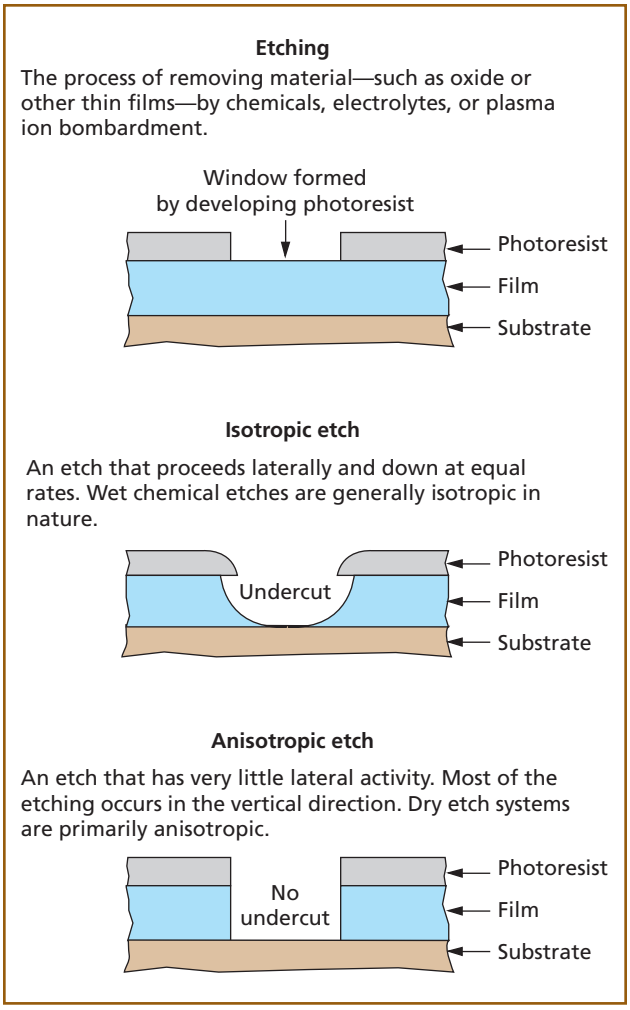


Figure 18.
Pattern transfer.

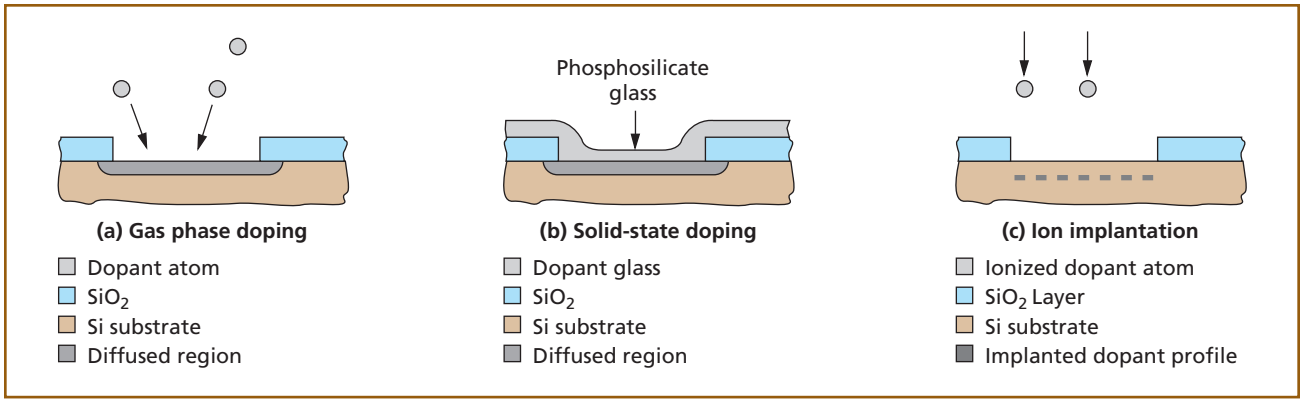


Figure 19.
Doping techniques for Si crystals.

tinue to reduce the horizontal dimensions.

The general field of plasma etching contains three distinct regions, each associated with a plasma density and an ion excitation energy:

- In the high-density gas region of plasma etching ($p > 100$ millitorr, where p stands for pressure), etching occurs by chemical reaction;
- In the medium-density gas region, called *reactive ion etching* ($p \sim 10$ millitorr), etching occurs by combining physical bombardment and chemical reaction; and
- In the low-density gas region, known as *sputtering* ($p < 1$ millitorr), physical bombardment is the dominant mechanism for removing material.

Within each major area, there are significant variations in the reactor designs, the plasma configuration, and the electrical biasing conditions.

Plasma etching, however, did have significant technical issues associated with it. The etching byproducts proved to be extremely corrosive, and vacuum pumping technology required major advances. Furthermore, discharge gases had to be neutralized using "scrubbers" that removed environmentally damaging gases, such as chlorine and fluorine, which cause the "ozone depletion effect."

With respect to the processed wafers, another technical issue began to arise as the submicron regime was researched and developed. Plasma etching with reactive ions was electrically damaging the thin SiO_2 insulator materials that comprise the ICs. This area is now under extensive study; and as device geometries and material film thicknesses continue to be scaled downward, the plasma damage problem is a major issue that needs to be addressed at each plasma processing step.

Incorporating Dopant into the Si Wafer

To achieve the desired electrical device structure, dopants must be selectively introduced into the crystal surface, in specific regions, to create the required dopant profiles as a VLSI IC is being fabricated. **Figure 19** shows the three major methods that have been used extensively during the evolution of manufacturing processes for discrete transistors and VLSI ICs.

To some degree, all three methods use another unique property of SiO_2, which was first reported by C. Frosh and L. Derick in 1957 and extensively researched later. They discovered that the primary dopant elements for silicon processing diffused very slowly through thin layers of SiO_2. This property was crucial to the "planar process." Basically, a thin layer of SiO_2 could be grown on the silicon wafer surface, and then the desired pattern could be etched through the SiO_2 using either hydrofluoric acid or plasma etching to expose the regions to be doped.

In the first technique, the surface of the wafer was exposed to a gas of the desired dopant. Depending on the temperature of the process, the gas would dissociate and the dopant element would diffuse into the Si, but not through the SiO_2. This technique, shown in Figure 19a, was first used in fabricational processes where the concentration control is critical, as in the diffused base junction of a bipolar device.

The second technique is based on solid-state dop-

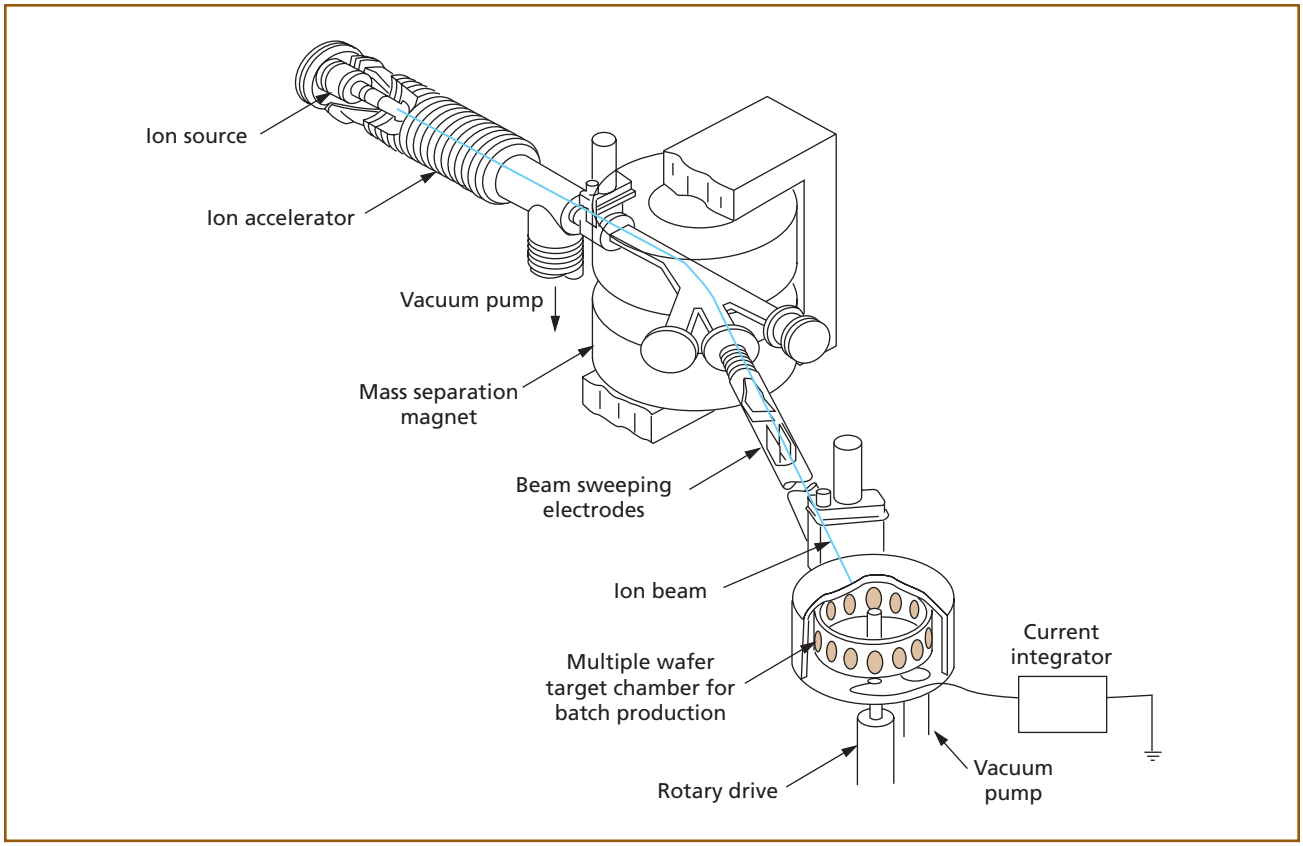


Figure 20.
Principle components of an ion implantation machine.

ing from a glass source, shown in Figure 19b. This technique introduces the dopant into a furnace gas stream, along with an oxidizing ambient, causing a glass to grow on the surface of the silicon wafer, which then acts as the diffusion source. It is used primarily for creating diffusions where the surface concentration should equal the solid solubility of the impurity in silicon, such as in junction bipolar emitters and MOSFET source/drains diffusions. The second technique is also used to dope polycrystalline layers, found in the gate structures of MOSFETs and the capacitor structures of DRAM cells. After the diffusion is completed, the doping glass source is removed from the silicon wafer surface with a hydrofluoric acid or a nitric acid solution.

Figure 19c shows the third dopant technique, called ion implantation, which came into widespread use in the mid-1970s. First a gas containing the dopant atoms is ionized, and then the ions are passed through a mass spectrometer, creating a high-purity ion beam. The beam is then accelerated to a specific energy, and the ions are implanted into the surface of the wafer. The three most common materials used to mask the regions of the wafer that are not being doped are SiO_2, polysilicon, and photoresist. Ion implantation, illustrated in **Figure 20**, offers device technologists many degrees of freedom in the formation of dopant profiles in the silicon surface. It can accurately set not only the energy (and depth) of the dopant profile, but also the dose. By measuring the current that flows into the wafer, it is possible to make a precise count of the dopant ions.

Today, ion implantation is used for almost all doping processes in which total dose can be accurately controlled over a range of 10^{+10} to 10^{+17} ions per cm^2. At least four technical issues must be carefully controlled in ion implantation. First, ions can build a charge layer in the various materials on the wafer surface and cause insulator breakdown. To resolve this problem, the wafers are exposed to electron flood guns that neutralize the wafer during implantation. Second,

the high-energy beam can also erode atoms off the internal surfaces of the implant machine and introduce undesired impurities into the silicon wafer. To control this problem, critical parts of the machine are made from silicon. Third, high-energy ions can create significant silicon crystal damage, which can alter the desired dopant profiles and also degrade device performance. Fourth, high-dose, high-energy production machines can cause significant wafer heating, which in turn can distort the wafers. Combating this effect requires adequate wafer cooling techniques.

Metallization Technology

The processes described in the previous sections are used to fabricate an IC's individual transistors, resistors, and capacitors. To form the desired IC, patterned thin-metallic films connect the individual bipolars, MOSFETs, resistors, capacitors, and diodes.

In the early years of discrete transistors, bipolar ICs, and MOSFET ICs, metallurgists explored a variety of metallization systems. Metals such as silver, gold, platinum, palladium, tungsten, and aluminum were popular choices. By the mid-1970s, however, almost all manufacturers found that an aluminum-copper alloy (Cu = 0.4 to 4.0 atomic percent) was the most practical material to use. It was an excellent conductor, easy to deposit and pattern, and it satisfied the reliability requirements for use in ICs.

Until the mid-1980s, a single layer of aluminum metallization was used to fabricate most ICs. It was then realized that using only one layer of metal severely limited the planar layout of the IC and the number of active devices per unit area. Researchers quickly substituted multiple layers of metal. The IBM Corporation was a clear leader in this field. Today, modern ICs at the 0.35-μm feature size typically contain as many as four to five layers of metal. While the processing associated with this multilayer metallization is complex, it is cost effective overall, because the size of the IC can be significantly reduced and its performance greatly improved.

As the feature sizes of modern ICs have decreased, the vertical walls and aspect ratios of contacts between the various metal layers and the silicon substrate have made the formation of reliable contacts more difficult. During the past several years, the use

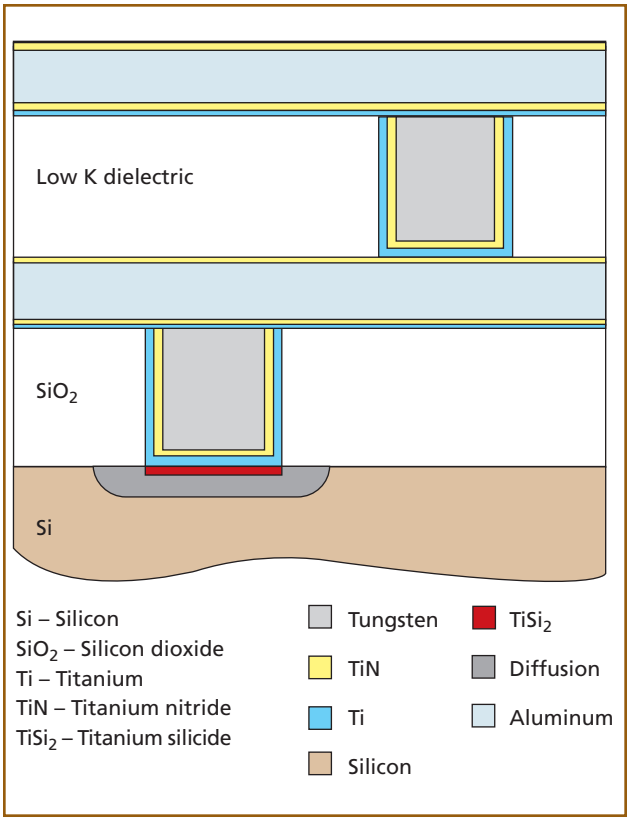


Figure 21.
Detailed cross section of a modern multilayer metal structure.

of tungsten, conformly deposited by CVD, has helped to solve this problem.

There are still, however, several major issues associated with the use of aluminum metallization. First, the aluminum conductors on an IC are subjected to extremely high current densities. For example, typical circuit design guidelines will specify current densities on the order of about $3.0 \times 10^{+5}$ amps/cm^2. The current density is a factor of 10^{+3} higher than current densities encountered in household wiring, creating a condition whereby the momentum of the conducting electrons is transferred to the aluminum atoms in the film, causing them to physically move. This phenomenon, called *electromigration*, has been researched extensively for the past thirty years.

Second, deposited aluminum films are usually under tensile stress, either as a result of the initial deposition conditions or the thermal cycling conditions experienced in operation. If the stress becomes excessive, the finely patterned lines will plastically deform and, in the worst case, void, creating what is known as

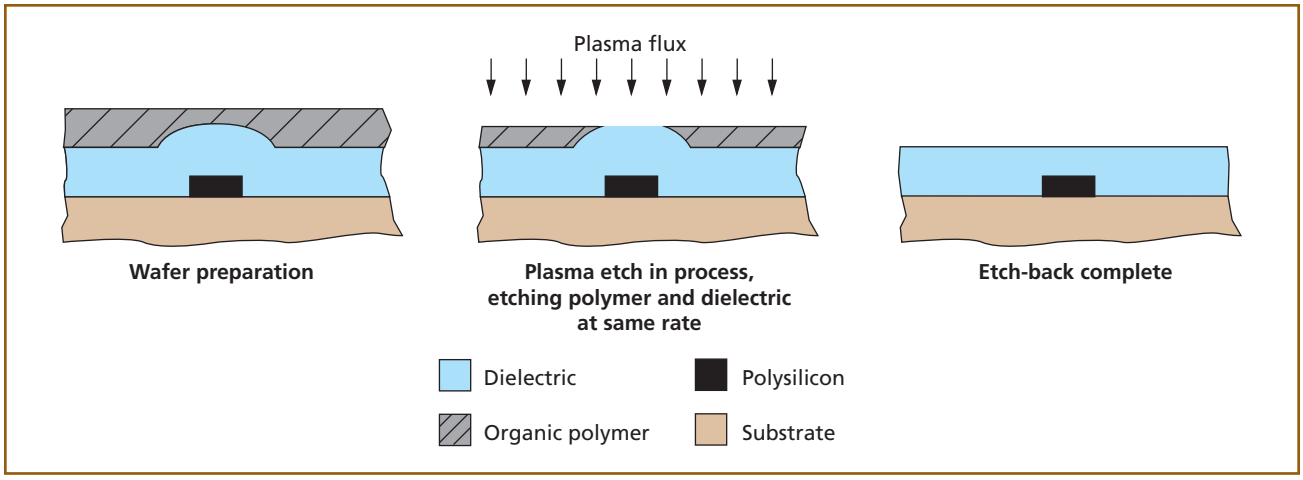


Figure 22.
Organic polymer planarization etch-back process.

stress migration. The separation in the aluminum line will cause the IC to fail. To avoid this type of failure in modern ICs with submicron feature sizes, the aluminum lines are sandwiched between conducting films of titanium nitride (TiN), as shown in **Figure 21**.

The use of multilayer metallization structures has raised a third issue, feature definition. As the metal layers cross each other and are separated by an insulator, a severe topology is generated on the wafer surface. The variation in surface height can exceed 1.0 μm and, in this condition, modern lithography cannot print the required feature sizes.

Technologists have presented two basic solutions to this problem. In the first solution, a thick layer of organic material is applied to the wafer surface after the intermediate insulators have been deposited. This material smoothes the surface to a large degree, but not completely. The organic material and part of the underlying insulator are then plasma etched, producing a fairly smooth surface, as shown in **Figure 22**. The etch rate of the organic polymer and the insulator must be equal for this process to work well. In some cases, geometrical effects associated with the organic material limit the ability to produce a truly planar surface.

The second process uses the technique that originally produced the flat silicon wafer, which involves polishing the intermediate insulator covering the wafer surface to achieve a high degree of planarity. This technique seems to contradict a general rule for handling wafers: Never touch the active surface of the wafer during fabrication. However, the existing expertise in polishing slurries, polishing pads, and cleaning techniques has made CMP the leading process used to produce planar multilayer metallization systems in modern VLSI ICs.

Device Passivation

Device passivation is another important field of IC processing and reliability. Passivation materials are introduced in semiconductor manufacture to ensure the initial fabricational yield, electrical performance, and extended reliability of the IC.

After the metallization process is completed, the silicon wafer is ready to be cut into individual ICs and packaged. The silicon wafer is covered with a thick layer of insulating material, usually an SiO_2 glass that contains phosphorus or a plasma-deposited silicon nitride material (SiN). Commonly used variations in the passivation layer result in layered structures, or compounds, referred to as silicon oxynitrides (an amorphous tertiary material that contains varying amounts of silicon, oxygen, and nitrogen). Initially, the passivation layer protects the IC from mechanical damage during initial circuit testing and the sawing and packaging operations. After the IC is packaged and tested, the passivation layer continues to protect it from the undesired effects of ionic contamination in the packaging compounds.

SiO_2 has another unique property. Although it is an excellent diffusion barrier to the dopants used in

the manufacturing process, SiO_2 can be easily contaminated with alkali ions such as lithium, sodium, potassium, and cesium. The diffusion rate of these materials in SiO_2 decreases rapidly with the mass of the ion. Sodium, an element found everywhere on the surface of the earth, is the ion most likely to degrade the operation of discrete bipolars, discrete MOSFETs, and ICs. In the operational temperature range of semiconductor devices (typically, -40°C to 100°C), sodium diffuses rapidly through SiO_2, making sodium diffusion barriers and sodium "getters" necessary for ensuring high electrical parameter yields and long-term device reliability in the IC manufacturing process. (A *getter* is a chemical or a process that absorbs and neutralizes an impurity.)

In 1964 D. Kerr of IBM made a major breakthrough in passivation.[19] Kerr left the phosphorus glass used in a bipolar process on the final silicon wafer. When submitted to reliability aging, the packaged bipolar devices he was fabricating demonstrated exceptionally stable operation. This discovery led to the extensive characterization of the phosphosilicate glass system. Since then, other sodium diffusion barriers have been developed, most notably silicon nitride, by J. Dalton in 1966. The combination of these two materials forms the basis of all passivation technology in today's VLSI ICs.

Present Manufacturing Facilities

During the past thirty years, the manufacture of VLSI ICs has grown exponentially. The need to meet the electrical performance demands (such as clock frequency and power consumption) of system designers and the quantities of VLSI ICs required in the marketplace has forced the manufacturing technology, as described in the earlier sections, to evolve rapidly. Processes have become quite complex, and the wafer size continues to increase. IC manufacturing has transformed itself from a labor-intensive industry to a capital-intensive industry. Today, a modern, competitive manufacturing facility costs in excess of $1.0 billion to construct. About 20% of a facility's cost goes into the construction of the clean room, including the support facilities of water purification and recycling, air purification with temperature/humidity control, and all other aspects of the infrastructure. The remaining 80% is allocated for the manufacturing equipment. The cost estimates of modern manufacturing equipment are:

- Lithography exposure tools—about $7 million each,
- Plasma processing machines—about $2 million each, and
- Furnaces and ancillary equipment—about $1.0 million each.

To ensure that manufacturing plants are managed efficiently, considerations such as operations research—including wafer queuing theory, operational equipment efficiency, wafer process times, inventory control, and overall cost of ownership analysis—are now as important as the purity of the chemicals and the silicon wafers that are used in the facility. The modern facility is a fascinating blend of advances in leading-edge technology and economic management theory. Given that the lifetime of most IC technologies for leading-edge product manufacture is only three to five years, factories must also be flexible enough to be quickly upgraded to accommodate several generations of manufacturing technology.

In conjunction with these financial issues, the industry has by necessity entered a "post-yield-limiting era." No longer is VLSI IC yield predicted by defect density theory and dominated by defects. With such enormous capital investments, each fabricational process has been engineered to virtually eliminate defects. Modern DRAM and microprocessor manufacturing plants have wafer yields (number of wafers finished/number of wafers started) in excess of 95% and IC yields (number of working ICs per wafer/number of potential ICs per wafer) in excess of 90%.

The Future

Today's microelectronics industry faces major technical and economic issues. This section discusses the paths that the industry may take in these areas.

Introduction

At present, 0.25-μm VLSI CMOS technology is being introduced into manufacture for the production of 64-Mb ($64e10^{+6}$) DRAMs and advanced microprocessors, and 0.18-μm VLSI CMOS technology is under advanced development, scheduled for introduction to manufacture in the year 2000. The

major technical issues of these generations of VLSI CMOS have been largely resolved. The financial issues associated with implementing these technologies, however, will represent a significant challenge for most IC manufacturers.

The next-generation technology, 0.13-μm VLSI CMOS, is in the advanced stages of research, and the fundamental issues facing a 0.10-μm VLSI CMOS technology are in the early research phase. Major technical issues concerning these generations of technology need to be resolved, foremost among which are lithography, metallization, gate dielectrics, and electrical parameter control. And, finally, financial issues may be the fundamental limiting factor for introducing advanced technologies.

Lithography

Lithography is the fundamental technology for the mass manufacture of ICs. If IC technology is to continue to scale in feature size, it will require major advances in lithography. This issue is being addressed by research and development activities taking place in several major fields.

In the field of optical lithography, exposure wavelength is a fundamental limiting parameter for the resolution of minimum feature size. Evolutionary optical lithography research and development in the wavelength region of 193 nm (argon fluoride lasers) should yield optical systems that will allow the continued scaling and production of ICs with a minimum feature size of about 0.15 μm. Because light, with a wavelength of about 0.15 μm, is strongly absorbed by almost all materials, future optical lithographic imaging systems with such short wavelengths will need to be constructed using reflective mirrors, rather than the refracting lenses used today.

Lithographic research efforts in the area of extreme ultraviolet light, with wavelengths of 50 nm to ~10 nm, have used mirror technology. Research currently being conducted at $\lambda = 13$ nm uses mirrors based on the Bragg reflection principle. These mirrors are constructed from the *super lattices* of materials—layers of alternating high- and low-density materials whose thickness must be critically controlled. Because Bragg mirrors are extremely difficult to manufacture, imaging system design and routine mirror fabrication have not yet been used in any extensive commercial application. Furthermore, the mask technology used with them must also be reflective, and the resist systems must be surface based, owing to the highly absorbing nature of all materials in this wavelength region.

In another approach, X-rays with a wavelength of about 1.0 nm are being explored in a unity-printing mode, because neither a lens nor a mirror technology exists. In this mode, the critical technology is masking, since the mask substrate must be a thin membrane—about 100 nm thick—to remain essentially transparent to the exposing X-rays. The IC features are formed on this membrane in a strongly absorbing material, such as a low-stress tungsten or a tantalum alloy. To minimize diffraction effects during exposure, the mask must be placed very close—about 5.0 μm—to the surface of the Si wafer. Producing high-quality, defect-free masks with no physical distortion is extremely difficult and has yet to be demonstrated as an efficient manufacturing technology.

Although attempts have been made to use ion beams in lithography, fundamental physical effects have limited all approaches. No method has been discovered to achieve cost-effective throughput for a low-intensity ion beam exposure system. On the other hand, if the ion beam is high in intensity, the ion-ion interaction leads to unacceptable image blurring and reduced resolution.

Electron beam technology—an established technology for mask making and IC research activities—presents a very promising lithographic approach. However, the current reticule production systems, which use a finely focused electron beam to write each pixel, are too slow for practical IC production use. Only projection electron beam systems offer a potential throughput that is cost effective. Scientists are conducting research and development on several variations of electron beam projection technology. A critical feature of each of these systems is the masking technology. Initial attempts at projection electron beam lithography—using either a fixed or variable aperture concept to construct an image from a series of rectangles and triangles—to date have not yielded a throughput that is cost effective.

More recently, research into an advanced, cost-effective system called Scalpel™, which uses a fixed mask and a unique scattering technique to define the electron beam pattern, is very promising for feature sizes smaller than 0.15 μm.[20]

In general, the physics, chemistry, and technology of electron beam lithography have been well established. But the critical technical issues concerning residual pattern placement errors and cost-effective wafer fabrication will need to be continually addressed until a truly high-volume, sub 0.15-μm lithography system can be introduced into manufacturing facilities.

Metallization

The technology of metallization now represents more than half of the process of Si wafer fabrication. This is a result of the exponentially increasing number of transistors and logic blocks, and the need to interconnect them. At present, four to five metal layers are being used on new VLSI designs in 0.25-μm CMOS technology.

As feature sizes continue to decrease, current density and parasitic capacitance are becoming major issues in determining overall circuit performance. Higher limits of current density are needed in power distribution lines, clock signal lines, and data buses. As a result, research and development into material systems, such as copper—with lower resistivity and better electromigration resistance than aluminum—is now very active.

Also, as the size of metallization spaces continues to shrink, the parasitic capacitances between lines are dramatically increasing. The response to this issue is research and development of insulators with reduced dielectric constants, as compared to SiO_2 ($k = 3.9$). A first generation of fluorinated SiOF compounds is being developed with $k = 3.5$, and longer-term research into organic polymers with $k = 2.0$ to 2.5 appears promising.

Gate Dielectrics

The scaling of all feature sizes, both in the lateral and vertical dimensions, has now led us to the point where fundamental considerations, such as quantum mechanics, are factors critical to further scaling. As SiO_2 layers about the thickness of 2.0 nm are used in research and development, significant gate insulator tunneling currents are observed in MOSFETs. While these currents may not pose a significant issue to circuit design or reliability, they can severely limit low-power applications of future VLSI CMOS, many of which are in portable, battery-operated applications.

It may be necessary, therefore, to replace SiO_2 as the gate dielectric and use a high-dielectric material, such as tantalum pentoxide, Ta_2O_5 ($k \approx 24$), or titanium dioxide, TiO_2 ($k \approx 100$). The quantum mechanical tunneling currents are suppressed by the thicker film, and the higher dielectric constant allows the gate electrode to continue to control the transistor action.

Electrical Parameter Control

Continued technology scaling increases the significance of fundamental limitations in transistor parameter control. As the MOSFET continues to shrink, the total number of active dopant atoms under a given gate decreases. Statistical theory indicates that, with present crystal preparation techniques, random fluctuations in doping density will seriously affect MOSFET device parameter control. Such an effect can virtually stop device scaling, because many designs, such as DRAMs, require precisely matched transistors within sense amplifier circuits that measure the small amounts of charge stored in each memory cell.

Financial Issues

If the costs of new manufacturing equipment continue to rise, they can severely limit the introduction of new technological advances, creating an effect similar to one that exists in the airline industry. Technologically, airplanes can routinely fly faster than the speed of sound; however, because of the financial and technical complexity issues associated with supersonic flight, the airline industry has instead adopted the concept of the jumbo jet and mass passenger transport. In a similar way, VLSI ICs may evolve into fully integrated, complete electronic systems on a single circuit. This will reduce overall system cost and improve total electrical performance without further dramatic reductions in feature dimension. Several major corporations recently announced that they plan to integrate a number of IC products into a single VLSI IC. Such an IC will be fabricated with a modular type of VLSI tech-

nology and will include large logic blocks; memory in the range of $10e^{+6}$, or higher; and analog functions.

Pessimists have argued repeatedly that the IC industry would slow its progress in technology, but to date, it has not. The industry has reached the financial point that manufacturing plant construction is exceedingly costly. Consequently, many smaller corporations have adopted joint ventures between and among themselves as a workable solution, or else they rely on huge VLSI Si foundry corporations for their product manufacture.

Another aspect of VLSI IC economics is that national standards of living are becoming dependent on microelectronics manufacturing capability. On the national level, governments are subsidizing microelectronics research and development and the building of VLSI IC manufacturing plants to improve the economic prospects of their countries. But if the cost of research and development and manufacturing facilities in the microelectronics industry continues to climb at an exponential rate, as it has in the past, only international cooperation will keep these costs affordable. There are already indications that such a possibility may evolve.

In the area of advanced semiconductor research and development, organizations such as SEMATECH, initially a U.S. government/industry consortium, have already engaged the active participation of foreign corporations. Also, in the area of research and development for the manufacture of 300-mm (12-inch) silicon wafers, the subsidiary formed by SEMATECH, called International 300-mm Initiative (I300I), has recently agreed to work with the SELETE Consortium of Japan to share technical information to develop a common set of material and equipment standards. These actions indicate that R&D costs (and the associated technical risks) are becoming too burdensome for any individual corporation or national consortium of corporations to handle. In addition, the semiconductor equipment manufacturers will only be able to economically survive if they can sell to a global market with an international set of standards.

Social and financial issues, not technical issues, may ultimately limit the widespread application of advanced deep submicron 0.10-μm VLSI IC technology. The social revolution of the early 1990s finds its roots in national financial collapse and restructuring primarily caused by unchecked technological competition in the military fields.

Conclusion

The historical revolution in microelectronics—from the first step of the invention of electrical amplification in a single semiconducting device in 1948, to present day VLSI IC technology, in which $\sim 5e10^{+8}$ transistors exist on a single piece of semiconductor crystal—is completely unparalleled in any other technology in the history of mankind. The science, technology, and financial issues confronting the VLSI industry are international in scope, and its technical future is very difficult to predict. The "killer" technology for VLSI ICs has not been identified. Technically, scientists have demonstrated quantum-level device structures that would further reduce the size of a device capable of performing a logic or memory operation, but they have yet to seriously address the technological and financial aspects of fabrication and volume production. The future of microelectronics will be the most interesting story to unfold in the next two decades.

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(Manuscript approved November 1997)

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